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Disruptive Wide Bandgap Semiconductors, Related Technologies, and Their Applications

Edited by Yogesh Kumar Sharma

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Notice

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Meet the editor

Dr. Yogesh Sharma was born in Amritsar, India, in 1983. He received his MSc degree in Physics from the Punjab University, Chandigarh, India, in 2004. Following this, he worked as a lecturer for 3 years in a college and taught graduate-level mathematics and physics courses. Later, he moved to the USA to pursue his PhD degree. He started his integrated PhD program at the Auburn University, AL, USA, in wide bandgap semiconductors, SiC and GaN. He completed his PhD degree in 2012 and ever since has been working in wide bandgap semiconductor technology. He has authored/coauthored over 50 journal/conference papers. He is the holder of one patent and is a reviewer of various international journals. He is a member of IEEE and IET.

Contents

Preface

Devices fabricated from wide bandgap semiconductors such as SiC and GaN are considered to be a third generation of semiconductor devices. These devices will change the power industry significantly in the near future. High-electric field of breakdown, low-intrinsic carrier concentration, and high-bandgap mean that the devices fabricated from these materials can outperform their Si counterparts in high-power regimes and hence enable engineers and researchers to build more efficient electrical systems. At present time, more efficient electrical systems are necessary to limit the amount of CO_2 emissions and make the planet greener. In this book, we try to cover the main aspect of SiC and GaN technologies. The book is organized in the following manner.

The introductory chapter deals with the basics of power devices and explains why it is advantageous to use SiC devices in power electronics. The use of SiC devices in hybrid SiC technology is demonstrated, and the issues related to it are addressed. Challenges such as the quality of the oxide-SiC interface and ohmic contacts on SiC are also discussed briefly in this chapter. The second chapter covers an in-depth analysis of the main differences of, while developing the simulation platforms for, these technologies using technology computer-aided design (TCAD) tools. Most of the tools that have been established are more suitable for Si technology, so special attention is needed while using them to develop wide bandgap semiconductor devices. The third chapter highlights the processing aspects of SiC devices. This chapter addresses the questions such as why SiC devices need a special set of expertise and tools for fabrication and why they are more expensive, and so on, as compared to their Si counterparts. The fourth chapter focuses on the development of packaging technology for power semiconductor devices. Packaging technology such as Ag sintering, copper wire bonding, and wire bond-free and planar modules with low inductance is discussed in this chapter. In Chapter 5, the current stage of SiC devices is summarized. The evolution of SiC devices, including different types, and market response to these devices is discussed. Also, this chapter addresses some practical challenges, which engineers have to face while using these devices.

The last two chapters deal with GaN technology. Chapter 6 reviews the state-of-the-art GaN Schottky diode technology. This chapter covers the background of GaN-based Schottky diodes, current transportation theory, Schottky material selection, contact quality, and thermal stability of Schottky contact to GaN. This chapter also discusses the evolution of epitaxial and device structures of the GaN-based lateral, quasi-vertical, and vertical Schottky diodes as well as AlGaN/GaN field effect Schottky diodes. Also, this chapter gives a viewpoint on the forthcoming development of GaN-based Schottky diodes. The last chapter, Chapter 7, deals with the application of GaN devices in electric vehicles (EVs). It presents the application of the GaN gate injection transistor (git) in inductive power transfer (ipt) for electric vehicles.

The chapters in this book have been contributed by the respected researchers and technology experts and cover up-to-date developments in wide bandgap semiconductor technology. I hope that graduate students, researchers, engineers, and technology experts who have been working in the exciting field of SiC and GaN power devices will find this book useful.

I would like to thank all the contributors for their hard work and support during this project. Special thanks go to Ms. Dajana Pemac of IntechOpen for her assistance and guidance during the writing of this book.

My greatest acknowledgement goes to my father (Jagdish Ram Sharma) and mother (Kusum Sharma) who have taught me to be a good person and respect all. I would like to thank my brother (Munish Sharma) and sister (Monika Sharma) from whom I have learned a lot throughout the life. Special thanks go to my beloved wife (Vasudha Dewan) and daughter (Ayana Sharma) for their love and patience during this work. Without my wife's encouragement, I would not have had started working on this project.

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Chapter 1

Introductory Chapter: Need of SiC Devices in Power Electronics - A Beginning of New Era in Power Industry

Yogesh K. Sharma

Additional information is available at the end of the chapter

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1. Introduction

1.1. Development in device technology

Germanium (Ge) was used as a material to manufacture the first semiconductor device. Ge was touted as the semiconductor material of the future. But after the arrival of silicon (Si), it turned out to be more suitable for several reasons [1–4]. The main reason is to get the high-purity Si from silica, which is widely available. Also, it is easy to modify Si into n-type, p-type, and semi-insulating materials [5]. In addition to this, Si can easily be converted into its native oxide, SiO_2, with the help of thermal oxidation at the relatively low temperature of around 900°C [6–8]. These features make Si, as a material, semiconductor industry favorite. Global semiconductor industry, and currently, is worth more than $430 billion [9]. Around 9–10% of this worth is in smart-integrated circuits and electronic power devices [10, 11]. These power devices processed more than 50% of our electricity [12, 13]. It has been reported that by 2025, Power Electronics market size will be worth $39.22 billion [9]. As we can envision, power devices have a larger impact on the economy of any country. Power semiconductor devices are crucial to determine the cost and efficiency of electronic systems.

In power systems, diodes (uncontrolled switch) and transistors (controlled switch) play a major role. A small increase in their efficiency and power-handling capability make the systems more powerful and energy efficient. In the early 1950s, the advent of solid-state devices like bipolar transistors led to the phasing-out of vacuum tubes [13, 14]. These Si devices created the second wave of electronic revolution possible, with Si as the material of choice. Power devices had played a vital role in electronics industry. There is a rich history about the evolution of power devices. Initially, there were only bipolar devices with a blocking capability of 500 V (or so) and high-current capabilities. But after sometime, in the 1970s, International

Rectifier Inc. launched the first metal-oxide-field effect transistor (MOSFET) [15]. The idea was to switch to MOSFETs from BJTs in high-power applications. The MOSFET is a unipolar device, meaning there is only one type of carriers (electrons) which participate during conduction and thus has a high switching speed. Another advantage the MOSFET has is a voltage control device and hence it is easy to switch (on-state to off-sate). On the other hand, the BJT is a current control device and as a result not so easy to control. Voltage control instead of current control means that less internal energy loss occurs in a device. Also, with an increasing switching speed, other components of the system like filters (consist of capacitors/inductors) can be reduced in size. Si-MOSFETs could be designed to handle voltages up to 1000 V and in special case (super-junction) to 1200 V [13, 16, 17]. At voltages higher than 1000 V, the on-state losses of silicon MOSFET start increasing drastically and hence no longer able to perform efficiently. The performance predicament between bipolar and MOSFET devices was solved with the invention of an insulated gate bipolar transistor (IGBT). This is a new device structure where the best electrical features of bipolar (BJT) and unipolar (MOSFET) devices were combined together. With this new device structure, it is possible to cover the blocking voltage range from 750 to 6500 V. Like BJTSs, IGBTs are also able to carry high-forward current.

1.2. Diode and transistor

In power electronics to build electrical systems, we need both a rectifier and a transistor. The features of an ideal rectifier and a transistor are shown in **Figure 1**. For an ideal rectifier, there is no voltage drop in on-state and no current flows in off-state. Hence, there is no power loss during the operation of a rectifier, **Figure 1(a)**. Similarly, in the case of an ideal transistor, there is no power dissipation during commutation from on- to off–states, **Figure 1(b)**. The waveforms of an ideal power switching system are shown in **Figure 2**. But in reality, this is not the case, either with devices or power systems. The characteristics of a real (non-ideal) rectifier/transistor are shown in **Figure 3**, and the corresponding waveforms of a power system are shown in **Figure 4**. The total power loss occurred in a switch (P_{Total}) and is given by:

$$P_{Total} = \Sigma P = P_{conduction} + P_{on} + P_{off} = P_{turn-on} + P_{turn-off} + P_{on} + P_{off} \quad (1)$$

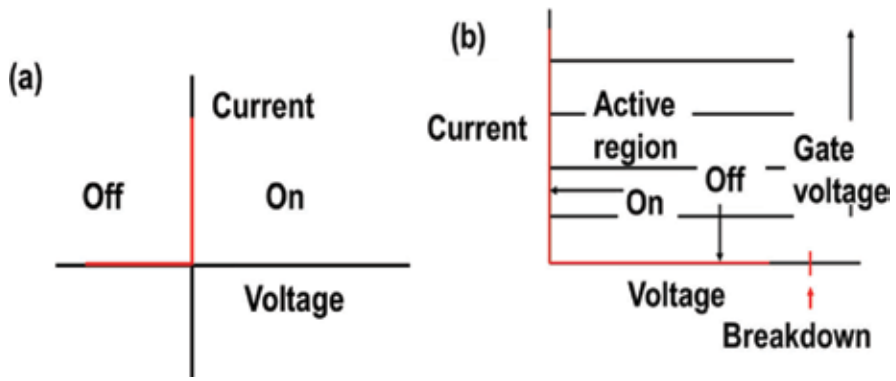

Figure 1. Ideal current-voltage characteristics of a diode (a) and a transistor (b).

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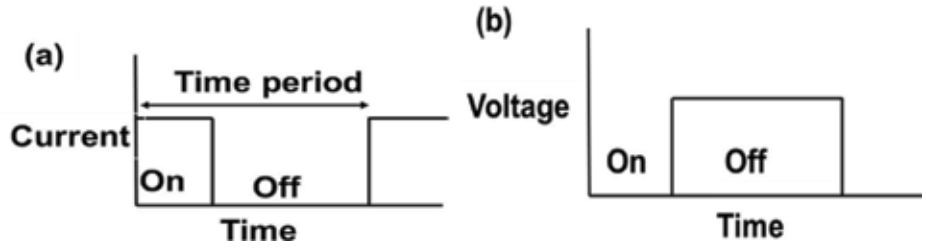

Figure 2. Switching waveforms of an ideal power system, (a) Current versus Time and (b) Volatge versus Time.

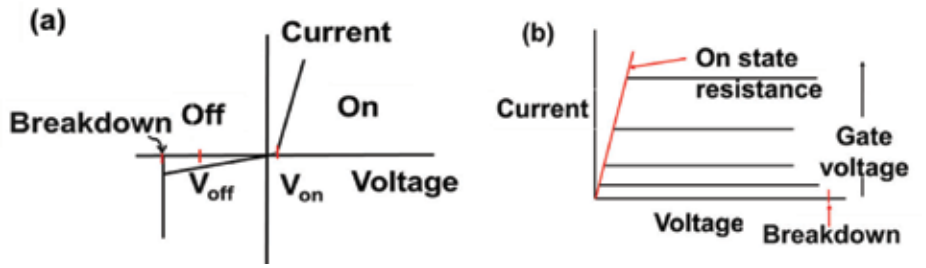

Figure 3. Real (nonideal) current-voltage characteristics of a diode (a) and a transistor (b).

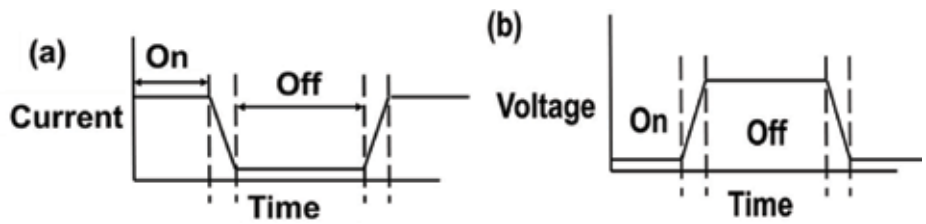

Figure 4. Switching waveforms in a real (nonideal) power system, (a) Current versus Time and (b) Volatge versus Time.

At high frequencies, the switching power loss dominates, so fast switching power devices are desirable. At low frequencies, on-state power loss dictates, so power devices with a low on-state resistance are vital.

1.3. Conduction mechanism of a power device

As mentioned previously with the help of an IGBT, it is possible to increase the operating voltage range of a power transistor without compromising its on-state losses. In unipolar devices like Schottky diode (SBD), MOSFET, the blocking capability of the device increases with an increasing drift region thickness. With an increasing thickness, the conduction losses of a device also increase. In a bipolar device, because of conduction modulation (injection of minority carriers (holes mainly) into the n-type drift region), this is not true, and the conduction losses are low despite a thick drift layer. For example, the specific on-resistance (R_{pin}) of a drift layer (blocking layer) for a unipolar device, n-type Schottky diode', is given by [18].

$$R_{pin} = T_{drift}/qN_{drift}(\mu_{n+}\mu_{p}) \quad (2)$$

where T_{drift} = thickness of the drift layer; N_{drit} = doping concentration of the n drift layer; μ_n/μ_p = bulk mobility of electrons/holes in semiconductor.

For an n-type pin diode, the specific on-resistance (R_{pin}) under high-current density condition is given by

$$R_{pin} = T_{drift}/q\mu_n N_{drift} + q(\mu_{n+}\mu_{p})\Delta p \quad (3)$$

Because of the extra term, $q(\mu_{n+}\mu_{p})\Delta p$, in the pin diode, the specific resistance will be lower as compared to Si Schottky diode. In the case of high injection $\Delta p >> N_{drift}$, the resistance will decrease considerably during conduction. Now, in order to get the diode into the blocking mode, minority carriers (corresponding to Δp) have to be removed from the drift region. These minority carriers in the drift region cause stored charge in the device and hence increase the switching losses. As a result, the operating switching frequency limit for bipolar devices (PIN or BJT) is lower, as compared to unipolar device (SBD or MOSFET). With the help of a wide-band semiconductor material like SiC, there is no need to switch to Si IGBT, as we can realize a high-blocking capability (>1200 V) SiC MOSFET without increasing the on-state losses. The specific on-résistance (R_{on}) of a MOSFET is given by [19, 20].

$$R_{on} = 4V^2_{blocking}/\mu_n \varepsilon_S E^3_{critical} \quad (4)$$

where μ_n = bulk mobility of SiC; ε_S = permittivity of SiC; E_C = critical electric field of break-down for SiC; $V_{blocking}$ = the desired blocking voltage.

Bulk electron motilities are similar for low-doped Si and SiC (900–1200 cm^2/Vs) [24]. However, $E^{SiC}_{critical} = 7\ E^{Si}_{critical}$, so that for a given blocking voltage, the specific on-resistance can be a factor of 343 times lower for SiC devices. This is the reason why we need a wide-band gap semiconductor material for power device.

2. Application of SiC devices in hybrid module technology

There are a plethora of applications where these devices had been used and have shown their positive impact, and many more potential applications are on the horizon [21–23]. Although there are different kinds of SiC devices available, the most interesting ones are Schottky diodes and MOSFETs. These devices can be used to build either full SiC modules or hybrid SiC modules. In a hybrid SiC module, conventional Si diodes are replaced by Schottky diodes while the transistors are still Si IGBTs. With hybrid approach, we can maintain the cost of an electronic system down but the power saving would not be as much as it can be by using full SiC modules. The fabrication of SiC devices is more complicated and costly as compared with Si counterparts. The situation is more compounded for SiC MOSFETs. SiC MOSFETs are not only more expensive than SiC Schottky diodes but also there are only few suppliers who can provide these devices with limited current ratings. As a result, it makes more sense to build

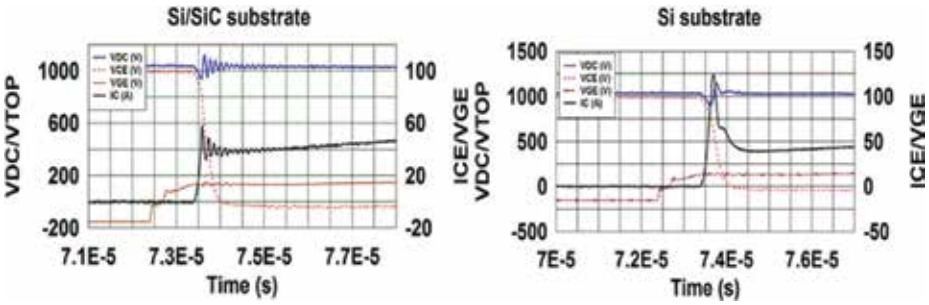

Figure 5. Output waveforms obtained for hybrid 1.7 kV SiC (a) and Si substrates (b) obtained during the first turn-on of the IGBT. These devices were tested at 150°C.

hybrid systems. Also at present, hybrid approach strikes a good balance between cost and efficiency achieved by these modules [24–27]. Also, it is worthwhile to point out that although SiC diodes and MOSFETs are available at 1.7 kV and lower voltages, there is no MOSFET supplier at 3.3 kV. Also, SiC diode technology is more matured and has been around for some time as compared to SiC MOSFETs. SiC diodes were made available commercially in early 2000s, while the first SiC MSOFET came to the market in 2011 (by CREE).

2.1. 1700 V Si/SiC hybrid technology

The results of a double-pulse test done on a hybrid substrate, built using 1 GBT and 1 diode (Si or SiC), are shown in **Figure 5**. These substrates are manufactured to conduct only 50A. By executing this test, we can evaluate the transient behavior of both IGBT and diode. In our case, we are interested in SiC Schottky diode's transient behavior and power losses suffered by it. The external gate resistors, $R_{gon} = R_{goff} = 6\ \Omega$, and the value of inductance (L) used is 260 μH. The waveforms during the second turn-on of the IGBT are recorded and are shown in **Figure 5**. The input voltage used for the test is around 1050 V. **Figure 5** shows that the peak reverses recovery current overshoot (I_{rr}) increases significantly to 87A, if Si diode is used instead of an SiC diode. The values of I_{rr} for Si and hybrid SiC substrates are listed in **Table 1**. Although the value of I_{rr} is lower for hybrid substrate, some oscillations in the current waveform are observed. The reverse recovery charge, Q_{rr}, is minute (3μC) in the case of SiC diode. This low Q_{rr} can be transformed into a low-energy loss during a switching event. Also, for hybrid SiC substrate, the reverse recovery energy (E_{rec}) is 1 mJ. The corresponding value for Si substrate is 11 mJ. All these tests are done at 150°C. The test setup used to perform a double-pulse test is shown in **Figure 6**.

2.2. 3300 V Si/SiC technology

In order to build 3.3 kV hybrid SiC substrates, two 1.7 kV, 50 A diodes are packaged in series. Again, the idea of using these diodes is to reduce the overall losses as compared with Si modules. These 3.3 kV modules can be used in wind power, solar energy, and rail-car applications. Like 1.7 kV hybrid modules, new system topologies can be realized with the help of these modules. Because of the limited availability of 3.3 kV SiC diodes, 1.7 kV SiC diodes are used to realize this high-voltage hybrid technology. All the diodes used to build these substrates are chosen carefully (e.g., the devices with similar V_F) so that there is no problem during current sharing in SiC diodes. This is very crucial for the reliability of these substrates. The waveforms

At 150 °C, 1.7kV	Full Si	Hybid Si/SiC
V_{line} (V)	1049	1056
dV_{ce}/dt (V/μs)	1372	1319
I_{rr} (A)	87	21
Q_{rr} (μC)	22	3
E_{rec} (J)	0.011	0.001

Table 1. Comparison of various parameters extracted for Si and hybrid 1.7 kVSiC substrates at 150°C from a double-pulse test.

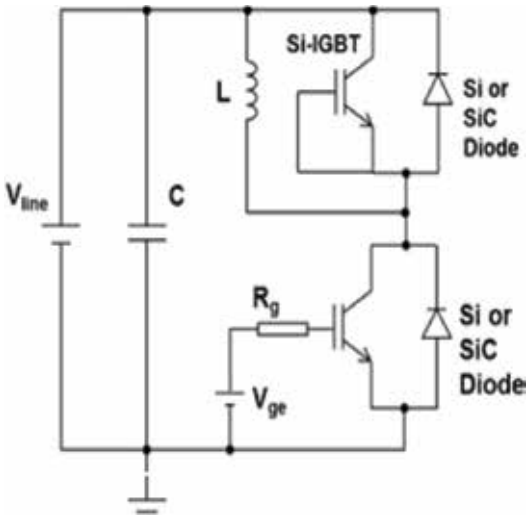

Figure 6. The schematic of a double-pulse test bench used to test devices.

during the second turn-on of the IGBT at 150°C are recorded and are shown in **Figure 7**. For a di/dt = 1100 or 1388 A/μs, a reverse recovery current overshoot (I_{rr}) of 128 A is observed for an Si substrate, which is higher than that of a hybrid SiC substrate (65A). The reverse recovery energy loss occurred in a substrate during the transient is E_{rec}, and the values for E_{rec} (Si) and E_{rec} (SiC) are 0.199 and 0.01 J, respectively. This represents a reduction of about 95% for hybrid substrate. Other transient parameters for the substrates, namely Q_{rr}, $E_{on,}$ and E_{off} (J), are also listed in **Table 2**. **Figure 8** shows the picture of a 3.3 kV, 200A hybrid SiC substrate. Again, like 1.7 kV hybrid substrates, 3.3 kV hybrid substrates are prone to electromagnetic interference (EMI), caused by the oscillations observed in the output waveforms.

3. Processing challenges of SiC devices

The fabrication of SiC devices is more demanding and complicated as compared with Si devices. Intrinsic properties of SiC make the devices suitable for high operating temperatures

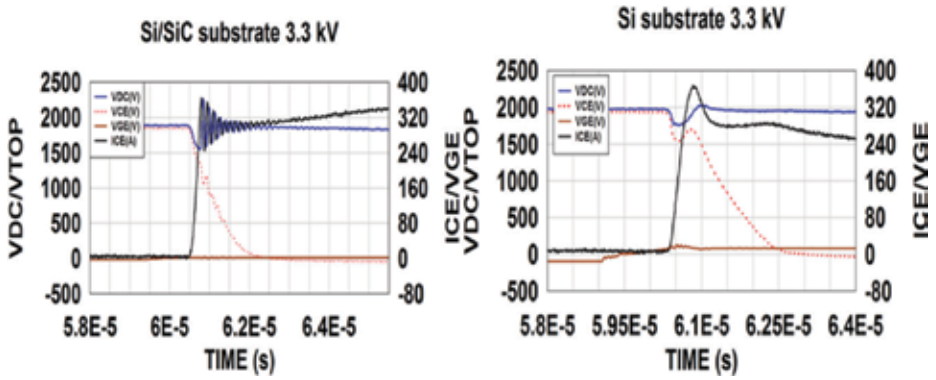

Figure 7. Output waveforms obtained for hybrid 3.3 kV SiC (a) and Si substrates (b) obtained during the first turn-on of the IGBT. These devices were tested at 150°C.

At 150 °C, 3.3kV	Full Si	Hybid Si/SiC
V_{line} (V)	1800	1800
dI_{ce}/dt (A/μs)	1100	1388
I_{rr} (A)	128	65
Q_{rr} (μC)	167	13
E_{rec} (J)	0.199	0.01

Table 2. Comparison of various parameters extracted for Si and hybrid 3.3 kVSiC substrates at 150°C from a double-pulse test.

(>200°C). But at the same time, due to its intrinsic properties, it is difficult to perform any electrical and physical change to the material at temperatures lower than 1000°C. That means in order to fabricate an SiC device, different set of tools are required as compared to Si device world [28–31]. The electrical and physical properties of Si and SiC are listed in **Table 3**.

3.1. Oxidation of SiC

In an oxide/semiconductor system, there are different types of charges which are present in the system. These charges are not desirable and greatly influence the electrical properties of a device. For example, the threshold voltage of a MOSFET and the breakdown voltage of a power, device, could change significantly because of these charges. These charges are divided into four types—mobile oxide charge, fixed oxide charge, oxide trapped charge, and interface trapped charge—and are shown in **Figure 9** [32].

At present, interface trapped charge is a key hurdle for the silicon carbide MOS R&D community. The origin of these charges is not well understood but may be related to mainly silicon- and carbon-dangling bonds, carbon clusters, carbon dimers in the SiC, and oxygen vacancies in the oxide very near to the interface [33–36]. Interfacial traps create localized energy levels in the energy band gap of SiC. These interface traps form potential wells that capture electrons

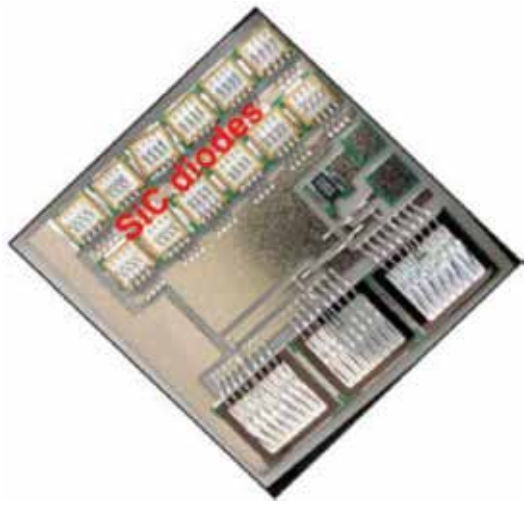

Figure 8. A picture of a 200 a, 3.3 kV hybrid SiC substrate.

Semiconductor	Si	3C-SiC	6H-SiC	4H-SiC
Bandgap (eV)	1.12	2.4	3.03	3.26
Breakdown Field (MV/cm)	0.25	>1.5	2.4 parallel to c-axis > 1, perpendicular to c-axis	2.2 parallel to c-axis
Intrinsic Carrier Conc.(cm^{-3})	1.45e10	1.5e-1	1.6e-6	5e-9
Electron Mobility @ n_d =10^{16} cm^{-3}	1430	800	60 parallel to c-axis 400 perpendicular to c-axis	900 parallel to c-axis 800 perpendicular to c-axis
Hole Mobility , @ n_a =10^{16} cm^{-3}	480	40	90	115
Saturated Electron Vel (10^7cm/s)	1	2.5	2	2
Thermal Conductivity (W/cm-K)	1.5	3.2	3.0-3.8	3.0-3.8

Table 3. Electrical and physical properties of Si, 3C-SiC, 6H-SiC and 4H-SiC.

and holes. In addition, charge traps also act as Columbic scattering centers [37]. These two effects decrease the effective channel mobility in a MOSFET. In Si world, a typical oxidation temperature employed to grow an oxide layer is 1050 (dry oxidation) or 850°C (wet oxidation). The oxidation step is followed by an annealing step in H_2 gas ambient at 800°C for 30 min. In 4H-SiC, typical oxidation temperature to grow a layer of native oxide is 1150°C. In some cases, it could be as high as 1300 or 1500°C which requires special oxidation furnaces, not the conventional quartz furnaces used for Si oxidation [38–41]. To use SiC devices to their full potential, we must continue to work to improve the electrical characteristics of the oxide/SiC

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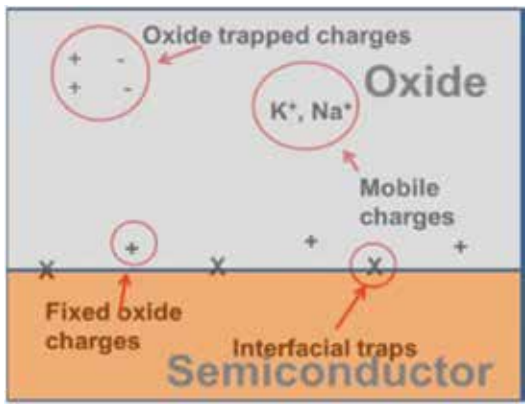

Figure 9. Different types of charges in oxide/semiconductor system [10].

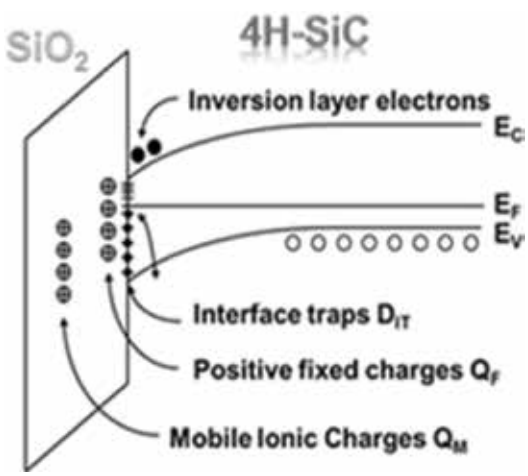

Figure 10. Energy band diagram of an SiC MOS system in inversion and location (qualitative) of different types of charges.

interface by developing more effective processes to passivate defects at the interface formed during the oxidation process. These defects give rise to interface trap density, D_{IT} (cm^{-2} eV^{-1}) and is shown in **Figure 10**. Depending upon the surface potential, these traps can be charged positively or negatively charged.

As mentioned previously, these traps decrease the effective channel mobility of electrons significantly. At present, there is a standard passivation process based on post-oxidation annealing in nitric/nitrous oxide (NO/N_2O) for 2 h at 1175°C. [42, 43]. This post-oxidation annealing (passivations) increases the inversion electron channel mobility of an SiC-MOSFET from single digits, ~ 8 $cm^2V^{-1}\cdot s^{-1}$, to around 30 $cm^2/V\cdot s$. Although these processes have made the commercialization of SiC MOSFETs possible, there is still room for significant improvement. This inversion channel mobility value is only around 4% of bulk mobility value of SiC. In case

of Si, the inversion channel mobility can be as much as 50% of bulk mobility [29]. In addition to standard N_2O annealing, there are different types of annealing which can increase the channel mobility significantly, but these annealings degrade some important parameters of a MOSFET and hence cannot be used [44–50]. More work is still needed in this field to improve the performance of SiC MOSFETs.

3.2. Ohmic contacts

In SiC, there is no or very little diffusion as a result, it is not possible to use temperature annealing process to drive in the dopants into the material. To get a desired doping profile in SiC, dopants are implanted using a high-energy implanter (typically 50–500 keV), and sometimes, wafers are needed to be at high temperature (~500°C) during this step. Implantation of dopants is followed by a dopant activation step, which requires a very high temperature. Typically, n-dopants get electrically activated at 1550°C, while p-dopants require a temperature of as high as 1700°C, which is very challenging to achieve. With n-dopants, the electrical activation rate of more than 90% can be attained, but in p-dopants, it is tough to realize an activation rate of more than 50%. The reason why lower activation temperature is required for n-dopants as compared to p-dopants is because of the difference in the location of respective dopant energy levels in SiC. For n dopants (N), the donor energy level is located at 0.3 eV (shallow) below the conduction band edge and hence not much energy is required to electrically activate these donors. In the case of p dopants (Al), the position of the acceptor level is 0.7 eV (deep) above the valance band edge. Hence, more energy is needed to electrically activate them. Even at present, various research groups are working on p-type ohmic contacts [51–56]. Also, high temperature and special metallization processes are necessary to form ohmic and Schottky contacts on SiC.

4. EMI problems

Due to fast switching speed of SiC devices (Schottky diodes, MOSFETs), some undesirable effects are observed during the switching (from on-state to off-state and vice versa) of these devices. The oscillations observed in the output current waveform, **Figure 11**, are the result of the fast switching behavior of 1.7 kV, 50 A SiC diodes, which are used to build 3.3 kV, 1200 A hybrid SiC modules. From the application point of view, this is problematic and can lead to EMI with neighboring electrical systems. Sometimes, it can also lead to a premature breakdown of the module during operation. In full SiC module, it is common measure to slow the switching speed of the devices (by increasing the gate resistance) to reduce/eliminate the oscillations. From **Figure 11**, we can clearly see that the oscillations are present, both in current and in voltage waveforms. Also, these oscillations are present in the gate signal, which is used to control Si IGBT (clear from the inset in **Figure 11**) in the module. Because of these oscillations, the gate signal voltage in some cases may shoot up/down to +40 to −40 V, much higher than the recommended voltage range (−15 to +15 V) of the gate signal. We can imagine how detrimental this would be for Si IGBTs. If new design ideas are used for the substrate layout of these modules, then the parasitic elements (stray inductance and capacitance) could be minimized, and, hence, there will be no necessity of compromising on the switching speed of SiC devices.

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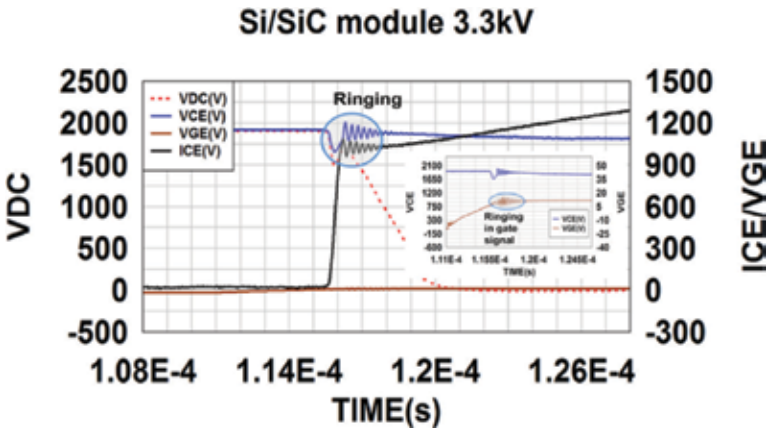

Figure 11. The ringing/oscillations observed in the output waveforms of a 3.3 kV, 1200A SiC hybrid module due to an underdamped response to an RLC circuit formed among the diode depletion capacitance, parasitic inductance, and SiC diode during the second turn-on event.

5. Conclusions

SiC device technology has a promising future. Different types of more efficient power systems have already been built using SiC devices and demonstrated in real applications around the world. This technology materializes the possibility of new topologies for inverter and converter, which were not possible in the past. Various fields including automotive, traction-train, renewable energy, geothermal energy, and so on have already been benefitted from SiC technology. Despite all these advantages, this technology is relatively new and hence poses some challenges. New control strategies, and more suitable module designs and packaging options are needed to be developed for the optimal use of these devices. The cost of SiC device is still a bit high, although, in the past couple of years, it has come down significantly. Even with all these challenges, new technology like SiC is indispensable to achieve the goal of a greener planet.

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Chapter 2

TCAD Device Modelling and Simulation of Wide Bandgap Power Semiconductors

Neophytos Lophitis, Anastasios Arvanitopoulos, Samuel Perkins and Marina Antoniou

Additional information is available at the end of the chapter

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Abstract

Technology computer-aided Design (TCAD) is essential for devices technology development, including wide bandgap power semiconductors. However, most TCAD tools were originally developed for silicon and their performance and accuracy for wide bandgap semiconductors is contentious. This chapter will deal with TCAD device modelling of wide bandgap power semiconductors. In particular, modelling and simulating 3C- and 4H-Silicon Carbide (SiC), Gallium Nitride (GaN) and Diamond devices are examined. The challenges associated with modelling the material and device physics are analyzed in detail. It also includes convergence issues and accuracy of predicted performance. Modelling and simulating defects, traps and the effect of these traps on the characteristics are also discussed.

Keywords: TCAD, modelling and simulation, silicon carbide, gallium nitride, diamond, physics modelling, material parameters

1. Introduction

1.1. Materials and devices

Power devices made from wide bandgap materials have superior performance compared to those made from silicon. They can sustain higher voltages or endure smaller losses, they can operate at much higher junction temperatures and can switch faster. This is because, as seen in **Figure 1**, of their superior electrical properties. This in turn can revolutionize how applications work and possibly make new applications possible. The most mature materials in terms of process and device technology are the 4H-SiC and GaN-based devices. There is however, an

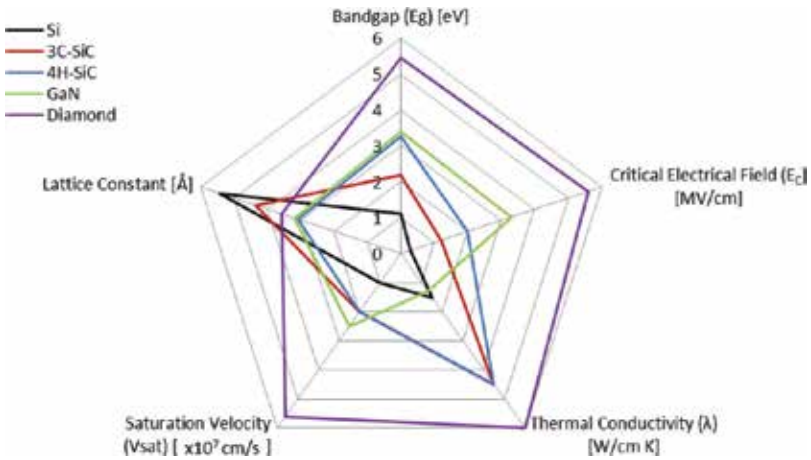

Figure 1. Material properties of significant power semiconductors normalized against Si, data taken form [1, 2].

increased interest and effort in advancing 3C-SiC and overcoming the technical challenges associated with the development of good-quality 3C-SiC wafers because of lower processing costs and the possibility for high channel mobility MOSFETs. Ultra-wide bandgap materials such as diamond are also being explored.

Silicon carbide is similar to silicon in terms of device design and optimization strategies. Most devices made in silicon can also be made in SiC. This includes Schottky Barrier Diodes, MOSFETs, IGBTs, and Thyristors. However, devices made in GaN are hetero devices and base their operation on the two-dimensional electron gas (2DEG) that is formed in the quantum well between the heterojunction interfaces. This quantum well provides electrons with a highly conductive channel, allowing high electron mobility. It is reported in literature that the electron mobility in GaN HEMT devices can be upwards of 1500 cm^2/Vs [3].

1.2. Technology computer-aided design

TCAD is an engineering computer-aided tool which enables the physics-based modelling of semiconductor devices and their fabrication process. Due to the excellent predicting capability, semiconductor process and device engineers use TCAD for virtual prototyping and optimization of devices, to reduce the number of experimental cycles and, therefore, to reduce the production cost. TCAD can also be used to study the performance of devices when used in new applications or environments, to find performance limits and to analyze failures [4, 5]. Modern TCAD suites are compiled by several tools. A typical example of a TCAD suite is diagrammatically described in **Figure 2** and it consists of the following elements:

- **Device design tool**

The device design tool allows the rapid creation of device structures via the use of scripting language or a graphical user interface without the need to know the process recipe. At this

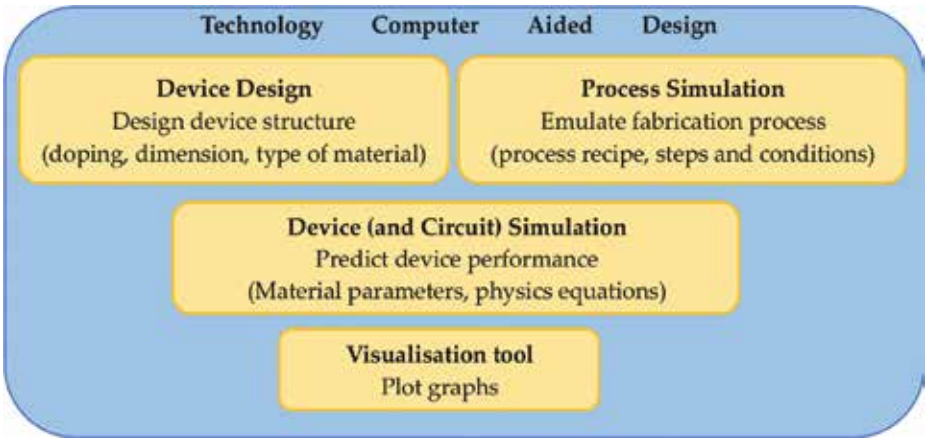

Figure 2. Exemplary combination of tools making up a typical TCAD suite framework.

stage, the device geometry, the material and doping profile, and concentration of regions is defined. Commercial tools include Synopsys Sentaurus Structure Editor [6] and SilvacoDevEdit™ [7]. These tools allow device designers to parameterize device aspects and features to optimize their design or to assess the performance dependence on the parameters of question.

- **Process simulation tool**

The process simulation tools allow for the virtual fabrication of devices and the emulation of fabrication steps and conditions. They typically make use of a scripting language and require knowledge of a process recipe. These tools allow process engineers to fine tune their recipe and to analyze the effect of each process step and condition on the resulting device structure. Commercial tools include Synopsys Sentaurus Sentaurus Process [8] and Silvaco Athena [9].

- **Device (and circuit) simulation tool**

Device simulation tools have the capability to simulate the electrical, thermal, and optical properties and performance of devices. They can also account for the circuitry that surrounds a device when used in real applications. Therefore, they typically have SPICE capabilities too. They predict the device performance by executing finite element analysis and the solution of fundamental semiconductor physics equations. They make use of numerical devices created either through a device design tool or a process simulation tool. They take into consideration the materials incorporated in the device and they have a database with physics equations and the equivalent material parameters. Commercial tools include Synopsys Sentaurus Device [10] and Silvaco Atlas [11].

1.3. Summary

This chapter aims to highlight issues and present solutions and methods for achieving accurate models of WBG power devices. This includes proper modelling the material physics equations

and their parameters, creating the finite elements and geometry and simulation of device characteristics including numerical issues and the effect of traps.

2. Material physics modelling

TCAD tools solve fundamental semiconductor physics equations to predict the performance of semiconductor devices. Accurately modelling the material properties through appropriate physics equations and parameters is essential for reliable simulations. These can depend on how advanced and mature the process, growth and technology is. For silicon, the material properties have been studied extensively and the technology is mature. Therefore, the material models and their parameters are typically considered accurate and able to predict the silicon-based devices performance with high level of accuracy. However, for WBG semiconductor-based devices, a lower confidence level exists. In the following subsections, we discuss the physics equations and the parameter sets required for accurate physical modelling of 3C-SiC, 4H-SiC, GaN and diamond power semiconductors. The equations used and parameters are compatible with most TCAD products.

2.1. Silicon carbide

There are hundreds of Silicon Carbide polytypes. From those, 4H-SiC is the most mature and studied polytype. The cubic polytype, 3C-SiC is also of particular interest because of its special properties, such as the ability to grow this compound semiconductor on large area silicon wafers, the lower temperatures required when processing the material and the ability to make MOSFETs with much higher channel mobility. The former two results in a much cheaper starting wafer whereas the latter one can enable the development of devices with higher efficiency. The corresponding values required in a physics parameter file for 4H-SiC were developed and improved alongside the improvement of the technology. Recently there have been efforts to compile an equivalent set of parameters for 3C and to validate them [12, 13]. This section presents the required models and the parameters of both materials. Wherever necessary, a range of values is used. Further, each physical mechanism presented is accompanied with the corresponding identified limitations. SiC polytypes can experience anisotropic properties, therefore when aiming multidimensional device simulation, these must be accounted for in the material parameter file and physics equations [14]. 4H-SiC experiences such behaviour, whilst 3C-SiC experiences isotropic behaviour. The parameters are then included within the 'Device (and Circuit) Simulation' tool of TCAD tools.

2.1.1. Band parameters

The desired properties of the WBG SiC originate from its bandgap characteristics. The value of E_g shall not be considered constant, but variable with dependencies on both the concentration of impurities and temperature as shown in **Figures 3** and **4** correspondingly. Increasing the temperature of the material essentially leads to lower gap values as described by Eq. (1). In

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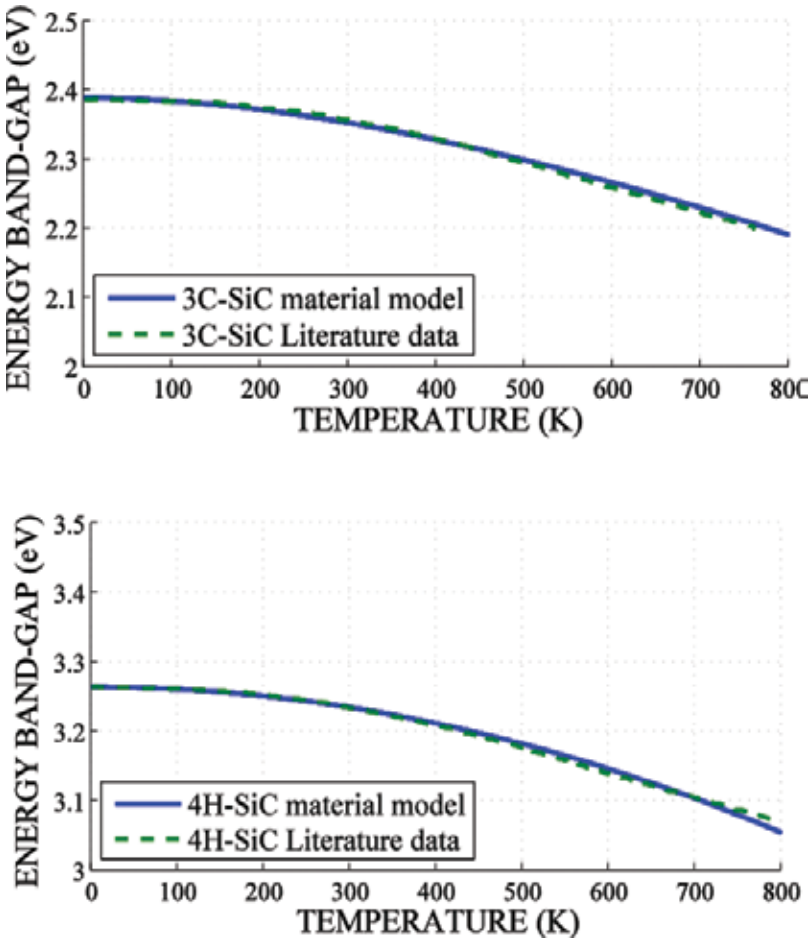

Figure 3. The 3C-SiC (top) and 4H-SiC (bottom) bandgap dependence on temperature as described with the models given in this chapter are in excellent agreement to literature data [15] for both β-SiC and α-SiC, respectively.

addition, the phenomenon of bandgap narrowing causes band displacements in the energy scale directly related to doping according to Eq. (2), (3). These displacements represent potential barriers that may influence carrier transportation phenomena in the device. The bandgap dependence on doping in SiC can be described as in Eq. (4). The perception of the modeled effective bandgap value for the SiC can be expressed as $E_{g,eff}(T) = E_g(T) - E_{bgn}$ utilizing the parameters shown in **Tables 1–3**.

$$E_g(T) = E_g(0) - \alpha T^2/(T+\beta) \tag{1}$$

$$E_{bgn}^{cond} = \begin{cases} A_n \cdot N_{tot}^{1/3} + C_n \cdot N_{tot}^{1/2}, & N_{D,0} > N_{A,0} \\ B_p \cdot N_{tot}^{1/4} + D_p \cdot N_{tot}^{1/2}, & otherwise \end{cases} \tag{2}$$

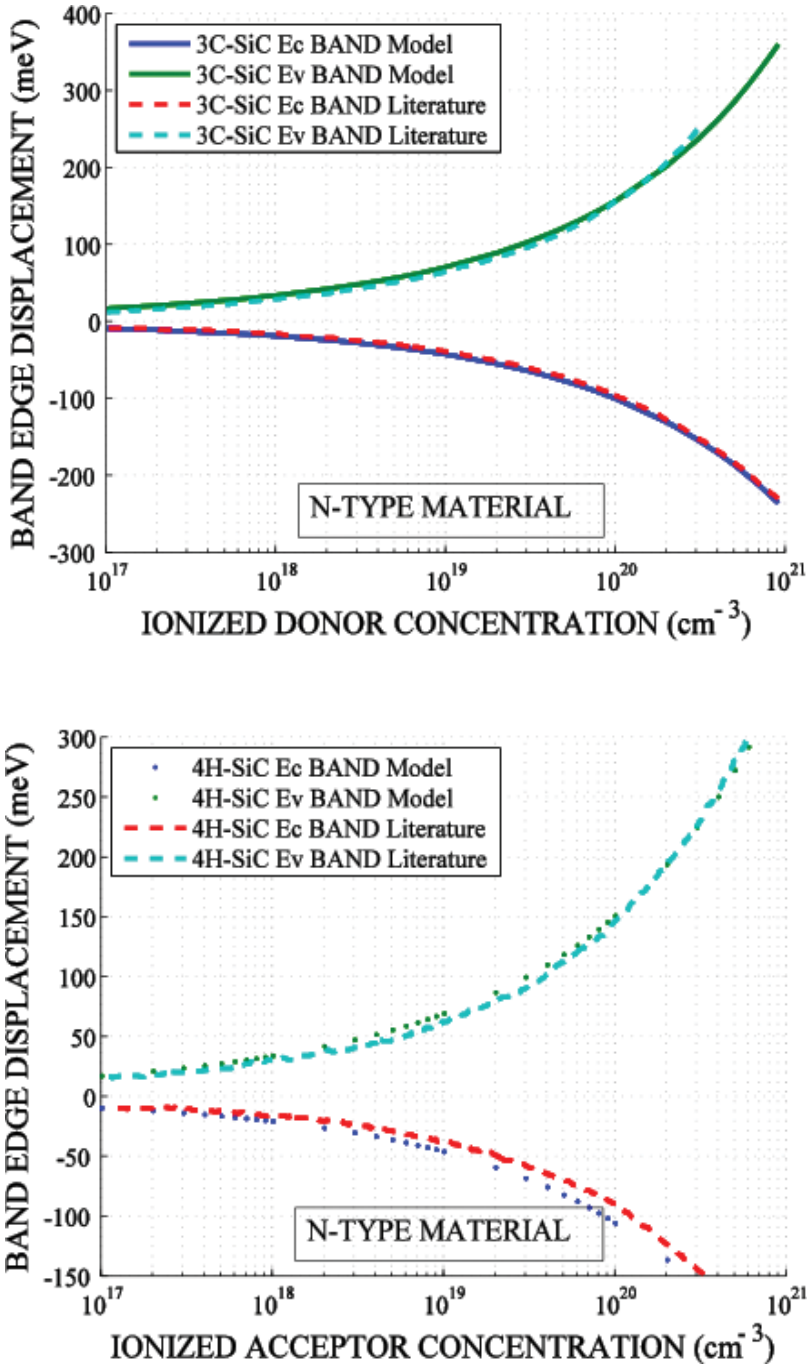

Figure 4. The bandgap narrowing phenomenon as modeled for TCAD simulations assuming n-type SiC material. The measured energy displacements of the bands are sourced from [16].

Parameters description	3C-SiC	4H-SiC
$E_g(0)$ [eV]	2.39	3.265
α [eV/K]	0.66×10^{-3}	3.3×10^{-2}
β [K]	1335	1.0×10^{5}

Table 1. SiC parameter set related to bandgap.

Lindefelt model coefficients	3C-SiC semiconductor material	
	n-type	p-type
$A_{n,p}$ [eV·cm]	-1.48×10^{-8}	1.3×10^{-8}
$B_{n,p}$ [eV·cm$^{3/4}$]	9.0×10^{-7}	-4.8×10^{-7}
$C_{n,p}$ [eV·cm$^{3/2}$]	-3.06×10^{-12}	1.43×10^{-12}
$D_{n,p}$ [eV·cm$^{3/2}$]	6.85×10^{-12}	-6.41×10^{-13}

Table 2. 3C-SiC band gap narrowing doping dependence.

Lindefelt model coefficients	4H-SiC semiconductor material	
	n-type	p-type
$A_{n,p}$ [eV·cm]	-1.791×10^{-8}	3.507×10^{-8}
$B_{n,p}$ [eV·cm$^{3/4}$]	8.927×10^{-7}	-2.312×10^{-6}
$C_{n,p}$ [eV·cm$^{3/2}$]	-2.2×10^{-12}	6.74×10^{-12}
$D_{n,p}$ [eV·cm$^{3/2}$]	6.24×10^{-12}	-1.07×10^{-12}

Table 3. 4H-SiC bandgap narrowing doping dependence.

Parameters description	3C-SiC	4H-SiC
N_C (300 K) [cm^{-3}]	1.5536×10^{19}	1.719×10^{19}
N_V (300 K) [cm^{-3}]	1.1639×10^{19}	2.509×10^{19}

Table 4. SiC temperature dependent density of states.

$$E_{bgn}^{val} = \begin{cases} B_n \cdot N_{tot}^{1/4} + D_n \cdot N_{tot}^{1/2}, & N_{D,0} > N_{A,0} \\ A_p \cdot N_{tot}^{1/3} + C_p \cdot N_{tot}^{1/2}, & otherwise \end{cases} \tag{3}$$

$$\Delta E_g^0 = -E_{bgn}^{cond} + E_{bgn}^{val} \tag{4}$$

To model the intrinsic characteristics of the semiconductor, the temperature dependence of the density of states (DoS) for SiC in Eq. (5) is used. The parameters of **Table 4** determine the

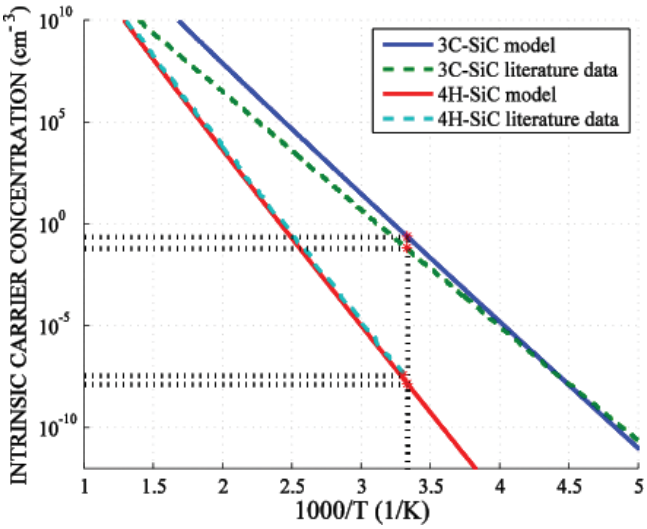

Figure 5. The intrinsic carrier concentration as resulting from the model of DoS for both SiC cases in question. Comparison with literature data for 3C-SiC [18] and 4H-SiC [16] is performed. Assuming low doping levels (5×10^{15} cm^{-3}) the bandgap narrowing is considered negligible.

intrinsic carrier concentration of the semiconductor as well as quantities like the effective carrier masses. In **Figure 5**, plotting the intrinsic carrier concentration against the temperature a discrepancy with measurements can be noticed for the case of 3C-SiC. This suggests that the TCAD simulations of 3C-SiC power devices utilizing this model should yield reasonably good results for limited temperature range of 200–500 K.

Under low field conditions, the mobility of both types of carriers in SiC also depends on the doping concentration and on temperature. The first dependence is described by the Caughey-Thomas (C-T) model $\mu_0 = \mu_{min} + (\mu_{max} - \mu_{min})/(1 + (N/N_{ref})^{\alpha})$ as illustrated in **Figure 6**. Each coefficient in the C-T equation changes with temperature as in Eq. (6) and the values in **Table 6**. Currently, there is an uncertainty for the holes' mobility actual value in 3C-SiC. However, the values adopted in **Table 5** are suggested from recent measurements [16, 17]. The mobility of carriers for the temperature range of 250–700 K was described in [12]. In high field conditions, with magnitude of values as shown in **Figure 7**, the mobility and velocity of carriers become inseparable directly affecting each other. The Canali model, Eq. (7) is utilized for these purposes and its parameters for SiC are presented in **Table 7**. In Eq. (8), the holes' saturation velocity determines the range of electric field values at 200 kV/cm < E < 2000 kV/cm [12].

$$N_{C,V}(T) = N_{C,V}300 \times (T/300)^{3/2} \tag{5}$$

$$Par = Par_0 \times (T/300K)^{\gamma} \tag{6}$$

$$\mu_0(E) = \frac{(\alpha+1)\mu_{low}}{\alpha + \left[1 + \left(\frac{(\alpha+1)\mu_{low}E}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{7}$$

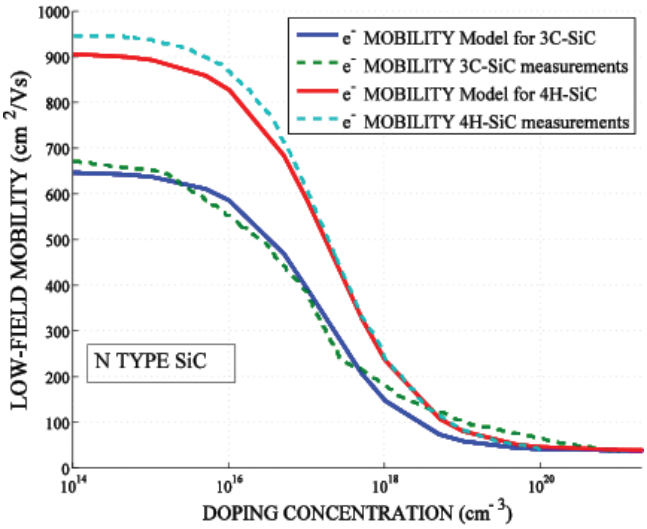

Figure 6. Based on experimental data [19], the SiC models utilized result in a very good accuracy. Increased the doping concentration, more scattering occurs and the mobility drops. The maximum carrier mobility values in SiC range and depend on crystal thickness [20] and impurities level.

Parameter	3C-SiC		4H-SiC [perpendicular to c-axis]		4H-SiC [parallel to c-axis]	
	Electrons	Holes	Electrons	Holes	Electrons	Holes
μ_{max} [cm^2/Vs]	650	70	910	114	1100	114
μ_{min} [cm^2/Vs]	40	15	40	0	40	0
N_{ref} [cm^{-3}]	1.5×10^{17}	5×10^{19}	2.0×10^{17}	2.4×10^{18}	2.0×10^{17}	2.4×10^{18}
α	0.8	0.3	0.76	0.69	0.76	0.69

Table 5. SiC parameters for low field mobility and coefficients used to express doping dependence.

Parameter	3C-SiC		4H-SiC [same for both directions]		Corresponding parameter from Table 5
	Electrons	Holes	Electrons	Holes	
γ_{max}	−0.3	−2.5	−2.4	−2.6	μ_{max} [cm^2/Vs]
γ_{min}	−0.5	−0.5	−1.536	−0.57	μ_{min} [cm^2/Vs]
γ_{Nref}	2	0	0.75	2.9	N_{ref} [cm^{-3}]
γ_{α}	0	0	0.722	−0.2	α

Table 6. SiC parameters for low field mobility and coefficients used to express temperature dependence.

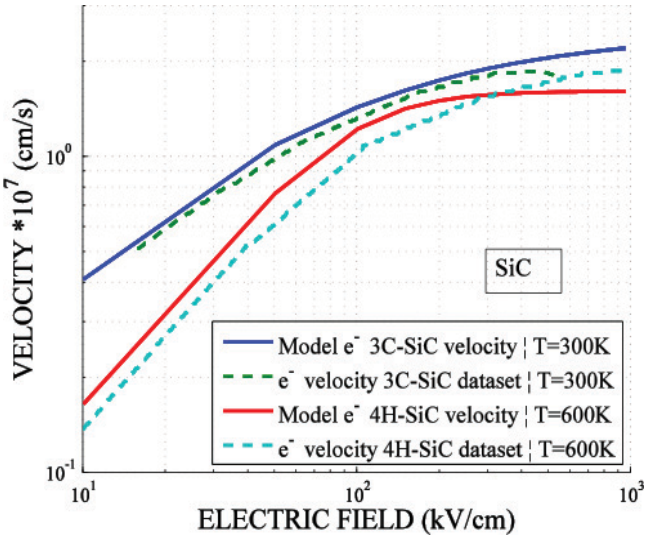

Figure 7. The models for SiC electrons' velocity allow accurate TCAD simulations for temperatures up to 600 K. Comparison with literature data for 3C-SiC [21] and 4H-SiC [19] is performed. A doping level of 5×10^{15} cm^{-3} is assumed.

Parameter	3C-SiC		4H-SiC		
	Electrons	Holes	Electrons [⊥ to c-axis]	Electrons [// to c-axis]	Holes
beta (β_0)	0.75	2.5	1.2	1.2	1.2
γ_{beta}	−0.9	0	1.0	1.0	1.0
alpha (α)	0	0	0	0	0
$v_{sat,0}$ [cm/sec]	2.5×10^7	1.63×10^7	2.2×10^7	1.9×10^7	2.2×10^7
$v_{sat,exp}$	−0.65	1.55	0.44	0.44	0.44

Table 7. SiC parameters for high field mobility and saturation velocity along with coefficients used to express temperature dependence.

$$v_{sat} = v_{sat,0}\left(\frac{300K}{T}\right)^{v_{sat,\exp}} \tag{8}$$

2.1.2. Doping and incomplete ionization

Compared to silicon, dopants in wide bandgap semiconductors have larger ionization energies, making activation of the doping species an issue. The dopant impurities are better modeled as traps to account for the phenomenon of incomplete ionization. As shown in **Table 8**, the formed energy levels depend on the polytype and the impurity. To model this behaviour, Eqs. (9) and (10) are utilized, where $N_{A,D}$ is the doping concentration, $N_{A,D'}$ is the effective doping concentration, $E_{A,D}$ and E_f are the activation energy, and the Fermi level, respectively, G_A is the degeneracy factor, and N_{crit} is the value that determines where the

Impurity	Species type	Energy levels [eV]	
		3C-SiC	4H-SiC
Nitrogen (N)	Donor[a]	0.057	0.071
Vanadium (V)	Donor[a]	0.660	0.800
Aluminium (Al)	Acceptor[b]	0.260	0.265
Gallium (Ga)	Acceptor[b]	0.343	0.300
Boron (B)	Acceptor[b]	0.735	0.293

[a]The formed energy level is considered from the conduction band (E_C).
[b]The formed energy level is considered from the valence band (E_V).

Table 8. SiC impurities/shallow traps due to doping.

metallic-type conduction mechanism starts [22]. The degeneracy factor temperature dependence can be expressed by Eq. (11), whilst the typical values for g_A is 4 and for g_D is 2 for the impurity levels of acceptors and donors in SiC, respectively [23]:

$$N_{A,D'} = N_{A,D}/\left(1 + G_A * \left(E_{A,D} - E_f\right)/kT\right) \qquad N_{A,D} < N_{crit} \tag{9}$$

$$N_{A,D'} = N_{A,D} \qquad N_{A,D} \geq N_{crit} \tag{10}$$

$$G_{A,D}(T) = g_{A,D} \cdot \exp\left(\frac{\Delta E_{A,D}}{kT}\right) \tag{11}$$

2.1.3. Impact ionization

The impact ionization coefficients of electrons and holes need to be determined to specify the breakdown voltage [24]. For 3C-SiC, the Chynoweth law $\alpha(E_{ava}) = \gamma \cdot \alpha \cdot \exp(-\gamma b/E_{ava})$ can be adopted. The parameter values are determined in **Table 9**, following the work of van Overstraeten-de Man [25]. The temperature dependence of these parameters is expressed by determining the optical phonon energy as indicated by $\gamma = \tanh(\hbar\omega_{op}/2kT_0)/\tanh(\hbar\omega_{op}/2kT)$.

Parameters description	Parameter name	3C-SiC		4H-SiC [⊥ to c-axis]		4H-SiC [// to c-axis]	
		Electrons	Holes	Electrons	Holes	Electrons	Holes
Ionization coefficients for electrons and holes	$a_{n,p}$ [cm^{-1}]	1.28×10^6	1.07×10^7	1.76×10^8	3.41×10^8	2.1×10^7	2.96×10^7
	$b_{n,p}$ [V/cm]	5.54×10^6	1.12×10^7	3.3×10^7	2.5×10^7	1.7×10^7	1.6×10^7
Low field range up to this value	E_0 [V/cm]	4.0×10^5	4.0×10^5	—	—	—	—
Optical phonon energy	$\hbar\omega_{op}$ [eV]	0.120	0.120	0.190	0.190	0.190	0.190

Table 9. SiC impact ionization coefficients for $T_0 = 300\ K$

Notably, it has been found in [26] that these values are relatively insensitive to temperature variations in the range of 300 K < T < 500 K. For 4H-SiC, a slightly different model is utilized after Hatakeyama's work [27] to effectively describe the anisotropic behaviour of the avalanche coefficients. The avalanche force is considered to have two components to account for the anisotropic structure of 4H-SiC [28], satisfying $F^2 = F_{//}^2 + F_{\perp}^2$. Utilizing the projections of these electric field components, the avalanche coefficients can be computed as indicated in Eqs. (12)–(15), with the default value of $\theta = 1$:

$$a = a_{\perp}^{\left(\frac{B \cdot F_{\perp}}{b_{\perp} \cdot F}\right)^2} \cdot a_{//}^{\left(\frac{B \cdot F_{//}}{b_{//} \cdot F}\right)^2} \tag{12}$$

$$b = B\sqrt{1 - \theta A^2 \left(\frac{BF_{\perp}F_{//}}{Fb_{\perp}b_{//}}\right)^2} \tag{13}$$

$$A = \log \frac{a_{//}}{a_{\perp}} \tag{14}$$

$$B = \frac{F}{\sqrt{\left(\frac{F_{\perp}}{b_{\perp}}\right)^2 + \left(\frac{F_{//}}{b_{//}}\right)^2}} \tag{15}$$

2.1.4. Generation-recombination

The doping dependence of the SRH lifetime is modeled with Scharfetter in Eq. (16). The band-to-band non-radiative recombination is expressed with the Auger recombination rates, $R_{net}^{A} = \left(C_n n + C_p p\right)\left(np - n_{i,eff}^2\right)$. As shown in Eqs. (17) and (18), the effect of temperature and doping is accounted for. Typical values for the Scharfetter and Auger models are shown in **Tables 10** and **11**. However, since these are heavily process dependent, they need to be adjusted every time the process conditions change:

Parameter	**SiC**	
	Electrons	**Holes**
τ_{min} [sec]	0	0
τ_{max} [sec]	2.5×10^{-6}	0.5×10^{-6}
N_{ref} [cm^{-3}]	1×10^{17}	1×10^{17}
γ	0.3	0.3
T_{α}	1.72	1.72
T_{coef}	2.55	2.55
E_{trap} [eV]	0	0

Table 10. SiC SRH lifetime parameter set.

Parameter	3C-SiC		4H-SiC	
	Electrons	Holes	Electrons	Holes
A [cm^6/sec]	0.3×10^{-31}	0.2×10^{-31}	6.7×10^{-32}	7.2×10^{-32}
B [cm^6/sec]	0	0	2.45×10^{-31}	4.5×10^{-33}
C [cm^6/sec]	0	0	-2.2×10^{-32}	2.63×10^{-32}
H	1.9	1.9	3.47	8.26
N_0 [cm^{-3}]	1.0×10^{19}		1.0×10^{18}	
T_0 [K]	300	300	300	300

Table 11. SiC Auger recombination rates.

$$\tau_{dop} = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_{A,0}+N_{D,0}}{N_{ref}}\right)^{\gamma}} \tag{16}$$

$$C_n(T,n) = \left(A_n + B_n\left(\frac{T}{T_0}\right) + C_n\left(\frac{T}{T_0}\right)^2\right)\left[1 + H_n \exp\left(-\frac{n}{N0,n}\right)\right] \tag{17}$$

$$C_p(T,p) = \left(A_p + B_p\left(\frac{T}{T_0}\right) + C_p\left(\frac{T}{T_0}\right)^2\right)\left[1 + H_p \exp\left(-\frac{p}{N0,p}\right)\right] \tag{18}$$

2.2. Gallium nitride

GaN-based devices utilize GaN, AlGaN and AlN materials. AlGaN is a molar fraction of AlN and GaN. GaN and AlGaN naturally form Wurtzite crystal structures with the ability of forming different Ga and N faces. For this chapter, only the Ga-face is considered. In TCAD, it is necessary to define the material properties of AlN and GaN separately. AlGaN material properties are thereafter approximated through a linear interpolation, depending on the molar fraction of AlN and GaN. A more accurate result can be yielded wherever the molar compounds are known and experimental evaluation of their properties has been performed. In those cases, new material parameters can be made which would reflect the exact molar compound of interest, which in turn would give more accurate simulations.

Similar to modelling SiC, the important parameters include modelling the bandgap, doping and incomplete ionization, impact ionization, mobility and generation-recombination.

2.2.1. Band parameters

Like all III-Nitride semiconductors, GaN and AlN are direct bandgap semiconductors, that is, the maximum valley in their valance band is directly below the minimum conduction valley. Similar to SiC examined earlier, E_g cannot be assumed constant in value and will vary heavily with temperature and doping concentration. Again, like SiC, thermally exciting GaN leads to lower band gap energies. According to Eq. (1) the variation of bandgap value can be described utilizing the parameters in **Table 12** [29].

Parameters description	GaN	AlN
$E_g(0)$ [eV]	3.507	6.23
α [eV/K]	9.1×10^{-4}	1.79×10^{-3}
β [K]	836	1.462×10^{3}

Table 12. *GaN/AlN* parameter set related to bandgap.

Further, utilizing Eq. (19), the intrinsic carrier concentration of the GaN material can be calculated. This premises that the DoS and/or the effective carrier masses in this WBG material are known. Equations (20) and (21) adequately describe this temperature dependent procedure. The intrinsic characteristics of GaN can then be given by [30]:

$$n_i = (N_c \cdot N_v)^{1/2} \exp\left(-E_g/(2k_B T)\right) \tag{19}$$

$$N_c\tilde{} = 4.82\ \ 10^{15} \cdot (m_\Gamma/m_0)^{3/2} T^{3/2}\ \left(cm^{-3}\right)\tilde{} = 4.3 \times 10^{14} \times T^{3/2}\ \left(cm^{-3}\right) \tag{20}$$

$$N_v = 8.9 \times 10^{15} \times T^{3/2}\ \left(cm^{-3}\right) \tag{21}$$

2.2.2. Mobility

The low field carriers' mobility for the bulk WBG compound depends on the carriers' density following the C-T formula, as illustrated in SiC physical model. However, variations of this model exist to fit better some compound semiconductors behaviour. In SiC above, the so-called Arora model is utilized originating from the C-T model. It provides additional control on the temperature dependence of SiC low field mobility parameters. For GaN and AlN, the Masetti

Parameter	GaN		AlN	
	Electrons	Holes	Electrons	Holes
μ_{const} [cm^2/Vs]	1500 [31] – 1800 [29]	20	300	14
$\gamma_{\mu_{max}}$	1	2.1	1	2.1
μ_{min1} [cm^2/Vs]	85	33	20	11
μ_{min2} [cm^2/Vs]	75	0	65	0
μ_1 [cm^2/Vs]	50	20	20	10
P_c [cm^{-3}]	6.5×10^{15}	5×10^{15}	8×10^{17}	5×10^{18}
C_r [cm^{-3}]	9.5×10^{16}	8×10^{16}	7×10^{16}	8×10^{17}
C_s [cm^{-3}]	7.2×10^{19}	8×10^{20}	5.2×10^{17}	8×10^{18}
α	0.55	0.55	0.88	1.05
β	0.75	0.7	0.75	0.75

Table 13. Coefficients used for temperature and doping (Masetti model) dependency of low field mobility in GaN and AlN.

Parameter	GaN		AlN	
	Electrons	Holes	Electrons	Holes
beta (β_0)	7.2044	4	17.3681	4
γ_{beta}	6.1973	0	8.7253	0
alpha (α)	0.7857	0	0.8554	0
$v_{sat,0}$ [cm/sec]	1.3×10^7	1.7×10^7	1.5×10^7	1.25×10^7
$v_{sat,exp}$	0.7	0.725	2	2

Table 14. *GaN*/*AlN* parameters for high field mobility and saturation velocity along with coefficients used to express temperature dependence.

model, in Eq. (22), is preferred to describe the doping dependence, with the fitting parameters shown in **Table 13**. In this table, $\gamma_{\mu_{max}}$ indicates the coefficient for the temperature dependency of the maximum mobility parameter, as described by Eq. (6). This is the only temperature dependent parameter that the Masetti model accounts for:

$$\mu_{dop} = \mu_{\min 1}\exp\left(\frac{P_c}{N_{A,0}+N_{D,0}}\right) + \frac{\mu_{const}-\mu_{\min 2}}{1+\left(\frac{N_{A,0}+\ N_{D,0}}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1+\left(\frac{C_s}{N_{A,0}+N_{D,0}}\right)^{\beta}} \tag{22}$$

The calculated mobility in low field conditions is utilized in the Canali model, as discussed in SiC section with Eq. (7). The parameter values presented in **Table 14** enable modelling the mobility in high field conditions while taking into consideration the temperature dependence with Eq. (6).

2.2.3. Doping and incomplete ionization

Dopants in this WBG semiconductor would not fully ionize even at high temperatures [32] because the impurities form deep levels, as further observed in **Table 15** [33–38]. The models as presented in Eqs. (9)–(11) can be utilized here following the same degeneracy factor values for the conduction and valence bands [39]. That is, g_A equals 4 for shallow acceptors and g_D equals 2 for shallow donors.

2.2.4. Impact ionization

The Van Overstraetan-de Man expression, described in SiC section, with the parameters in **Table 16** can be used to model the impact ionization phenomenon [29]. It is worth noticing that for the case of high electric fields (i.e. larger than the E_0 value) the impact ionization coefficients are predicted to be similar in GaN [40].

2.2.5. Generation-recombination

The non-radiative recombination [41], SRH, is described by the Scharfetter model in Eq. (15) is considered a dominant process in the bulk. **Table 17** includes the relevant parameter values. Auger recombination process is realized utilizing Eqs. (17)–(18) along with the coefficient

Impurity	Species type	Energy levels [eV]			
		GaN		AlN	
		Ga	N	Al	N
Silicon (Si)	Donor[a]	0.017	—	—	—
Nitrogen (N)	Donor[a]	—	—	1.4–1.85	—
Vacancy (V_N)	Donor[a]	—	0.03–0.1	—	0.17
Carbon (C)	Donor[a]	0.11–0.14	—	0.2	—
Magnesium (Mg)	Donor[a]	—	0.26, 0.6	—	—
Vacancy (V_{GA})	Acceptor[b]	0.14	—	—	—
Silicon (Si)	Acceptor[b]	0.19	—	—	—
Magnesium (Mg)	Acceptor[b]	—	0.14–0.21	0.1	—
Zinc (Zn)	Acceptor[b]	0.21–0.34	—	0.2	—
Mercury (Hg)	Acceptor[b]	0.41	—	—	—
Cadmium (Cd)	Acceptor[b]	0.55	—	—	—
Beryllium (Be)	Acceptor[b]	0.7	—	—	—
Lithium (Li)	Acceptor[b]	0.75	—	—	—
Carbon (C)	Acceptor[b]	—	0.89	—	0.4
Gallium (Ga)	Acceptor[b]	—	0.59–1.09	—	—
Aluminium (Al)	Donor[a]	—	—	—	3.4–4.5
Vacancy (V_{Al})	Acceptor[b]	—	—	0.5	—

[a]The formed energy level is considered from the Conduction band (E_C)
[b]The formed energy level is considered from the Valence band (E_V)

Table 15. Impurities and shallow traps due to doping in *GaN*/*AlN*

Parameters description	Parameter name	GaN		AlN	
		Electrons	Holes	Electrons	Holes
Ionization coefficients for electrons and holes	$a_{n,p}$ [cm^{-1}]	1.5×10^5	6.4×10^5	2.9×10^8	1.34×10^7
	$b_{n,p}$ [V/cm]	1.41×10^7	1.46×10^7	3.4×10^8	2.03×10^8
Low field range up to this value	E_0 [V/cm]	4.0×10^5	4.0×10^5	4.0×10^5	4.0×10^5
Optical phonon energy	$\hbar\omega_{op}$ [eV]	0.035	0.035	0.035	0.035

Table 16. *GaN*/*AlN* impact ionization coefficients for $T_0 = 300\ K$

values shown in **Table 18** [42]. Auger recombination in nitrides is responsible for the loss of quantum efficiency in InGaN-based light emitters [43]. This non-radiative loss mechanism is due to the large values of the Auger coefficients (2×10^{-30} cm^6/s) for specific parts of the emission spectrum, like blue to green region.

Parameter	GaN		AlN	
	Electrons	Holes	Electrons	Holes
τ_{min} [sec]	0	0	0	0
τ_{max} [sec]	0.7×10^{-11}	2.0×10^{-11}	1.0×10^{-9}	
N_{ref} [cm^{-3}]	1×10^{16}			
γ	1	1	1	1
T_{α}	−1.5	−1.5	−1.5	−1.5
T_{coef}	2.5	2.5	2.5	2.5

Table 17. GaN/AlN SRH lifetime parameter set.

Parameter	GaN	
	Electrons	Holes
A [cm^6/sec]	3.0×10^{-31}	3.0×10^{-31}
B [cm^6/sec]	0	0
C [cm^6/sec]	0	0
H	0	0
N_0 [cm^{-3}]	1.0×10^{18}	1.0×10^{18}
T_0 [K]	300	300

Table 18. GaN Auger recombination rates.

2.3. Diamond

Diamond (C) is considered to be a strong contester for high power due to its outstanding electrical and thermal material properties [44]. However, the realization of power semiconductor devices based on this material is extremely difficult and such devices are currently at the research level. The main reason is that there are not enough activated carriers at room temperature, leading to poor device performance. Furthermore, diamond is also extremely expensive to fabricate due to large scale material growth constrains.

It is worth mentioning that since diamond is at very early stages of development, it is also at very early stage at the material characterization and modelling. Currently, diamond does not exist in the material libraries of the commercial TCAD simulation packages. As a result, all material properties and fitting parameters of various materials interface with diamond need to be added manually.

2.3.1. Band parameters

The experimentally extracted value of diamond bandgap (Eg) is about 5.47 eV at room temperature [45]. This value directly translated into high material critical electric strength. High

breakdown field strength means that the material can withstand high potential drops across very thin layers thus minimizing the on-state resistance of the device allowing for the fabrication of highly energy efficient high voltage high current devices.

The values for the density of states for the valence and the conduction band (Nv,Nc) are given by expressions Eq. (5) where in this case $N_v300 = 1.8e19$ and $N_c300 = 5e18$ [cm^{-3}], as reported in [22, 44–47]. Therefore, the appropriate levels of density of state could be calculated using Eq. (19). For CVD diamond this value is around 1.2×10^{-27} cm^{-3} [22] at 300 K, Eg is the bandgap, T is the absolute temperature in Kelvin and k the Boltzmann constant (1.38×10^{-23} J/K). This value is extremely small for any meaningful numerical analysis using TCAD simulations. Therefore, possible strategies to facilitate and match experimental results include adding a fitting coefficient/value for intrinsic concentration, activating the constant carrier generation models or including trap levels and recombination centres in the materials bandwidth [22].

2.3.2. Doping and incomplete ionization

Diamond doping either of n-type or p-type to a less extent is challenging; in order to develop accurate and reliable simulation models one has to include the incomplete ionization models with the appropriate coefficients. It is therefore necessary to use the 'incomplete ionization model' [48] (**Figure 8**). The equations implemented follow the model described in Eqs. (9) and (10). Note that the degeneracy factor in this particular case is a function of temperature, given by the model in Eq. (23):

$$g_{A,D} = 4 + 2\exp\left(-\Delta g_{A,D}/(kT)\right) \tag{23}$$

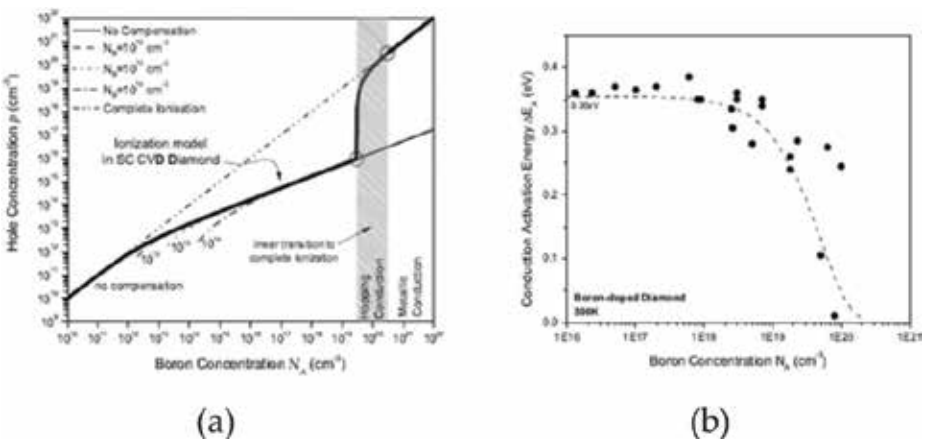

Figure 8. (a) Incomplete ionization model implemented for boron in single crystal diamond and (b) variation of activation energy with doping concentration of boron [22].

Ionization coefficients for electrons and holes	a_n (cm^{-1})	a_p (cm^{-1})	b_n (Vcm^{-1})	b_p (Vcm^{-1})
Diamond [22]	1.89×10^5	5.48×10^6	1.7×10^7	1.42×10^7

Table 19. Avalanche coefficients for diamond.

2.3.3. Mobility

For an intrinsic diamond, the hole mobility is up to 3800 $cm^2/(Vs)$ whereas for boron-doped diamond the mobility is dominated by the concentration dependent scattering. At elevated temperatures, above 325 K it has been shown that the mobility is decreased due to acoustic phonon scattering [48, 49]. The combination of p+ doped diamond leads to lattice scattering. It therefore is advisable that these complex relationships between mobility, doping and temperature are taken into consideration when diamond simulations are implemented. A fairly accurate model, the unified mobility model (UniBo) [50] accounts for the dependence of the mobility on the doping and on the temperature using with a single model.

2.3.4. Impact ionization

Impact ionization integral coefficients for electron and holes are very important in the design of diamond devices with the appropriate values been included in the impact ionization models parameters. Under reverse bias conditions, the increase of the ionization integral towards unity indicates the increase in the generation of avalanche carriers due to impact ionization, leading eventually to the device breakdown. The avalanche coefficients are given by Eq. (24) where in which $a_{n,p}$, $b_{n,p}$ and $c_{n,p}$ are fitting parameters and E is the lateral electric field through the semiconductor layer. The numerical values for both diamond and silicon are given in **Table 19**:

$$A = a_{n,p}\exp\left(-b_{n,p}/E\right)c_{n,p} \tag{24}$$

3. Device modelling and simulation

Due to the very low intrinsic carrier concentration of WBG semiconductors, the expected leakage current is very low ($\sim 10^{-20} Acm^{-2}$), which causes converge issues. To alleviate from this, the numerical precision should be significantly high. This is achieved with the inclusion of certain keywords in the 'Device (and Circuit) Simulation' tool command file (e.g. 'Extended-Precision' for SDevice tool of the Synopsys Sentaurus TCAD). Simulations that use extended arithmetic precision are computational more intensive, therefore, the arithmetic precision should be increased in a trade-off manner up to a level that is able to provide a solution.

A further method utilized to improve convergence issues, especially when simulating the blocking characteristics, is to add extra carriers' generation through an equivalent keyword in the command file. The latter can increase the leakage current to levels that are high enough (e.g. $> 10^{-10} Acm^{-2}$) for the simulations to converge at lower precision level. This

method not only helps the simulations convergence but it also helps with accounting the realistic leakage currents in WBG devices, which are orders of magnitudes higher than the predicted ideal ones. The reason for the much higher real leakage currents is attributed to the immaturity of the technology, the high defects and traps density and due to background irradiation. Their effect on the leakage current is therefore, considered with this constant carrier generation statement.

The choice of solvers is also important when simulating WBG devices. Some linear solvers will be more suited for small to medium 2D simulations and others for medium to large 3D simulations due to their superior parallel performance and significantly smaller memory usage. In addition, relaxing the numerical setting for the linear solver constitutes another trade-off which may improve the operation of the solver, however, convergence complications may come as a cost.

3.1. Silicon carbide

For accurate simulation results, modelling the defects and traps is imperative. They directly influence the performance and strongly affect its reliability [51]. To highlight the effect of traps on the device performance and electrical characteristics, the P-i-N rectifier structure of **Figure 9** was prepared for modelling and simulation. A Gaussian energetic distribution of deep levels is considered distributed spatially uniformly.

For most applications, the linear region of the forward I-V characteristics is important [14], the sub-threshold characteristics, however, are indicators of the material quality [53]. Both regions of the device characteristics are affected by the presence of traps. **Figure 10** depicts the effect of the traps capture cross section, whereas **Figure 11** depicts the effect of the concentration of deep level traps on the sub-threshold current-voltage (IV) forward characteristics. Because

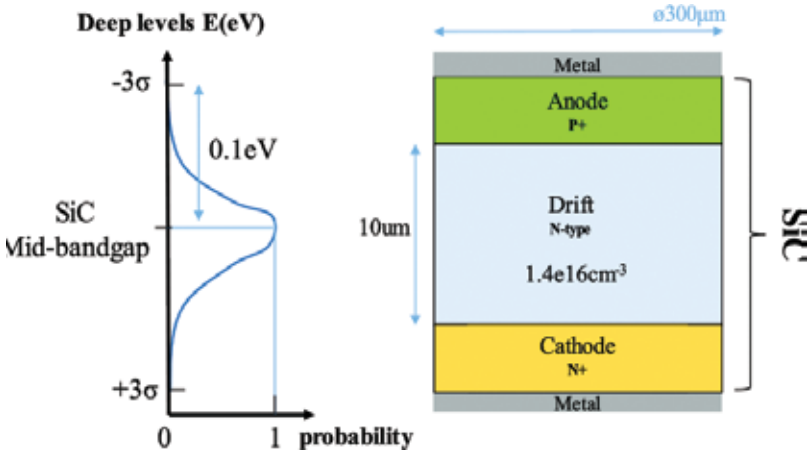

Figure 9. Simplified device schematic used for simulations of a SiC P-i-N power rectifier following the fabricated diode in [52]. The Gaussian energetic distribution of the deep levels considered is also illustrated.

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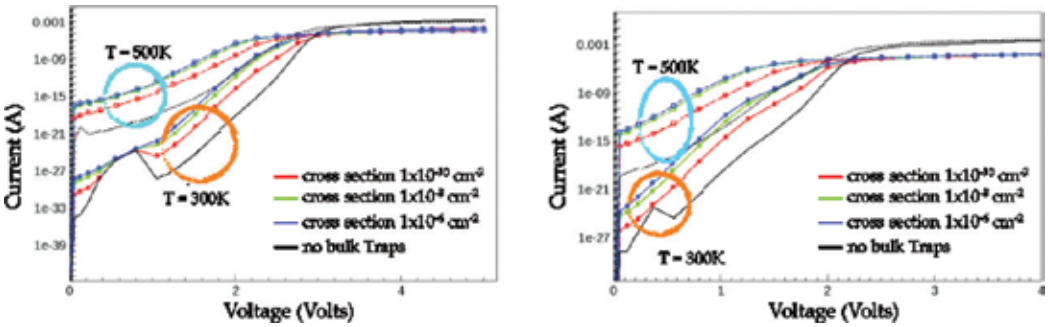

Figure 10. Sub-threshold region of a SiC P-i-N structure with 10 um drift region at 1.4e16 cm^{-3}. The defects concentration is fixed with a variable cross section value. The simulated 4H-SiC material contains donor traps (left), whereas the 3C-SiC contains acceptor traps (right).

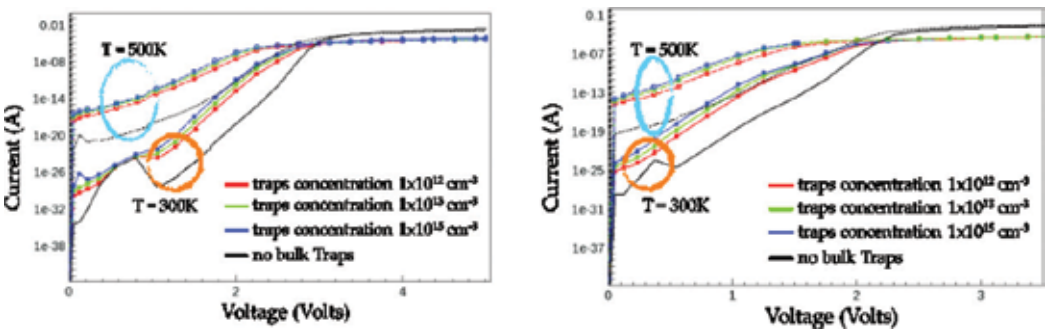

Figure 11. Sub-threshold region of a SiC P-i-N structure with 10 um drift region at 1.4e16 cm^{-3}. The defects' cross section is fixed with a variable concentration value. The simulated 4H-SiC material contains donor traps (left), whereas the 3C-SiC contains acceptor traps (right).

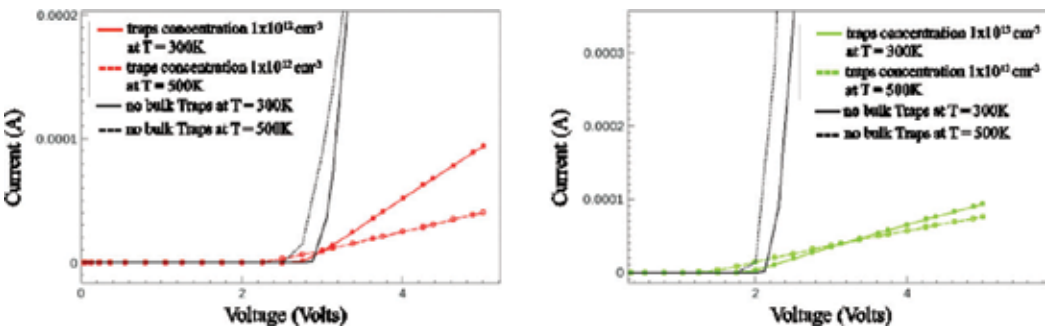

Figure 12. The impact of carriers' scattering lowers with increased temperature. This behaviour is independent of the type and the concentration of the deep level as can be seen for the 4H-SiC (left) and the 3C-SiC (right) case.

generation-recombination is the main carrier transport mechanism in the sub-threshold region, an increased concentration of deep levels or a larger capture-cross-section results in a higher magnitude for leakage current [14].

The forward the linear region is governed by the recombination-generation and the drift-diffusion. In this case, the defects have an opposite effect on the IV characteristics. An increased concentration of the traps intensifies carriers scattering, thus effectively reducing the mobility of carriers, which in turn leads to a decreased conductivity. This behaviour is less significant at elevated temperatures as the carriers gain enough kinetic energy to remain unaffected from the presence of nearby defects in the bulk. Consequently, the on-resistance of the material can decrease, as illustrated in **Figure 12**.

Traps also need to be included when modelling the interfaces between SiC and other materials. The traps' energetic profile at or near the interface in those cases need to be identified and modeled appropriately. For SiC Schottky interfaces, the combined effect of tunnelling and traps is modeled with the quantum tunnelling and trap-assisted tunnelling models [54]. The effect of traps also needs to be modeled at the SiC/SiO2 interface, in particular when modelling SiC MOSFETs [55].

3.2. Gallium nitride

The GaN High Electron Mobility Transistor (HEMT) is regarded as the most successful attempt at harnessing the superior material properties of Gallium Nitride. The AlGaN HEMT is a heterostructure formed through the union of $Al_XGa_{1-X}N$ and GaN. The inherent spontaneous and mechanically induced piezoelectric polarization charges a dictate the formation of a 2D Electron Gas across the heterojunction interface [56]. It is worth noting that the 2DEG channel is inherently present across the device and therefore, means that the device is naturally on. This has caused engineers to develop normally off GaN HEMT one being the p-type Gate GaN HEMT device. This device contains a p-typed GaN region beneath the gate which depletes the 2DEG of carriers and therefore, effectively stops the channel underneath the gate. In this section, device modelling will focus upon this device. The complexities associated with modelling GaN HEMT devices in TCAD are summarized below [57]:

- Reduced crystal symmetry compared to silicon due to the Wurtzite crystal structure.
- The polarization charges and subsequent effects on the device performance.
- The lower intrinsic carrier concentration associated with wide bandgaps semiconductors.
- The exchange of the inter-valley at high field that modulates the current through the Gunn effect.
- The abrupt nature of the heterojunction between the semiconductors and partially floating regions.
- The significant and extensive quantity of traps and their subsequent characteristics.

The forward operation of the GaN HEMT device is dependent on the characteristics of the 2DEG channel. There are multiple methods that can be employed to model the 2DEG channel. The first is the placement of an interface charge across the AlGaN/GaN interface. The second is a simplified strain model in which the TCAD calculates the polarization charges based on the material which calculates the spontaneous and piezoelectric charges through the molar

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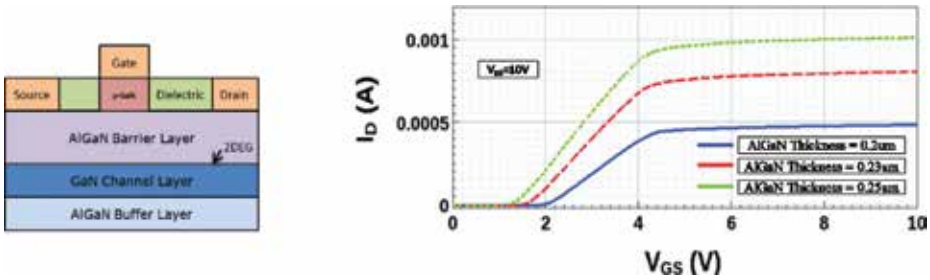

Figure 13. Simplified schematic representation of the simulated HEMT device (left) and its simulated transfer characteristics for 0.20, 0.23 and 0.25 μm AlGaN barrier layers (right).

fraction of the AlGaN layer and the corresponding strain based on the GaN layer. Another technique is applying a full strain model which calculates the polarization charges and are expressed through the local strain tensor. Finally, a stress model can be applied which calculates the polarization charges and are expressed in the local stress tensor.

TCAD simulations with the simplified strain model utilized, describe how the threshold voltage changes with the thickness of AlGaN. This behaviour is in accordance to Eq. (25) [58] where; V_{th} is threshold voltage, Φ_B is the height of the Schottky barrier, E_C is the conduction band offset, d is the thickness of the AlGaN barrier, N_D is the 2DEG concentration and ε is the relative dielectric constant of AlGaN. To increase the threshold voltage of the GaN HEMT, three parameters can be changed, the work function of the Schottky contact, the aluminium mole concentration in the AlGaN and the thickness of the AlGaN region. In this model, we have chosen to decrease the thickness of the AlGaN barrier whilst maintaining the same parameters for the rest of the device. **Figure 13** depicts the simplified equivalent schematic representation of the simulated device and the transfer characteristics for three different AlGaN thicknesses of 0.20, 0.23 and 25 μm. As shown, the threshold of the device varies even with a very small change in the AlGaN thickness. This also demonstrates how sensitive the 2DEG is to the process. For that reason, a fixed interface charge across the AlGaN/GaN interface, is many times the preferred modelling approach, the concentration of which can be used as a fitting parameter:

$$V_{th} = \Phi_B - \frac{\Delta E_C}{q} - \iint_d \frac{qN_D(x)}{\varepsilon} dx^2 \tag{25}$$

4. Conclusions

Adequate modelling and simulation of WBG power devices and their performance with TCAD presents challenges and complexities. It includes modelling the material physical properties, improving the numerical accuracy of simulations, taking special care for the device structure design and incorporating the effect of defects, often in the form of traps. It also includes understanding the complexities and trade-offs between convergence and simulation

speed, and how these are affected by the choice of solvers and numerical accuracy. This chapter gave an overview of those for 3C-SiC, 4H-SiC, GaN and diamond-based devices.

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Chapter 3

Main Differences in Processing Si and SiC Devices

Fan Li and Mike Jennings

Additional information is available at the end of the chapter

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Abstract

Due to the different physical properties of Si and SiC, many conventional Si device processing techniques cannot be directly transferred to SiC device fabrication. To deliver high-performance SiC commercial power devices, new techniques quite different from Si industry were developed in past decades for processing device, such as dopant implantation, metal contact, MOS interface, etc. On the other hand, the physics model behind many of these SiC processing technologies is not updated in the same pace that the success of them can still not be fully understood.

Keywords: SiC processing, dopant implantation, metal contact, MOS interface, physics model

1. Introduction

Silicon has dominated the electronics industry ever since it was born. In power electronics area, nearly all commercial power devices are made of Si nowadays. However, due to the target of a more environmental friendly society, there has been a continuously increasing demand of power devices working in more harsh conditions such as higher power, higher temperature, higher frequency or even higher radiation, some of which are well beyond the physical limits of Si. For the first time, the position of Si is challenged by some other materials, most of which have a larger band gap than Si, thus called wide band gap (WBG) semiconductors, including silicon carbide (SiC), gallium nitride (GaN) and diamond. SiC may be the most promising candidate at the moment, whose technology is most mature among WBG semiconductors with commercial devices readily on the market [1, 2], and most importantly, SiC is the only WBG semiconductor with SiO_2 as the nature oxide, which is used extensively in power devices as insulators, dielectrics and diffusion barriers [3]. Just as the SiC substrate and epilayer

growth technologies which had gone through decades of developments before power device quality level wafers can be delivered, SiC device processing techniques were improved as well at the same time. It has been studied intensively in last 20 years, and although there is still plenty of room to be improved, commercial power MOSFETs and Schottky diodes with some more conventional structures are not an issue anymore. This chapter will talk about the state-of-the-art processing techniques for SiC devices, including intentional doping, electrical activation, metal/semiconductor interfaces and MOS interface. Particularity, the difference between Si and SiC processing in these areas will be discussed.

2. Intentional doping in SiC

In 1930, Bernhard Gudden [4] was the first one to report that the electrical carriers of semiconductors are actually the impurities within their crystal lattices. If the impurity concentration is too high, the semiconductor becomes metallic, and if too low, more like an insulator.

2.1. Thermal diffusion and ion implantation

Impurities are usually introduced to the bulk semiconductor in early stages of a device fabrication process. Most commonly used dopants are from group V (N, P and As) for n-type and group III (B, Al and Ga) for p-type doping purposes. Doping a bulk semiconductor can be relative easily achieved by adding dopant elements into the epilayer growing process, and the impurity level can be modulated by controlling the precursor gas concentrations [5]. Take a typical vertical MOSFET structure as an example; on the epilayer surface, specific n-type and p-type regions are required to form ohmic contact, MOS channel and body diode. The selective doping area is usually defined by doping masks made of dielectrics or metals using standard photolithography processes. Nowadays the selective doping of semiconductor is achieved mostly in two ways, namely, thermal diffusion and ion implantation.

It is well known that molecules tend to move from higher to lower concentration regions, and this process can be enhanced by increasing the ambient temperature, pressure or concentration gradient in-between. This idea is adopted in semiconductor industry to introduce impurities using dopant sources with various phases: gas, liquid or solid. Thermal diffusion-based doping process often occurs in a quarts tube (see **Figure 1**) in an inert gas atmosphere to minimise contaminations. The dopants firstly arrived at the semiconductor surface form a relative high impurity concentration region; consequently, a concentration gradient exists between the surface and bulk, after which the diffusion is initiated by the thermal energy provided. With time going on, dopants diffuse deeper into the semiconductor bulk, and when the desired doping profile is obtained, it can be stopped quite conveniently by simply cutting the heat supply.

Attributed to the developments of experimental physics, ion implanting dopants directly into semiconductors are also an option now. Ion implanters were not widely available to device engineers until the 1970s [6], while now it is commonly used in both lab and industry processing. In an ion implantation system, dopants are ionised atoms generated from an ion source

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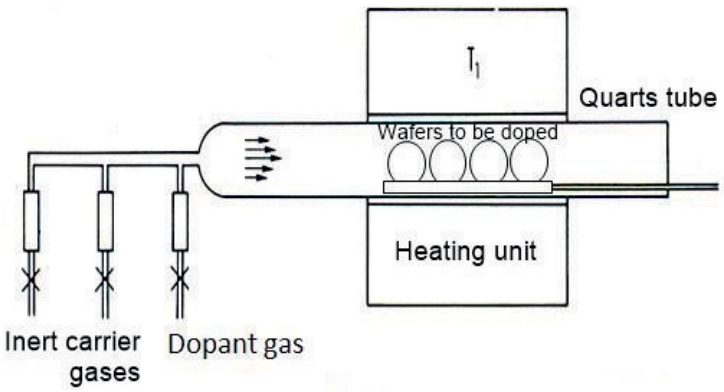

Figure 1. Schematic graph showing a typical dopant thermal diffusion process using a gas source.

shown in **Figure 2**. Being ionised, the dopant atoms can be accelerated by electromagnetic field to gain energy so high that, when hitting the target surface, they are able to break the semiconductor chemical bonds and penetrate into the crystal lattices. The implantation depth can be controlled by changing the electromagnetic field strength, and the resultant impurity concentration (cm^{-3}) is determined by the amount of dopants supplied by the source, which is called 'dose', and the unit is number per specific area (cm^{-2}).

In Si device processing, both thermal diffusion and ion implantation can be used depending on specific requirements. In fact, implantation followed by a short time thermal diffusion is becoming popular nowadays. For WBG semiconductors such as SiC, however, diffusion coefficients of common dopants are so low that are negligible below 1800°C [8], which leaves ion implantation the only option, and the PIA process is essential.

Even being a more complex and expensive system, ion implantation proved to be more controllable than thermal diffusion. Also, the movement of dopants in a thermal diffusion process may involve unexpected spreading in other directions, leading to poor doping profiles. This is not an issue for ion implantation since dopant movement in the semiconductor is minimal, which means the elimination of dopant out-diffusion. There are, of course, also limitations for ion implantations. First of all, it is essentially a dopant bombarding process, which means damages are inevitably induced to the target, mainly in the surface region. Secondly, as-implanted dopants are almost always interstitial (not chemically bonded), namely, not active carriers. An extra post-implantation annealing (PIA) process is typically required to recover the lattice damage and put the implanted dopants into substitutional positions so they can contribute to current conduction, called dopant activation.

2.2. Activating implanted dopants in SiC

The activation of dopants in 4H-SiC has been intensively studied, and the efforts are mainly put into two directions, namely, protecting the semiconductor surface morphology while at the same time maximising the active concentration of implanted dopants.

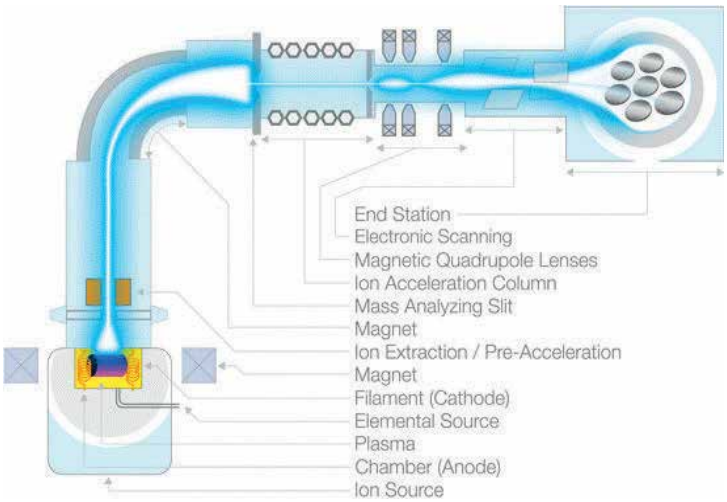

Figure 2. The schematic diagram of an ion implantation system [7].

The temperature required for SiC post-implantation activation (PIA) is very high that above 1400°C [9, 10] is common for n-type and even higher (>1600°C) for p-type [11–13] since acceptors generally sit deeper in the band gap than donors, namely, more difficult to activate. This high temperature means conventional quartz tubes are not up to the task and high melting point tubes made of Al_2O_3 and SiC or similar have to be used. Also, high-temperature annealing leads to a roughened semiconductor surface (known as 'step bunching'), enhanced at implanted regions. This can deteriorate the performance of interface features such as Schottky contacts and FET channels [14–16]. A protection capping layer is often used to preserve the SiC surface; such cap materials studied for 4H-SiC include AlN [17, 18], BN/AlN [19] and graphite [12, 15]. AlN and BN/AlN processes are found complex and expensive, thus not widely accepted. The graphite cap proved to be effective in preserving surface morphology up to 1800°C [11] but may reduce the MOSFET channel mobility due to the excessive silicon vacancies, which are most likely induced by the reaction between diffused Si atoms and the graphite [11, 20]. A SiO_2 layer should not react with Si or C at the common annealing temperatures and can be easily deposited by CVD method and removed via HF etching. It was also studied and resulted a similar surface roughness level as a graphite cap with the same annealing conditions [21]. In the few literatures on 3C-SiC, n-type implanted 3C-SiC was studied for different annealing conditions (1150–1400°C) with [22] and without [23, 24] a graphite cap, and it turned out that there was little advantage of using a graphite cap in terms of protecting the 3C-SiC surface, probably because the temperature limited by Si substrates is not high enough to make the difference.

For a given implanted doping level, the active dopant concentration in SiC generally increases with the PIA temperature. And for a fixed PIA temperature, the active dopant concentration increases with the implanted doping level [25], although the percentage of activated dopants (activation rate) seems to decrease [9]. Complete activation of N-type implanted 4H-SiC has been demonstrated by annealing at 1700°C and using phosphorous as dopant [26], while P-type material still remains a challenge [12].

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3. Ohmic contact on SiC

Most metals are known as highly electrical and thermal conductive attributed to their delocalised electrons, not to mention the convenient alloying process which helps to form reliable interactions for packaging. Consequently, they are the most widely used material for contact materials in semiconductor industry. Dating back to Braun's discovery in 1874 [27], the study of metal/semiconductor (M-S) interface is almost as old as the semiconductor device itself. A lot of huge efforts were put into exploring the M-S interface, and there had been classic physics models that were well developed. Yet still, this area remains active with new discoveries reported, and novel theories developed continuously. The emergence and adoption of WBG semiconductors raise discussions on new experimental results, and the well-established theories are challenged.

3.1. Metal contact interface: classic theory

It can be seen in **Figure 3** that the work functions of most metals used in electronic industry are quite big compared with Si affinity, that is, an inherent energy barrier exists between metal/Si interfaces, preventing free carrier exchange. And due to a much lower affinity value (except for 3C-SiC), this barrier is only getting higher at a metal/SiC interface, which also explains why Schottky behaviour is typically observed for as-deposited metal contacts on

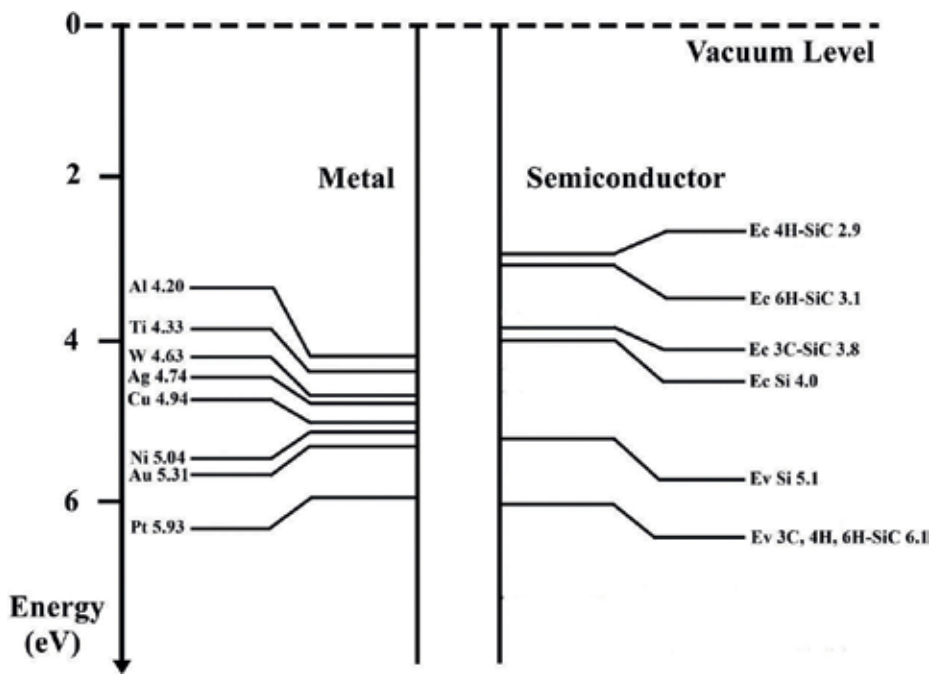

Figure 3. Band diagrams of Si, 3C-, 4H- and 6H-SiC and work functions of commonly used metals in electronic industry [28, 29].

4H-SiC. To fabricate an ohmic contact, increasing the contact region local doping level (via thermal diffusion or ion implantation) is the most common way for both Si and SiC. When the contact region is lowly doped, the depletion region is quite wide that the electron exchange at the M-S interface is only possible when electrons overcome the barrier by gaining enough energy as shown in **Figure 4**, usually thermally activated and thus called thermionic emission (TE). If doping level is very high, the depletion region becomes quite narrow, and electrons can tunnel through the barrier freely with the help of an external electric field, which is called field emission (FE). And if the doping value is in the middle, the depletion region is narrowed but not enough to enable electron tunnelling. In this case, electrons still need extra thermal energy to 'climb up' the barrier, but not as much as TE. The energy required just needs to be adequate for the electrons to 'climb' to a position shallow enough for tunnelling that begins to take effect. Since both TE and FE mechanisms are involved, this is therefore called as thermionic/field emission (TFE).

Among all, FE is the most desired conduction mechanism for deletion-type ohmic contact fabrication, since it is not a thermally activated process, namely, the electrical performance is relative temperature insensitive, which is attractive in more reliable device operation point of view. In real cases, both TFE and FE conduction are quite common. To predict the potential conduction mechanism at the SiC ohmic contact interface, the characteristic energy E_{00} of 3C-, 4H- and 6H-SiC as well as Si is calculated [30] for doping values from 1×10^{16} to 1×10^{20} cm^{-3} and plotted in **Figure 5**. Dielectric constants and electron conductivity effective mass are shown in **Table 1**. The specific boundaries between three mechanisms may vary a bit between groups; the one used in **Figure 5** is proposed by Schroder [31]. As can be seen, to enable FE tunnelling, a doping level above 1×10^{20} cm^{-3} is required for all semiconductors studied here.

Until now, the contact local doping level has been considered as a constant, which cannot be true for WBG materials. This is because with a wider band gap, dopants naturally sit in deeper energy levels and may not be thermally ionised at room temperature; it is called 'freeze-out' [33]. The partial ionisation of carriers leads to quite different ohmic contact performances from conventional theories. Field emission, for example, in which case the contact resistance used

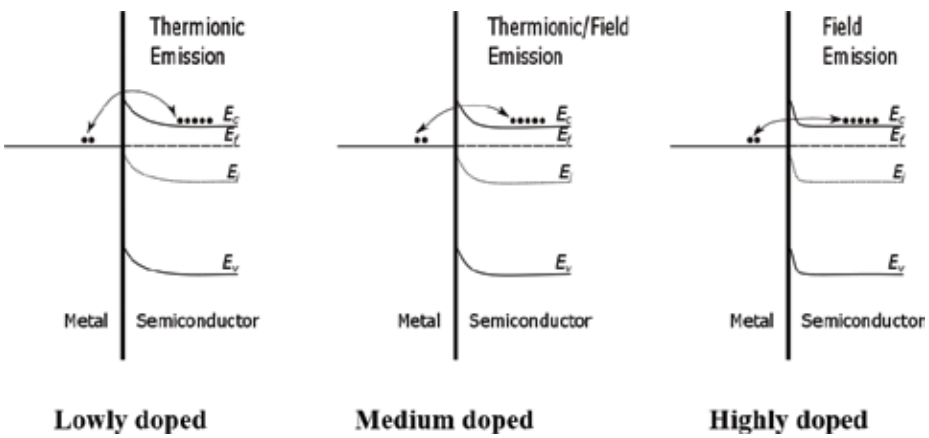

Figure 4. Metal-semiconductor (n-type) interface carrier conduction mechanisms for different doping levels.

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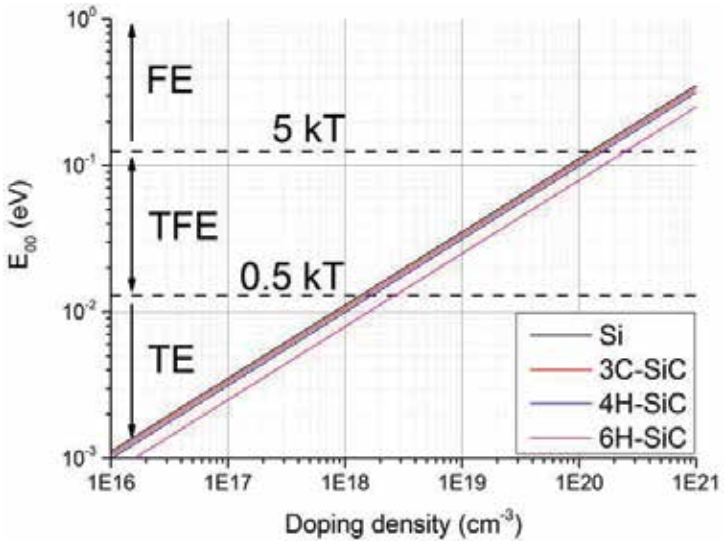

Figure 5. Characteristic energy E_{00} as a function of doping density for n-type Si, 3C-, 4H- and 6H-SiC.

Semiconductor	Dielectric constant	Electron conductivity effective mass
Si	11.7	0.26
3C-SiC	9.72	0.32
4H-SiC	9.66	0.36
6H-SiC	9.66	0.57

Table 1. Dielectric constants and electron conductivity effective mass of Si, 3C-, 4H- and 6H-SiC [32].

to be temperature independent, now will drop with elevating temperature. This is because with more dopants ionised, the contact local doping increases; thus, the depletion width is reduced [34], in favour of the field emission conduction. On the other hand, partial ionisation also means it is more difficult to achieve lower contact resistance at room temperature. To compensate this, after metal deposition on even very highly doped SiC films, extra annealing step (1000–1200°C) is usually required to form a homogeneous silicide or carbide layer at the contact interface, which further lowers the Schottky barrier height, leading to a lower contact resistance. For N-type ohmic contact, nickel-based alloys are typically used, and resultant silicides are Ni_2Si [35], while for P-type, Ti/Al alloys are common, leading to the formation of TiC or Ti_3SiC_2 [36] at the interface after the contact anneal. The complete story behind the rapid thermal anneal for SiC ohmic contact is still not clear; apart from the silicide reaction, which had been consistently observed and confirmed, local carbon clusters [37, 38] enriched at close to the contact interface, potentially providing more free carriers, were also often discussed and may have played a part, too. Specific contact resistance as low as 1×10^{-6} Ω cm^2 [9, 39] can be obtained on N-type SiC ohmic contact, and for the more difficult P-type due to deeper acceptor level, a higher value around 1×10^{-4} Ω cm^2 is typical [12, 36, 40].

4. SiC/SiO_2 MOS interface

Early MOSFETs have a long channel, leading to excessive on-state resistance which is not appropriate for power electronics, thus only applied in low power levels such as microprocessors, microcontrollers and logic circuits. On the other hand, the voltage-control and fast-switching features of MOSFETs are very attractive for power switch applications; consequently many efforts had been put into making power MOSFETs. The first high-voltage structure was developed in the 1970s and called V-MOSFET [41], named after the V-shape grove channel as seen in **Figure 6a**. This design never got popular due to the difficulty in fabricating a smooth V-shape trench on Si substrates, which was at that time formed by potassium hydroxide-based etching, whereas etching rate varies in different crystal orientations [42]. Also, the pointy trench bottom causes severe electric field crowding and easily leads to device early breakdown. Not long after, a planar structure shown in **Figure 6b** was invented. Instead of a V-shape grove, the channel was defined by controlling the thermal diffusion of dopants in the P-base and N^+ source regions, thus called vertical-diffused (VD) MOSFET. With main features relatively easy to fabricate and quite reliable, VD-MOSFET is the most successful design up to date. To achieve higher forward current density, the cell pitch of VD-MOSFET is usually made as small as possible. However, the narrow JFET region between two P-bases restricts the current flowing between channels and drift region, inducing extra on-resistance [43]. In the late 1980s, U-MOSFET design (**Figure 6c**) was proposed as a potential solution of getting rid of the JFET region. U-MOSFET is similar to the V-groove design in the sense that both of them use a trench to eliminate the JFET region, reducing the device on-resistance. By the time U-MOSFET was proposed, Si etching technology had been greatly improved that rounded trench corners are possible with reactive ion etching or other techniques [44]. However, the trench MOS interface and oxide reliability issues are not fully solved; consequently, U-MOSFETs still cannot compete with their planar counterparts.

All three power MOSFET designs introduced above have a vertical structure to maximise current handling ability of discrete devices. For vertical devices, the current rating can be increased by simply enlarging the device active area, such as bigger contacts for diodes or more parallel cells for MOSFETs. In some applications where power devices and control and logic circuits are integrated (e.g. smart power devices, power ICs), the processing and packaging may require all electrodes on the same side of the device, which makes a lateral design necessary, and this is where lateral diffused (LD) MOSFET fits in. As a modification from the long channel design, LDMOSFET usually has a much shorter channel length to minimise the on-resistance. Meanwhile, a long drift region is included for high-voltage purpose as seen in **Figure 6d**. Unlike vertical designs whose breakdown voltage is constrained by the drift region (epilayer) thickness, LDMOSFET utilises the semiconductor surface to greatly increase the device blocking voltage. Inevitably, the current conducting ability of LDMOSFET has to be greatly compromised. As a result, LDMOSFETs are mostly used for RF power amplifiers, microwave and medium power switching applications.

The adoption of WBG semiconductors enables MOSFETs to be used in power electronics applications with much higher power levels. While the Si/SiO_2 interface has been intensively

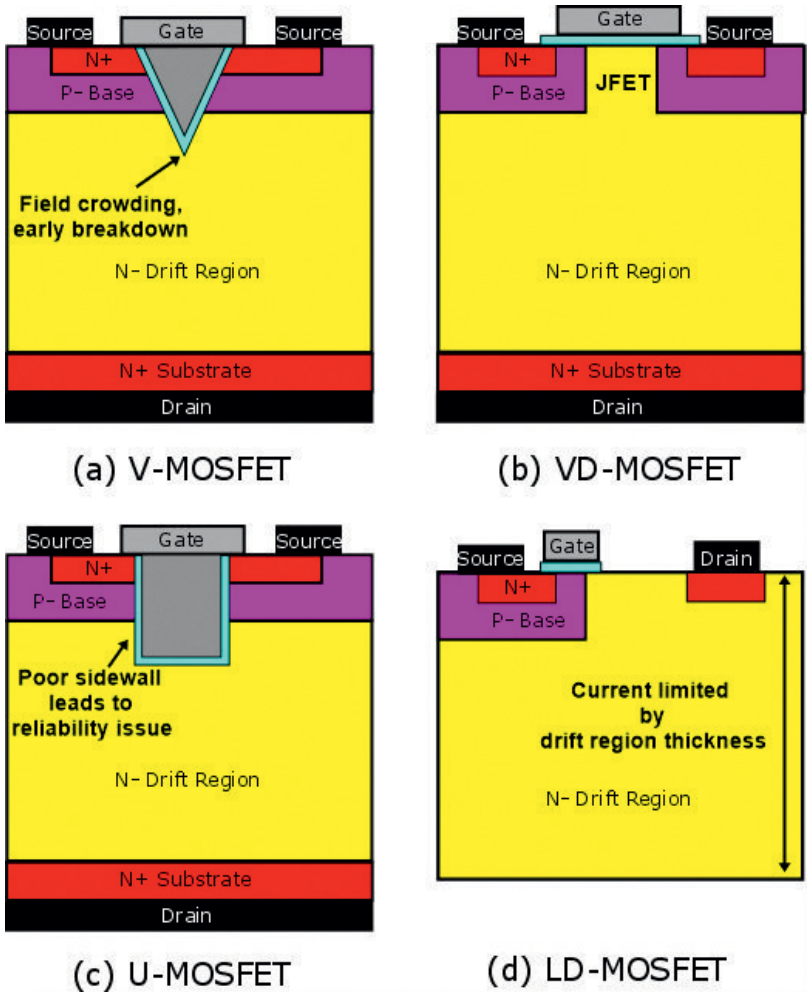

Figure 6. Schematic structure views of various MOSFET designs.

studied and the technology being very mature, the SiC/SiO_2 interface is still an active topic, revealing all kinds of possibilities and challenges.

4.1. Degradation of MOS channel mobility

Apart from phonon and coulombic which also troubles the bulk region, for channel region there is an extra surface roughness scattering mechanism. Among all, the Coulombic scattering caused by extra charges at the MOS interface is more process dependent and has been the target of studies. In real life, gate oxides are often with defects acting as carriers' leakage paths and cause early breakdown. By trapping and discharging carriers during the MOS device operation, these defects (also called states) are the main reason behind the severe Coulombic scattering. Extra charges found in most MOS systems are categorised into four groups, namely,

mobile charges, fixed charges, oxide-trapped charges and interface charges. A schematic graph indicating the general location and polarity of various charges are shown in **Figure 7**.

Mobile charges are metal ionic impurities (such as Na+) introduced during the device fabrication process and can move freely in the oxide with a gate bias. Since positively charged, they will attract semiconductor electrons to the surface and induce extra band bending, leading to a shift of flat band voltage. Mobile charges are highly uncontrollable and thus must be minimised through clean and careful fabrication process. In contrast to mobile charges, fixed charges refer to those who do not move with gate biases. The origin of fixed charges is believed to be the excessive ions left near the interface after the oxidation process termination [45]. They are usually located in the oxide and close to the MOS interface as shown in **Figure 7**. Fixed charges can be both positive and negative, and the total amount depends heavily on the oxidation condition. Since fixed charges stay close to the interface, they also affect the semiconductor band bending. As a result, a shift of flat band voltage from the theoretical value is again observed.

Interface charges, as the name suggests, sit at the MOS interface. Energy levels of these traps are in the semiconductor band gap; consequently, they can act as carrier traps communicating (charge/discharge) with the bulk semiconductor during device operation. And since these traps are right at the MOS interface, they scatter the channel carriers much more than other charges. The origins of interface traps vary among different MOS systems. For Si/SiO_2 interface, most of

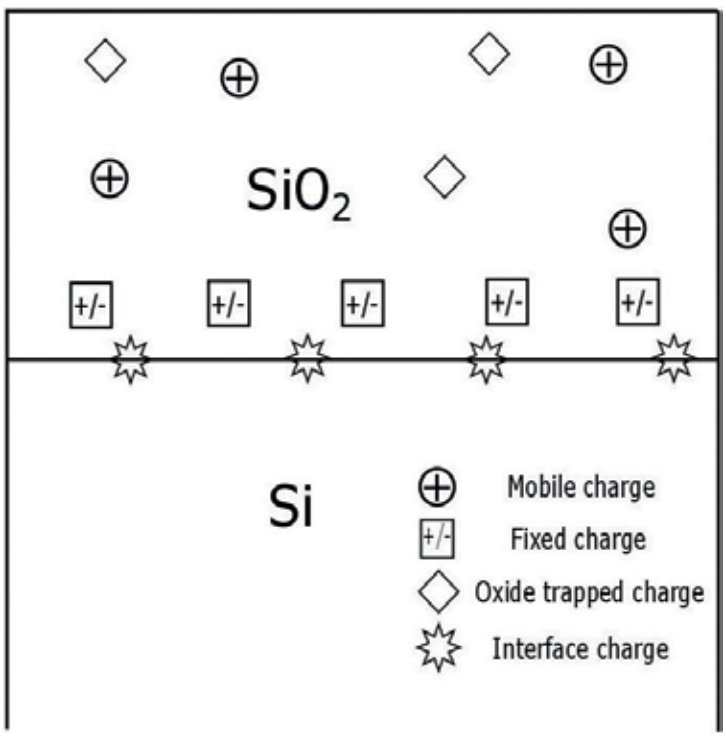

Figure 7. Common oxide charges at MOS interface with locations and charge polarity indicated.

the interface traps come from unterminated Si dangling bonds. H_2 annealing after the gate oxidation is typically applied to passivate the unterminated Si dangling bonds. Unlike the previous three, oxide-trapped charges are induced by the device operation rather than the fabrication process. The oxide layer, thermally grown or deposited, contains intrinsic defects such as oxygen vacancies [46]. Although these defects are electrically neutral, during the device operation, carriers may be injected into them and make them negatively or positively charged. Depending on the energy level, they may or may not be able to communicate with the semiconductor carriers. For those very close to the MOS interface that are able to be charged and discharged during device operation, they effectively behave as interface traps, otherwise similar to fixed charges.

4.2. SiC/SiO_2 interface traps

With all the superior electrical performance and the ability to be thermally oxidised, it is no surprise that there are a lot of interests in making SiC MOS devices. The most commercialised 4H-SiC is naturally mostly studied. The hexagonal lattice of 4H-SiC means there will be several faces available for oxidation. Most of the work has been devoted into the (0001) Si-face, the only one available in commercial wafer form. Following discussions are therefore mainly based on (0001) Si-face. There have been studies suggesting that MOS interface traps for all SiC polytypes are similar [47]; thus, the study on the 4H-SiC/SiO_2 interface also provides a great insight for other polytypes. Unfortunately, the 4H-SiC/SiO_2 interface turns out to be quite poor, and the electrical performance is not even close to the Si case. The interface trap density (D_{it}) at an as-grown 4H-SiC/SiO_2 interface is typically close to 10^{13} cm^{-2} eV^{-1}, which is hundreds of times higher than the Si/SiO_2 interface [48]. The channel mobility generally decreases with increasing D_{it}; thus, the latter is commonly used as an indicator for the MOS interface quality. With decades of study, reasons behind the poor 4H-SiC/SiO_2 interface are still not fully understood. In [46], a discussion was made on the potential origins of interface traps, and two sources were identified, first of which is the carbon accumulated at the MOS interface during the SiC oxidation process. The reactions occurring during Si and SiC oxidation processes can be generally expressed by reactions described in Eqs. (1) and (2):

$$Si(s) + O_2(g) \rightarrow SiO_2(s) \tag{1}$$

$$SiC(s) + x\,O_2(g) \rightarrow SiO_2(s) + CO/CO_2(g) \tag{2}$$

Depending on the oxygen pressure, there may be some intermediate reactions [49], but it can be seen that SiC oxidation is accompanied by the release of gaseous carbon, either CO or CO_2. However, the increase of oxide thickness after the oxidation process goes for a while makes it more difficult for carbon to escape, and the reaction (Eq. (3)) may occur instead:

$$SiC(s) + O_2(g) \rightarrow SiO_2(s) + C(s) \tag{3}$$

The theory of carbon failing to escape through thicker oxide naturally leads to the idea that there should be less carbon at the MOS interface with thinner oxide. Indeed, a recent study [50] demonstrated an almost ideal SiC/SiO_2 interface with a very thin oxide layer (≈14 nm);

the D_{it} value was below 10^{11} cm^{-2} eV^{-1}. However, as mentioned before a certain oxide thickness (≈50 nm for SiC MOS devices) is necessary for a reasonable threshold voltage, which means very thin oxide is not practical in real device fabrications. Thin thermally grown oxide with deposited oxide on top of it may be an option but still not easy, since deposited oxide is known to contain many more defects than thermally grown ones [51].

This leads to the second source of SiC/SiO_2 interface traps, namely, oxide defects. Oxide defect-induced traps are essentially the oxide-trapped charges mentioned before. In SiC/SiO_2 study they are also known as 'near-interface traps' since they do not actually sit at the interface but instead are located in the SiO_2 very close to the interface. For Si, energy levels of oxide-trapped states are in the conduction band, thus not electrically active. For SiC, however, whose band gaps are 2–3 times wider, many of the oxide-trapped charges located in the band gap are being electrically active, as has been confirmed by photon-stimulated electron tunnelling [52]. The near-interface traps have time constants much smaller than the carbon clusters, which are also called fast traps while the latter known as slow traps. A schematic representation of the carbon cluster mode is illustrated in **Figure 8** with energy levels of the traps specified. Due to the much lower mobility of holes than electrons, SiC MOS devices are almost exclusively based on n-channel design; naturally, the traps scattering the channel carriers most are the ones located close to the conduction band edge. **Figure 8** shows that the 4H-SiC conduction band edge is mostly troubled by near-interface traps and π-bonded carbon clusters, with the former more dominant. Both of these traps are accepter-like, namely, negatively charged when being occupied, which can explain the quite positive threshold values often observed for 4H-SiC MOS devices. On the other hand, 3C-SiC is free from near-interface traps attributed to a smaller band gap but is still troubled by π-bonded carbon clusters. These carbon

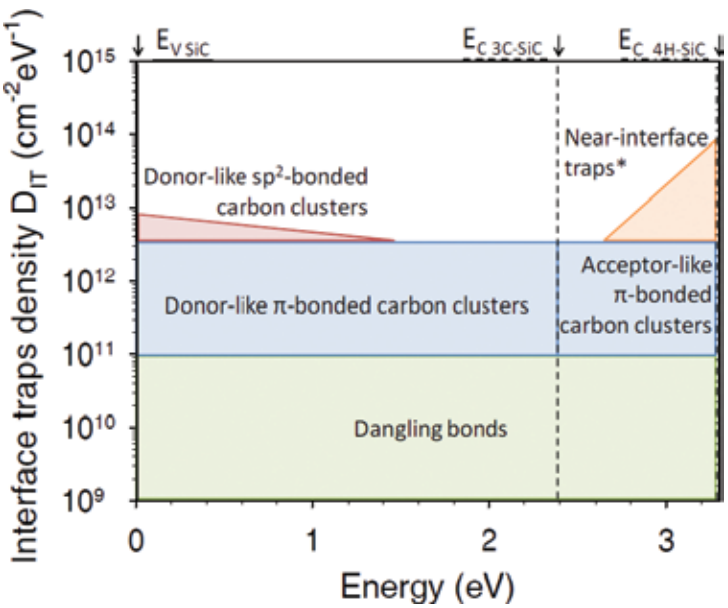

Figure 8. Schematic representation of the 'carbon cluster model' [53].

clusters near the 3C-SiC conduction band edge are donor-like, thus positively charged if unoccupied, which means the resultant threshold voltage may be more negative. Dangling bonds still contribute to some of the interface traps here but are only secondary concerns. Consequently, for SiC, H_2 annealing is not as effective as it is for Si. Other techniques had to be explored for SiC/SiO_2 interface optimisation.

4.3. SiC/SiO_2 interface treatments

The efforts put into improving the SiC/SiO_2 interface can be grouped into three directions, namely, post-oxidation annealing (POA), channel counter-doping and high-temperature oxidation.

Nitridation may be the most widely used method to improve the $4H\text{-}SiC/SiO_2$ interfaces. It is usually achieved by annealing thermally grown gate oxides in nitrogenous trace gas environment (NO or N_2O), called post-oxidation annealing (POA). It is believed that the N-O bond breaks at high temperature and supplies free oxygen which oxidises 4H-SiC [54]; consequently, nitridation by POA is accompanied by a further growth of the oxide, although not significantly. Gate oxide can also be directly grown in such atmosphere to obtain similar benefits. Previous X-ray photoelectron spectroscopy (XPS) results showed that after NO/N_2O POA, there were fixed nitrogen atoms near the interface with a density $\approx 1 \times 10^{14}$ cm^{-2} [55], even after removing all the oxide by a hard HF etching, indicating that nitrogen atoms were strongly bonded to 4H-SiC substrate. There had been evidence showing the nitridation reduced both carbon-related and near-interface traps [56], even though there is still no complete explanation of the theory established. The near-interface traps are probably reduced by the formation of an oxynitride layer between 4H-SiC and gate oxide, which redefines the oxide/semiconductor boundary [57], and the oxide-trapped charges are no longer near the interface. In terms of the carbon clusters, they are probably decomposed by inserted nitrogen atoms, which shift the energy levels of remaining clusters deeper into band gap, namely, further away from the conduction band edge and less effective in terms of scattering channel carriers [58]. Apart from N_2O/NO, it was reported that annealing the gate oxide in a phosphorous trace atmosphere ($POCl_3$ [59] or P_2O_5 [60]) also led to a channel mobility improvement, although it introduced severe threshold voltage instability as a result of SiO_2 being converted into phosphor silicate glasses. Reducing the number of interface traps by introducing extra atoms into the interface is called passivation, and regardless of the source (N or P), it is always required that enough foreign atoms diffuse through the gate oxide and reach the interface. Certainly higher annealing temperature and time duration will help with that; however, due to the very low diffusion coefficient of nitrogen in SiC, nitrogen atoms saturate only within a monolayer deeper into the interface [61], and consequently the mobility value does not increase further, and the peak value typically stays around 40 $cm^2/V\,s$ [62]. Phosphorous has a higher saturation density than nitrogen in 4H-SiC, but still, the peak mobility value stays around 80 $cm^2/V\,s$ [63] regardless of further increased annealing time durations.

The limitation of thermal diffusion naturally leads to the idea of incorporating more passivating atoms into the interface by ion implantation, also known as channel counter-doping. 4H-SiC MOSFETs were fabricated on nitrogen-implanted substrates and higher peak channel mobility

(≈60 cm^2/V s) than unimplanted or even NO/N_2O annealed samples was observed [64–66], before the mobility curve becomes significantly distorted for a dose level of 2.2×10^{14} cm^{-2}. The success of counter-doping technique brings in another possible explanation [66] other than the defect passivation for the improved 4H-SiC/SiO_2 interface. With the channel surface being partially compensated by the nitrogen implantation, a depletion region is formed between the thin counter-doped n-type surface and the underlying p-type channel region. The n-type counter-doped surface may be positively charged even without any gate bias due to the p-n junction depletion. In inversion mode, higher carrier mobility can be achieved since these positive charges will cancel part of the negative electric field built in the channel region, reducing the surface roughness scattering. Apart from nitrogen, other elements were also studied for the counter-doping. In [67], a variety of ions including B, N, F, Al, P and Cl were individually implanted into a 4H-SiC substrate, which was then oxidised to make MOS capacitors. It turned out only group V elements (N and P) led to a reduced D_{it} while the other increased it. A negative shift of flat band voltage is always observed for N or P counter-doped MOSFETs, a natural result of the channel being partially compensated. For devices fabricated with N- or P-based POAs, similar negative shifts were also observed, which suggests that counter-doping may have occurred in POAs through minor thermal diffusion, making it difficult to distinguish the effects from passivation and counter-doping. More recently [68], counter-doping 4H-SiC MOSFET channel using Sb was studied, and a peak field-effect mobility as high as 80 cm^2/V s was obtained. The fact that the mobility value dropped to almost zero at 70 K (Sb freezes out) confirmed that the improvement is not achieved by defect passivation, since otherwise the mobility should only be influenced by SiC electrons and the Sb freeze-out will have minimal effect. Further processing the Sb counter-doped sample with NO POA led to an increased channel mobility in all temperatures including 70 K, which suggests that the counter-doping and defect passivation may be two independent mechanisms, yet both increase the channel mobility.

Both previous methods introduce extra foreign element atoms to the SiC/SiO_2 system. It will be ideal to have an as-oxidised MOS interface free from excessive interface traps. High-temperature oxidation is considered as a possible solution. It was firstly reported in [69] that D_{it} decreases with increasing oxidation temperature, which was related to a reduction of SiC_xO_y near the interface at higher oxidation temperature. More recently [70], a channel mobility of 40 cm^2/V s was reported for 4H-SiC MOSFET with gate oxide thermally grown at 1500°C without any further treatment, and the XPS measurement suggests a reduction of carbon near the interface. The mechanism behind high-temperature oxidation is still unclear and needs to be explored more.

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Chapter 4

High-Performance Packaging Technology for Wide Bandgap Semiconductor Modules

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Additional information is available at the end of the chapter

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Abstract

The properties of wide band gap (WBG) semiconductors are beneficial to power electronics applications ranging from consumer electronics and renewable energy to electric vehicles and high-power traction applications like high-speed trains. WBG devices, properly integrated, will allow power electronics systems to be smaller, lighter, operate at higher temperatures, and at higher frequencies than previous generations of Si-based systems. These will contribute to higher efficiency, and therefore, lower lifecycle costs and lower CO_2 emissions. Over 20 years have been spent developing WBG materials, low-defect-density wafers, epitaxy, and device fabrication and processing technology. In power electronics applications, devices are normally packaged into large integrated modules with electrical, mechanical and thermal connection to the system and control circuit. The first generations of WBG device have used conventional or existing module designs to allow drop-in replacement of Si devices; this approach limits the potential benefit. To realize the full potential of WBG devices, especially the higher operating temperatures and faster switching frequency, a new generation of packaging design and technology concepts must be widely implemented.

Keywords: reliability, solder, wirebonding, inductance, thermal impedance, sintering, high-frequency

1. Introduction

Semiconductor packaging provides the interface between semiconductor devices and the outside world. All semiconductor devices need packaging of some sort, whether they are the integrated circuits of a computer's central processing unit, an amplifier, diode, transistor or

any other kind of device. This chapter focuses on power modules: a subsection of the field of semiconductor packaging. A power module normally contains several power electronics devices such as MOSFETs or IGBTs, diodes, and often the associated passive components like gate resistors and DC link capacitors. The package provides a mechanical interface with the rest of the system, since most semiconductor components produce heat that must be managed in order to keep the device below its maximum allowable junction temperate (T_{jmax}), the package is almost always mechanically connected to a heatsink. The packaging is also the primary thermal interface between the heat-generating devices and the heat sink. The operating temperature of the devices defines their performance and long-term reliability, if devices operate at higher temperatures their reliability will decrease exponentially as temperature increases [1]. As a result, the thermal interface provided by the packaging is crucially important, and many of the properties of the processes and materials are optimized to provide the best possible heat sink with the lowest achievable thermo-mechanical stress. Electrical interfaces between the devices and the system are also features of the package, with signal pins and power terminals being internally connected to the devices, and emerging through the packaging to allow external connections. Depending on the design, it is also common for electrical insulation to be a feature of the package, normally to ensure that the high-voltage part of the circuit inside is suitably isolated from the heatsink to which the package is attached. The outer surface of the package must also meet the requirements of creepage and clearance to ensure that the terminals are properly insulated from each other. The packaging also provides environmental protection for the modules to some degree. The simplest arrangements have a plastic housing filled with a potting compound, normally a silicone gel. The plastic case makes the module a robust component which can easily be handled during testing, installation, and operation while protecting the devices inside. The case and potting provide protection from dirt, contamination and foreign objects which could damage them or their interconnections. The package can provide reasonable protection from liquid water, but most packages do not provide thorough protection from water vapor. For special applications such as some aerospace systems, hermetically sealed packages are required to provide complete isolation from the environment.

A simplified diagram of a typical power electronics module is shown in **Figure 1** which has the main design elements outlined above. There is a broad range of shapes and sizes of power modules, but the structure of many of the most commercially successful ones can be described as having similar construction to this. The semiconductor devices are attached, normally using solder, to a ceramic tile metallized with copper on each side. The tile, or substrate, provides a thermal path to extract heat from the device and has a circuit outline etched into the top to provide.

Isolation between contact pads for the various terminals of the device: anode and cathode in the case of a diode; emitter, gate and collector in the case of an IGBT; or gate, drain and source in the case of a MOSFET for example. Connections between these pads and the device are made using wirebonds, aluminum being a widely used metal in power electronics which is compatible with the aluminum surface of the device. With this combination of soldering and wirebonding, the device is connected to the package, and these connections are some of the most crucial for ensuring the long-term reliability of the entire package under real-world

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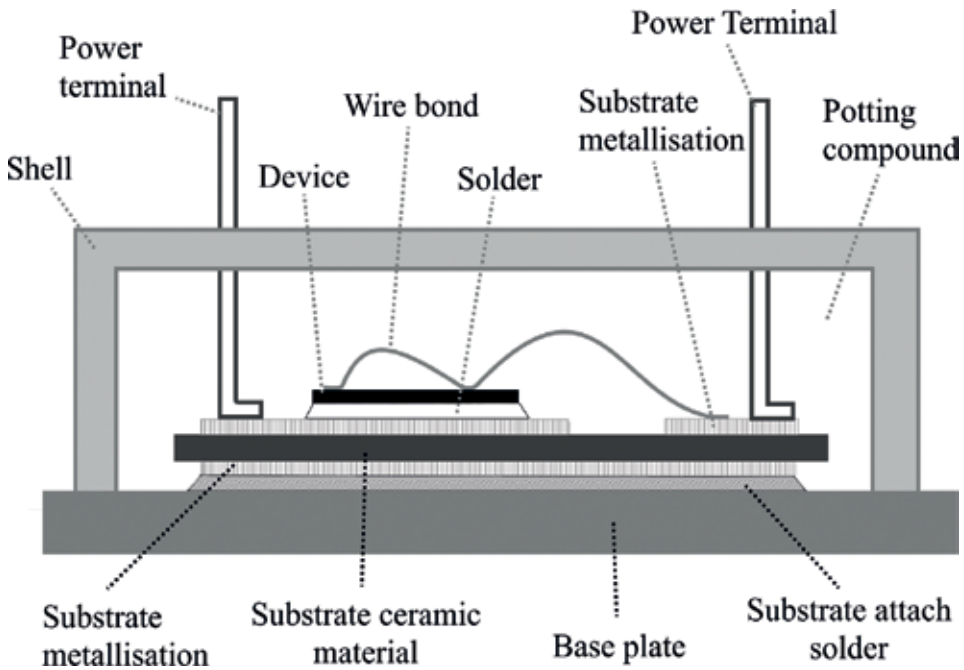

Figure 1. A simplified diagram of conventional power module packaging structure. Key to structure is the insulating ceramic tile which is soldered to a base plate. The semiconductors are soldered to the topside of the tile along with the power and signal terminals. The topside interconnection to the devices is achieved with wire bonding. The structure is then encapsulated in silicone gel and a plastic housing.

conditions [2]. The entire substrate is then soldered to the base plate, providing a thermal path from the device to the outside world. In many packages, multiple substrate tiles are soldered into one module. Terminals also need to be connected to the contact pads on the substrate tile to allow current flow into and out of the package, and auxiliary signal pins are connected for the device gates and other connections needed to control the devices. The entire arrangement is then surrounded by a plastic case and potted with dielectric gel to provide some protection and electrical insulation (**Figure 2**).

Power module packages based on the principles shown in **Figure 1** have been successful for decades but are not capable of exploiting the benefits of WBG devices such as higher junction temperatures and faster switching speeds. Every part of the package needs to be reconsidered if it is to become a high-performance part suitable for housing WBG semiconductors: the backside die attach material must be able to operate reliably for years at junction temperatures over 200°C; the topside attachment must be suitable for high power density and high reliability. The ceramic substrate and the base plate must have excellent thermal conductivity to keep the devices as cool as possible. The current density of SiC devices is higher than Si which is an advantage for reducing the volume of components, but it also makes it more difficult to cool them. The encapsulating gel must be able to sustain high temperatures without degrading especially since they are normally in intimate contact with the devices themselves, and therefore will be subject to some of the highest temperatures in the package. Further from the

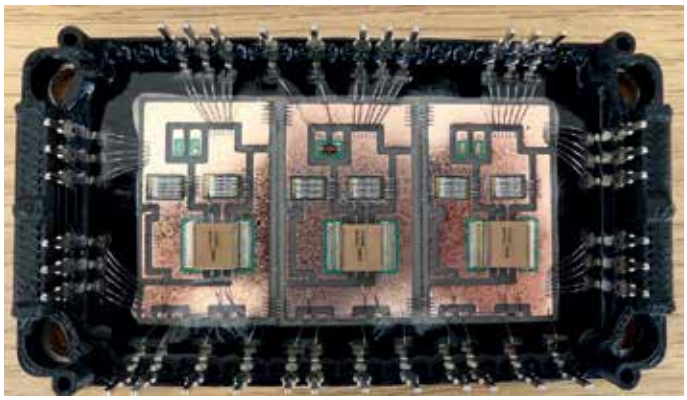

Figure 2. An example of a three-phase power module with one SiC MOSFET per switch, negative temperature coefficient resistor for temperature sensing, and a DC link capacitor on each substrate. The package concept is similar to that shown in **Figure 1**. Image courtesy of Dynex Semiconductor Ltd.

junction, temperatures will be lower but the capabilities of materials still need to improve, including the plastic housings, and glue used to connect the housing to the baseplate.

These shortcomings in packaging technology have been recognized and described thoroughly for example in [3], and Section 2 presents a summary of some of the solutions that have been investigated.

2. Materials and processes

SiC has a higher thermal conductivity than Si which is one of the properties that makes it an excellent material for power electronics devices. To take advantage of this, all the other materials in the module must have compatible high performance. Alumina or Al_2O_3 is the most widely used ceramic used for insulating substrates in power modules primarily due to its low cost and large numbers of suppliers across the world. The properties of Al_2O_3 are not ideal, having a relatively large thermal impedance and high coefficient of thermal expansion. AlN is commonly used in modules where higher reliability and lower thermal impedance are more important requirements, in applications such as rail traction and renewable energy, where system failures can be costly in terms of maintenance and operational losses. AlN has a thermal conductivity around six times greater than Al_2O_3, and CTE around half as much, making it a much more efficient heat sink which is a better thermal match to the semiconductor devices and therefore reduces thermomechanical stress, which is the main cause of fatigue and wear-out failure in power electronics modules. Silicon nitride, Si_3N_4, is being increasingly used because it has an even lower CTE than AlN and high mechanical strength [4]. The bond between the ceramic material and the metal layer of the substrate is a common wear-out failure mode caused by long time-constant (minutes and hours rather than seconds) temperature cycling of the module. Therefore, the reliability of the overall system is dependent on the reliability of the substrate material, and improving substrates is an intense area of R&D for the

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manufacturers. Active metal brazing for bonding the metallization to the ceramic has shown to be more reliable to peeling off then direct copper bonding (DBC), and also aluminum direct bonding (DBA) has been shown to excellent reliability. For these reasons, Si_3N_4 is likely to be an ideal substrate candidate material for WBG devices. Conventionally substrates have been formed of a single layer of ceramic with metallization on either side, but double layer ceramics are becoming more common for WBG applications: Two ceramic layers are bonded together with a metallization layer between them, with metallization on the top and bottom sides also, giving an overall sandwich structure of three layers of metal and two ceramic [5]. Typically, the top and middle metal layers are used for conducting current, and the bottom layer is used to connect to a heatsink. Electrical connections are made using through the ceramics, thus allowing a very low profile package with a large degree of overlap between conducting surfaces. This allows designers to create very low inductance and low thermal impedance packages.

The module baseplate in silicon power module has normally been made from Cu in less-expensive modules and AlSiC in high-reliability modules. AlSiC is required for achieving the maximum benefit from AlN ceramic tiles, as the large CTE mismatch between AlN and Cu causes excessive stress, despite the high thermal conductivity of the system. High reliability baseplates are normally the largest single component of a module and the most expensive after the semiconductors. The trend in baseplate material is toward higher thermal conductivity, lower CTE, and higher mechanical strength. Base plates must also be finished to a high quality to give excellent bonding and interconnection with the other components. Enhanced cooling can be provided to the module by incorporating metal pin fins on the underside which can be used to directly liquid-cool the material, and these solutions have been widely used in automotive and traction applications to give low Z_{th} from junction to case in the module [6]. Recently, MgSiC has emerged as a promising new baseplate material, which offers marginally higher thermal conductivity (up to around 210 W/mK compared with 170–180 for AlSiC) but which could be simpler to manufacture, and hence help to reduce cost [7].

For high-power modules, thick copper bus bars are needed to handle high current loads without overheating. Solder interconnects have been very common as they are easily manufacturable and can be made in the same process as die attach soldering or substrate attach. As these other processes are becoming solder free, a new attach process for bus bars is beneficial, otherwise one soldering process will remain. Ultrasonic bonding is a mature process for bus-bar attach, which is already widely used in power electronics modules [8].

2.1. Die attach

The most widespread interconnection process for the backside of vertical power semiconductor devices is soldering, either using a solder paste which is mixture of flux and solder alloy; or using a solder preform which is a pre-fabricated foil of solder alloy, usually with the same surface area as the device to be soldered. The choice of alloy to be used for the die attach depends on several factors, such as whether or not the application has a requirement to be Pb free; the maximum processing temperature of other components in the module (such as passive SMT components); and cost. If there is no requirement to be Pb-free, this

allows a wide choice of relatively inexpensive Pb-based alloys with melting points up to 300°C, albeit alloys which are far from being eutectic and could have a pasty phase 10°C wide or more between solidus and liquidus. High-melting point lead-bearing alloys are common in high-power, high-reliability power modules in which maximum T_j of the current generation of Si devices is 150°C and while it is theoretically possible to operate Si devices of around 200 V blocking voltage up to 200°C [9], is unlikely to increase above 175°C in high-power modules with blocking voltages greater than 3.3 kV due to device-physics limitations. This gives a temperature range of more than 100°C between the absolute maximum junction temperature of the devices and the melting point of the solder. When considering the suitability of an interconnection material, a useful parameter to define is the homologous temperature, T_H, where

$$T_H = \frac{T}{T_M}$$

T (K) is the temperature of interest, which could be the mean operational temperature or the maximum junction temperature in this case, and T_M (K) is the melting point of the material. In general, smaller homologous temperatures will give longer lifetimes in electronics packages either by operating as far as possible from the melting point of the solder, or by using a higher melting point solder; however, creep deformation can still occur at relatively low temperatures [10]. If T_H is <0.4 this is considered mechanically stable, $0.4 < T_M < 0.6$ is considered to be the creep range, sensitive to strain, and $T_M > 0.6$ is unable to bear engineering loads [9]. If we take 473 K (200°C) to be a useful operating temperature for SiC devices, the melting point of 1234 K (961°C) for pure silver gives a T_H value of 0.38. In comparison, a Pb-rich solder with a melting point of 573 K (300°C) has a T_H value of 0.82.

The wide band gap of SiC or GaN allows devices to have a maximum junction temperature of around 300°C, this rules out any solder with a melting point close that figure. Solders with even higher melting points could be too costly, so there has been a great deal of effort in packaging R&D to find an alternative interconnection technology for Si and WBG devices. At the same time that WBG power devices are becoming mature, along with the associated demands on power electronics packaging, there is also the external pressure of environmental policy to eliminate hazardous substances from manufacturing. As mentioned earlier, Pb and its use in solder have been specifically targeted in legislation worldwide as a material which could be eliminated from consumer and industrial products. The European End of Life Vehicle (ELV) Directive sets targets for the reuse, recycling, and recovery of ELVs and their components [11] and the European Reduction of Hazardous Substances (RoHS) Directive Restriction of the Use of Certain Hazardous Substances in Electronic and Electrical Equipment specifically restricts the use of Pb. As of 2018, alloys with a Pb content of more than 85% are exempt from the RoHS restrictions but are subject to periodic exemption review.

In 2010, a consortium of Bosch, Infineon Technologies, NXP, Freescale Semiconductor and STMicroelectronics formed with the aim of developing alternative processes for die attach in semiconductor packages to replace Pb solders, specifically high-melting point solders. The

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consortium is known as the Die Attach 5 (DA5) [12]. The DA5 are focusing on four potential replacements to high-Pb solder: Ag sintering; high electrical and thermal conductivity adhesives; alternative solders; and transient liquid phase soldering (TLPS) [13]. Alternative solders with appropriate properties are available, such as Au80Sn20, AuGe, and AuSi, but the high gold content makes them too expensive to be viable for most applications. Even the best conductive adhesives have poor electrical and thermal properties compared with solder. Ag sintering or transient liquid phase bonding provides a more promising alternative.

2.2. Silver sintering

Sintering is the process of forming a solid mass of material from smaller particles or flakes using temperature, pressure, or both, while remaining below the melting point of the sinter material. It is widely used in manufacturing of metallic and ceramic parts. In the context of power-electronics packaging, we refer to sintering as the process of forming interconnection layers by processing a layer of micro or nanoparticles (normally of Ag) by applying a temperature and pressure profile for a controlled period of time. The resulting porous Ag layer has excellent electrical and thermal conductivity and a melting point equal to bulk silver at 961°C, normally with some remaining porosity. The silver particles (also known as the filler) in the paste are combined with a capping agent, binders and solvents. The purpose of these additional materials is to ensure that the silver particles do not begin to sinter themselves together before the actual processing begins, and to make the consistency of the past suitable for screen printing or dispensing. A range of chemicals have been used by the different suppliers of sinter pastes, a useful summary of these was published in 2014 [14]. Sinter pastes are broadly classified as being either 'pressured,' that is they require pressure to be applied during processing, or 'pressureless.' Sintering is an attractive technology for Pb-free and high temperature operations because the processing temperature are similar to those already used for device soldering, and pressureless paste in particular is seen as a potential drop-in solution which would require the minimum of additional manufacturing equipment; however, it is common for even pressureless pastes to benefit from some application of pressure during the manufacturing stage to increase the deformation of the Ag filler particles and increase the diffusion rate of silver atoms. An early patent (1973) for using sintering to join metal parts illustrated the use of the technique in lap, butt, and T-joints [15]. Sintered connections are not a new technology in semiconductor device packaging, with sintered glass beads being used for insulating materials, and sintering ceramic sheets being used as substrates ([16] for example). Only more recently, sintering has been used as a means to connect electronic components themselves [17] and particular power-semiconductor devices [18]. In 2006, a sintered interconnection for semiconductor device interconnection was described [19] which had an electrical conductivity of around 2.6×10^{-5} $(\Omega cm)^{-1}$, thermal conductivity of around 2.4 W/Kcm and apparent elastic modulus of 9 GPa. The high thermal conductivity of a sintered joint can lead to a small reduction in the thermal impedance Z_{th} from junction to case compared with a soldered die, particularly in small modules where there are not many devices which may overlap thermally with one another. One team of researchers [20] observed 12% lower thermal impedance compared to a SAC305 solder connection (**Figures 3** and **4**).

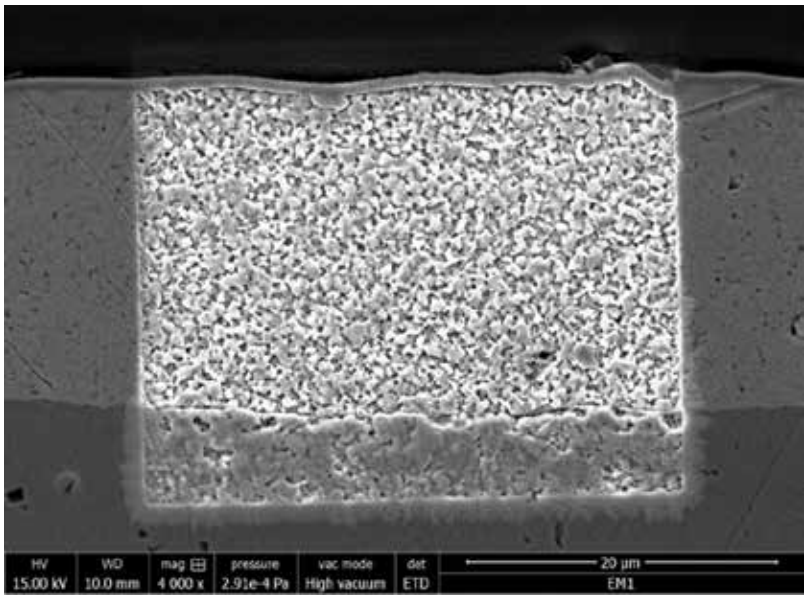

Figure 3. Cross section of a sintered die attach layer captured using scanning electron microscopy. The bright central area shows where the porosity of the layer has been revealed using focused ion beam (FIB) milling. The edges of the image show the apparent porosity after polishing with diamond suspension fluid. Image courtesy of Dynex Semiconductor Ltd.

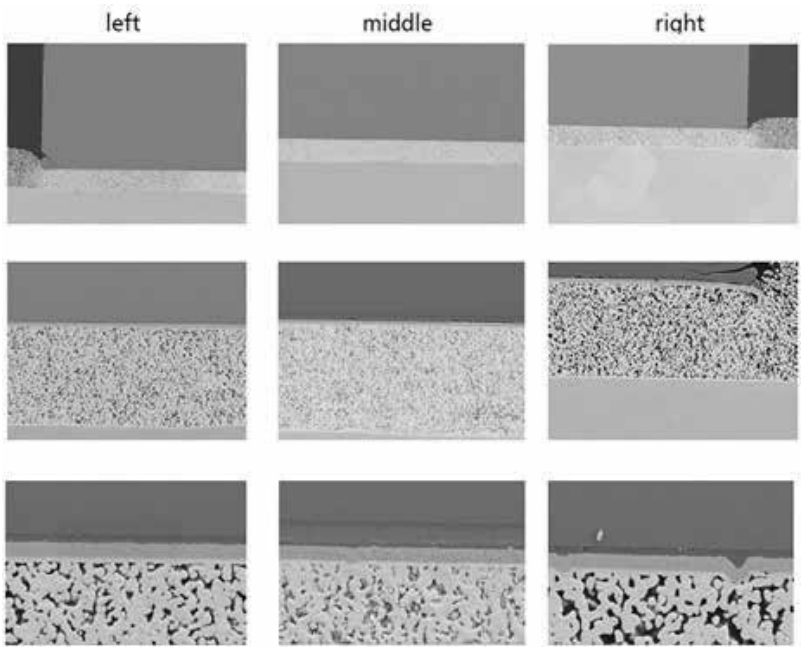

Figure 4. Scanning electron microscope (SEM) images of the sinter layer under a semiconductor die showing the variation in porosity from the edges to the middle. The measured porosity on the left, middle, and right-hand side is 22.6, 19.5 and 26.1%, respectively. Image courtesy of Dynex Semiconductor Ltd.

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Sintering for die attach in power electronics modules has been an area of extensive research and development and a recent consideration of the maturity of the state of the art has been published in [14, 21]. Ag sintering processes are mature enough for some manufacturers to ship power modules with sintered interconnections, for example it has been used by Semikron to produce entirely solder-free modules [9] and has been used successfully in bipolar devices for joining large thyristors to molybdenum plates. The SKiN module went even further and replaced the wirebonds with a PCB which is sintered to the topside of the device [22]. Uncertainty around the potential for widespread use of Ag sintering for die attach centers on a relative lack of data on the long term reliability compared with soldered interfaces, although many laboratory studies of reliability have been carried out that invariably show a large increase in the number of cycles-to-failure, sometimes by a factor of 10 compared to solder.

One reason silver sintering is more challenging to apply to mass production because of the difficulty in carrying out in-line high-volume automated quality control of sintered joints. In IGBT module production lines, there is 100% screening of the solder layers using X-ray imaging to find and measure the presence of voids in the solder caused by contamination, poor wetting or process irregularities. Modern industrial X-ray imaging systems are capable of automatically detecting and measuring the area of voids for statistical process control and comparison against defined pass/fail criteria. Imperfections in sintered bond lines do not appear as voids in the die attach layer, a good sintered joint and a failed sintered joint look identical to most X-ray systems with the exception of an advanced 3D tomography system, but such analysis would take too long per scan and therefore be too expensive to use as a screening technique in large-scale production. Poor bonding during the sintering process which leaves thin planar areas of no contact between the device and sinter layer, or the sinter layer and the substrate, might potentially be identifiable using scanning acoustic microscopy (SAM). The other alternative would be to forgo complete screening and instead carry out destructive tests on samples from each production batch using the mechanical strength measured in a die-shear test for example as a figure of merit. An alternative destructive method used during process development is a bend test in which the die and substrate and bent over a mandrel, of the substrate cracks and deforms before the device adhesion fails, the sintered joint is considered to be good. **Figure 5** shows the result of a bend test of 0.635 mm thick AlN active metal-brazed (AMB) tiles from the FIR3ST project power module. The tiles have been bent over a mandrel almost 90° which has caused the AlN ceramic and the SiC devices to fracture. The devices remain adhered to the surface.

The long-term reliability of Ag-sintered interfaces under thermomechanical cycling conditions is not as well understood as for soldered interconnections, but is an area of ongoing research. Sintered interconnections are vulnerable to the same driving forces of failure as soldered ones because they form a sandwich of materials with different coefficients of thermal expansion and experience temperature cycling with both fast time constants (caused by losses when the devices are switched and conducting current) and slow time constants (caused by heat soak of the overall system and the specific mission profile of the application). This causes thermomechanical stress which leads to cracking and delamination of the layers. Even if the CTE of the materials is closely matched thermomechanical failure modes will take place because power semiconductor modules are, in general, rarely in thermal equilibrium, but always have some temperature gradient across the vertical structure of the module. Studies

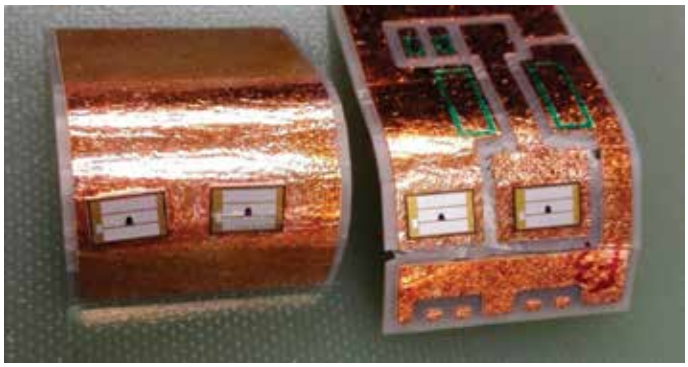

Figure 5. Sintered SiC MOSFETs on direct bonded copper (DBC) ceramic tiles after bend test. The substrate is bent through almost 90° and is cracked beneath the devices, which have remained adhered to the damaged surface. Image courtesy of Dynex Semiconductor Ltd.

have focused on how resilient sintered connections are compared with soldered interconnections under temperature cycling conditions, and on the nature of failure modes unique to sintered interfaces. Mechanical shear strength of nano-silver sintered die has been used as a measure of bond quality in 1.706 × 1.380 mm SiC SBDs [23]. It was found that the die shear strength was strongly related to the process time and temperature, with a 40 minute dwell at 300°C providing shear strength of around 40 MPa. These reduced by around 50% (the failure criteria defined in this study) after 5000 temperature cycles between 50 and 250°C. The reduction in shear strength was attributed to thermal-stress-induced dislocation creep leading to the formation of microcavities and grain boundaries.

The properties of sintered interfaces have been found to be a function of the porosity and porosity is a function of the starting material and the pressure used in the process [24]. Even small changes in the porosity can have a large impact, for example increasing the porosity from 5 to 7% (in other words from 95% dense to 93% dense) decreased the thermal conductivity from 380 to 320 W/mK at 100°C, accompanied by a similar relative change in electrical conductivity. On the other hand, the coefficient of thermal expansion was found to be relatively constant at temperatures less than 250°C and between porosity of 5 and 38% [25]. One study found that an established production process capable of sintering DBC master cards up to 5″ × 7″ in area has a porosity of 5%, but that reducing pressure by a factor of 4, the porosity increases to around 20%. **Figures 3** and **4** show SEM images of a 20 μm thick sinter layer showing the variation in porosity between the central area of the bond and the edges. Focused ion beam (FIB) milling is needed to reveal the true porosity under the polished surface.

A comparison of some properties between solder and silver sinter materials is shown in **Table 1**. Large area sintering has been investigated as a possible alternative to the use of solder for substrate to baseplate attachment [26]. A large ceramic tile (40 cm^2) was sintered to a baseplate and subjected to temperature cycling between −40 and +150°C. The integrity of the sample was measured using scanning acoustic microscopy and the test was stopped after 3000 cycles when it was found that the sinter layer showed no signs of degradation, but the substrate was beginning to delaminate. This is a common trend found in many papers on sintering: practically, all of the research papers report considerable increases in reliability under

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temperature cycling and active cycling conditions, between a factor of 4 and 10 increases in the number of cycles to failure. This large increase in reliability of one specific interface usually means that another interface in the system becomes the first failure mode instead of the die attach layer, or other solder layer. In many cases, the weak point is the ceramic tile, which starts to delaminate and will quickly cause a large rise in the thermal resistance between junction and case once the delamination begins to impinge on the area under the devices.

One negative aspect of sinter layers for both die and substrate attach is that the thin, stiff layers offer less stress relaxation to the structure, and the mechanical stress is transferred to other layers in the module. **Figure 6** shows how from changing from soldering to sintering of substrates on a base plate the convex bow shape is completely reversed to become concave. The convex bow is necessary to ensure good thermal contact during operation as the module tends to flatten out due an effect similar to a bimetallic strip as it heats up, thus ensuring as large as possible contact area between base plate and heat sink. If the base plate has become concave, there will be a large area which is not contacted with the heat sink, so thermal impedance will increase, and as a result, the junction temperature.

2.3. Diffusion soldering

In any fully formed solder joint, there is a layer of intermetallic compounds formed as the metallization of the workpieces is dissolved into the molten solder. Typically, these intermetallic

Parameter	Pb-Sb solder	Pb-free solder	Ag nanopowder
CTE (ppm/K)	28	20	19–21
Thermal Conductivity (W/mK)	70	70 (SnAg3.5)	240–290
Melting Point (°C)	183	220	~961
Electrical Conductivity	14.5	8–12	41

Data have been gathered from [9, 28, 29].

Table 1. Showing a comparison of some important properties of solders and sinter materials used for die attach.

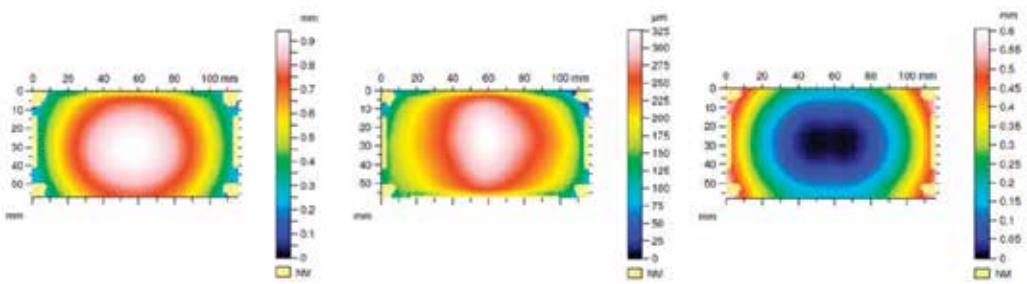

Figure 6. Three profiles of nominally identical baseplates before processing (left), after substrates have been soldered (middle) and after substrates have been attached by sintering (right). The sintering process causes the baseplate to switch from a convex to a concave profile.

layers are of irregular thickness of around several microns. Diffusion soldering promotes the growth of the intermetallics throughout the bulk of the solder joint, so that at the end of the process, the entire solder layer is formed of intermetallics. Sn rich solders and copper metallized substrates are a common combination which give Cu_6Sn_5 and Cu_3Sn intermetallics that have melting points of 416 and 676°C, respectively. A combination of Ag metallized die backside and Sn rich solder can give Ag_3Sn (T_m = 480°C). Studies have shown that diffusion-soldered interconnections can have a factor of 10 higher reliability than conventional solder joints, at least as good as sintered interconnections [27].

2.4. New topside interconnections

Aluminum wedge wirebonding remains the most widely used topside interconnection and has been an area of intense R&D to improve reliability. The most dramatic change is the use of copper wire instead of aluminum [30, 31]. The higher thermal and electrical conductivity of the wire allows increased current density for a given reliability or greater reliability at a given current density. The use of copper wire for die topside interconnection requires a special metallization on the topside of the chip, and some groups have experimented with the use of thick pads on the die topside to enhance the bondability of copper wire [32]. An alternative is the use of aluminum clad copper wire [33–35].

One study introduced the concept of spot sintering braided cable connections to the topside of devices [36]. A power cycling comparison was made between soldered, wirebonded diodes; and sintered diodes with spot sintered braid topside interconnection. A load current of 90A was used with a constant on time and off time of 1 and 5 s respectively. This test method gave a ΔT_j of between 86 and 100 K. The average number of cycles to failure of the soldered/wirebonded interconnection was 50 k cycles, for the sintered die, it was around 300 k cycles.

3. Special design considerations for wide band gap power modules

Advantages of using unipolar wide-band gap devices in power electronics applications also have downsides. High switching speeds when switching inductive loads will cause large voltage overshoots which may exceed the breakdown capability of the device. The ringing of the voltage and current in the circuit caused by fast switching can have implications for EMC and interference at a system level. **Figure 7** shows examples of waveforms from 3.3 kV rated devices.

Packaging design has an important role to play in mitigating these unwanted side effects. Any electronic component always has some unwanted electrical characteristics and these are normally referred to as ‘stray’ or ‘parasitic’ properties. Stray capacitance, inductance, and resistance can all have negative effects in power electronics modules, and the fast switching speeds of WBG devices make it crucial to not only minimize these stray properties, but even to engineer them to specific values in order to optimize performance. Stray inductance causes voltage overshoots during periods of changing electrical current according to the relationship

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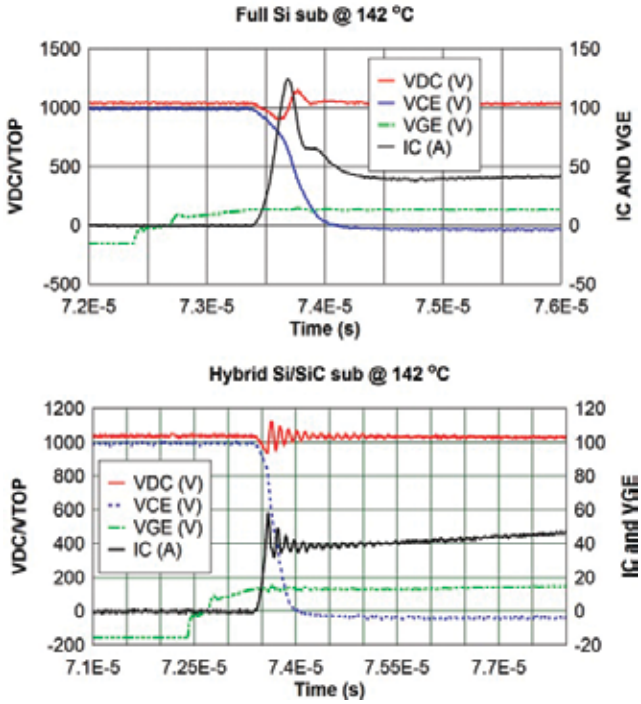

Figure 7. Turn-on waveforms for a 3.3 kV Si IGBT with Si fast recovery diode (top), and the same IGBT but with SiC SBD (bottom). The first turn off of the unipolar SiC diode causes oscillation of the output current compared with the slower bipolar Si diode [37].

$$V = L\frac{di}{dt}$$

where V is the overshoot voltage, L is the inductance, and di/dt is the rate of change of current. Clearly any inductance in the circuit combined with the high di/dt values associated with WBG devices will cause large voltage overshoots which could destroy the devices if the overall voltage exceeds the breakdown voltage of the device. Stray inductance can easily be minimized in principal by making the current carrying components planar, reducing depth, and overlapping terminals with opposite polarity as much as possible. In practice, however, this is more challenging to achieve: the presence of wire bonds for interconnection make it difficult to achieve really low parasitic inductance, say <5 nH per phase leg, and achieving low profile planar modules requires totally different module design concepts.

3.1. Examples of advanced packaging concept implementation

The power module developed by the I²MPECT collaboration [38] achieved low stray inductance by adopting a wirebond free design, instead sintering a flexible PCB directly to the topside of the devices and using a low profile design with ultrasonically bonded bus bars for

a solder free final package. Ag plated Si3N4 substrates are used and a pressure-assisted sintering processing connects SiC MOSFETs to the substrates, and the substrates are also sintered to the baseplate. The module is shown in **Figure 8**.

A 3.3 kV full SiC power module for rail traction applications has been reported [39] and further use of a full SiC 3.3 kV module rated at 450 A has been described in [40] and a similar package type has been used with 3rd generation SiC MOSFETs to give a module with 3.3 kV voltage rating and $R_{DS\ (on)}$ of 5 mΩ at 25°C and 13.8 mΩ at 175°C [41]. This package is becoming widely available from all the principal power module manufacturers, and while it uses relatively conventional packaging technology, for example, it still relies on extensive wire bonding for the topside connections to the devices, it focuses on using a new design approach to reduce the parasitic inductance. In rail traction applications, power modules normally consist of a single switch circuit topology combined together in the inverter to form phase legs. This newer style of package adopts a phase leg topology in a single package, which allows the bus bars to be designed in a way which allows a high degree of overlap between the DC+ and DC− bus bars, thus reducing the inductance while maintaining a module that can be manufactured on existing production lines.

In [42], a packaging concept is presented featuring a modular full SiC design. In each switching element, 1200 V 80 mΩ SiC MOSFETs with solderable top and bottom sides are joined source-to-source with solder and copper bumps in a flipchip type arrangement. This allows a planar, low inductance, double-side cooled switch to be manufactured with a reported inductance [43] of around 12 nH at 10 kHz. V_{ON} of the MOSFETs was monitored during temperature cycling from −55°C to +150°C with 30 min soak at each temperature extreme and 15 min transition time. No sign of degradation was apparent after 500 cycles. Thermal simulation and FLIR camera measurement showed that with 100 W dissipated in each MOSFET, junction temperature could be kept below 80°C [44]. The main elements of this design are shown in **Figure 9**.

In [45], a novel 10 kV, 60 A all SiC power module prototype was manufactured using third Generation Wolfspeed 350 mΩ SiC MOSFETs. Pressure-assisted sintering was used for the

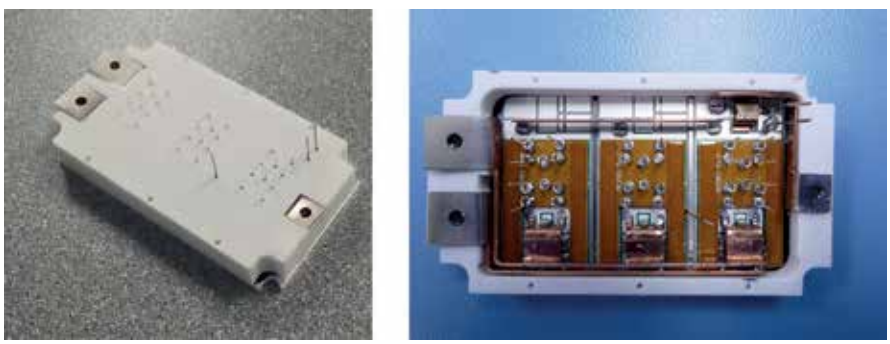

Figure 8. I2MPECT SiC power module. On the left, the complete package with lid. The right-hand side shows package internal solder-free structure, with ultrasonically bonded bus bars, double side sintering, and flexible PCB for topside die attach. Image courtesy of Dynex Semiconductor Ltd.

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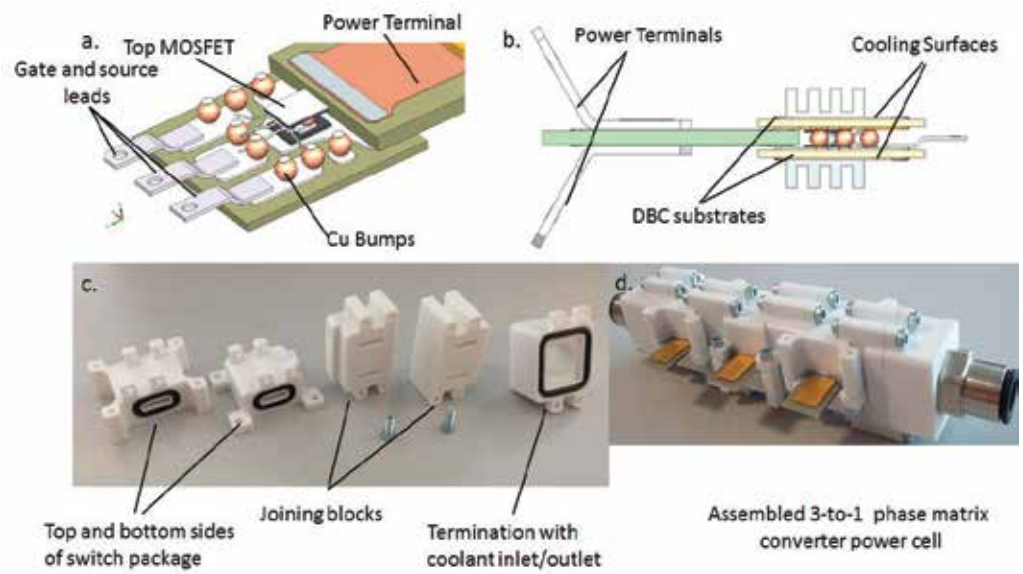

Figure 9. Overview of the module design concept described in [42]. A CAD drawing of the substrate element is shown in (a) revealing the source-to-source soldered MOSFET chips and Cu bumps used for interconnection. (b) Shows the overall sandwich structure allowing double side cooling, (c) and (d) show the real implementation of the building blocks and interconnecting elements. (image credit to Dr. Alberto Castellazzi, Univeristy of Nottingham, and Mr. Philippe Lasserre, deep concept, France).

die attachment in a wirebond free arrangement which gave an overall thermal resistance in the range 0.11 to 0.14 K/W. This design allowed the low power-loop inductance of 4.4 nH to be achieved, while a direct impingement liquid cooled heat sink allows power densities up to 18.1 W/mm$^{3.}$

4. Conclusions

Market forces and technology trends push semiconductor power modules requirements to higher power density, higher operating temperature, higher efficiency, lower cost and higher reliability. Wide band gap power semiconductor devices and Si devices are placing new demands on packaging technology in order to realize the potential of the latest generation of devices to meet these requirements. Silicon devices still have a much larger market share across all applications in which the ever increasing demands outlined above are already providing challenges. As a result, it is often Si power modules that lead the way with the most advanced packaging technology because of the high demand for these devices and competitive market for high reliability products. Sintering, copper wire bonding, wirebond free, planar modules with low inductance have all been introduced with Si devices. It is almost counter intuitive that the first generations of SiC power devices have been brought to market using less advanced packaging technology, often simply being used as drop in replacements for Si devices in conventional packaging, so the full capability of the devices cannot be

utilized. However, it seems certain that the time is near when the combination of advanced packaging and the latest generation of WBG devices is realized in mass production of power electronics modules.

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Chapter 5

Status of SiC Products and Technology

Anup Bhalla

Additional information is available at the end of the chapter

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Abstract

The benefits of silicon carbide (SiC) devices for use in power electronics are driven by fundamental material benefits of high breakdown field and thermal conductivity, and over 25 years of sustained development in materials and devices has brought adoption to a tipping point. It takes the confluence of many separate developments to drive large-scale adoption, which we will examine in this chapter.

Keywords: silicon carbide, SiC, SiC substrates, SiC epitaxy, SiC applications, SiC packaging, SiC Schottky diode, SiC cascode, SiC MOSFET, supercascode, SiC reliability, SiC gate oxide

1. Introduction

Silicon carbide (SiC) has about a 10× higher critical field for breakdown and a 3.5× higher thermal conductivity than silicon (Si). The former characteristic allows unipolar devices to be built with 1/100 on-resistance of silicon devices for the same voltage rating, while the latter allows efficient removal of heat generated during power conversion. The system benefits of SiC for power electronic applications have been amply demonstrated, but the growth of SiC adoption especially for transistors to replace Si IGBTs and Si MOSFETs has, until 2017, been relatively slow [1–3]. Projections in the last 5–10 years showing a "hockey-stick" ramp in SiC shipments have not occurred. It has taken time for the material, technology, and products to mature, reliability concerns to be addressed, prices to drop sufficiently, and the driver and applications ecosystem to develop. Finally, with the migration to 6-inch wafers, SiC adoption is poised for rapid acceleration. We examine each of the major contributing factors,

highlighting the enormous progress across all fronts, as well as the work remaining to be done at this exciting time for SiC power electronics.

2. SiC market projections and driving applications

Figure 1 shows the projected SiC growth by the application area. The traditional markets in power supplies for SiC Schottky diodes and (photovoltaic) PV inverters are rapidly being supplemented by growth in (electric vehicle) EV on-board chargers and charging stations, and 2018 is expected to see growth of SiC transistors in power supplies, previously the domain of silicon super-junction (SJ) MOSFETs. Strong growth is also happening in the UPS systems driven by higher efficiency and in high-performance motor-drive segments. Moreover, strong market pull from automotive inverter companies developing SiC solutions, ramping 2020–2024, is expected to rapidly tip SiC device revenues past the $1 b revenue threshold. Given the favorable policies of governments in Asia and Europe toward EVs (**Figure 2**), the demand currently seen for SiC devices for chargers is expected to grow quickly as market penetration increases from the meager 1–2% to 10–15% in the next decade. Traditional applications will then open up to SiC as prices fall, driven by the growing economies of scale and increasing competition in the supply of SiC substrates, epitaxial material, and products. This will be tracked by the introduction of an ecosystem of high-performance passives, drivers, and sensors that simplify the extraction of the system benefits of this wide bandgap technology. It is expected that SiC will reach about 10% of the Si market by 2025. Over a longer time frame, 3300V–10KV class of products will get deployed in applications such as railway traction, MW motor drives for wind, ship, and industrial use, high-voltage DC power conversion, solid-state breakers, etc.

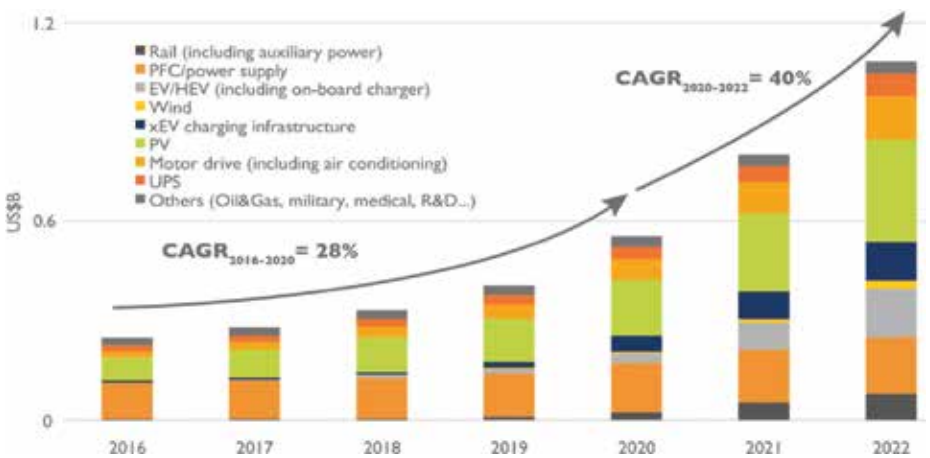

Figure 1. SiC device market projection. Source: Yole developpement 2016.

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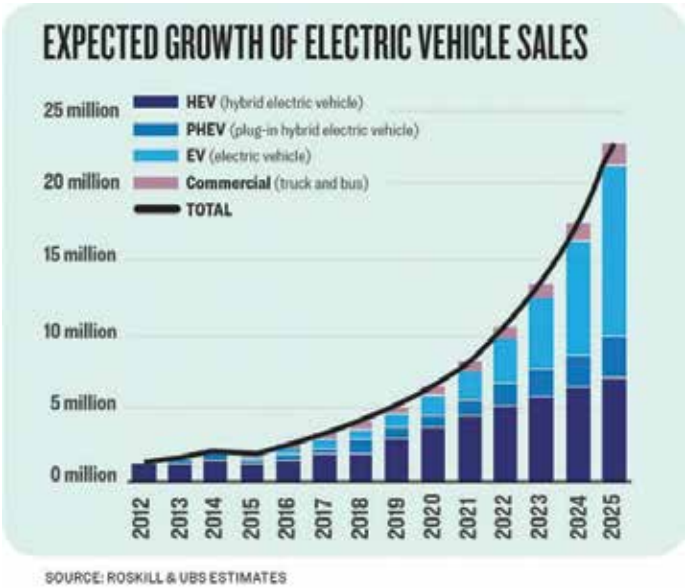

Figure 2. Expected growth of EV Sales.

3. SiC material and epitaxy progress

Figure 3 captures the rapid improvement in the density of micropipe defects in SiC 6-inch substrates. While 6-inch substrates dominate the cost of SiC products presently, the rapid capacity expansion by key suppliers in the USA, coupled with robust volume growth, is expected to bring cost parity with 4-inch mature SiC substrates by mid-2018. Beyond 2018, 6-in. SiC will drive cost reductions across all product types. Improvements in wafer shape, boule yields, and reduced defects are key to eventual device yields and lower costs. As with silicon technology, many quality improvements are possible only when the scale of the business allows large-scale manufacturing that brings clarity to underlying issues and drives equipment improvements and investments as manufacturers compete.

There has also been considerable progress in 6-in. epitaxy [4], along with the introduction of improved single-wafer tools and better metrology for defects. Post-epitaxy thickness uniformity ±8%, doping ±15%, and BPDs <0.1/cm^2 are available up to 1700 V. **Figure 4** shows the state-of-the-art 6-in. product yield on 200A, 650 V JBS diodes, a testament to the starting epi material quality married to Si foundry manufacturing discipline. **Figure 5** shows the rapid advancement in post-epitaxial wafer defect density.

Also significant is the introduction of the foundry model in SiC. Until SiC volumes grow to exceed 10–30 K wafers/month, the economics of a dedicated factory for wafer cost are not favorable, since the entire cost of running the fab must be amortized over a small

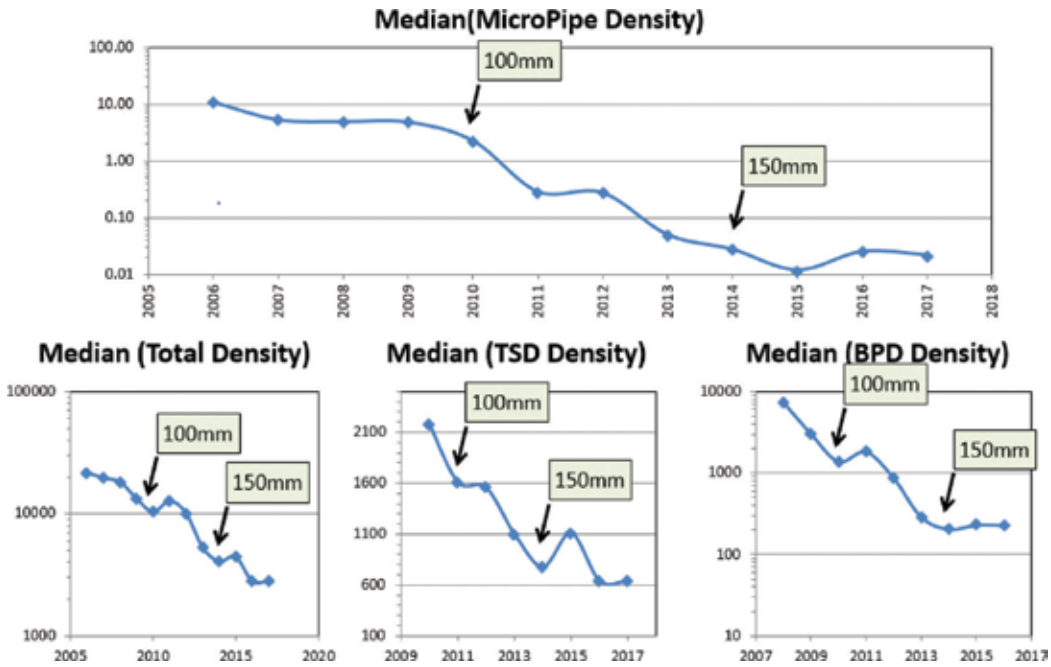

Figure 3. Improvement in SiC substrate quality over time. Courtesy: II-VI corporation.

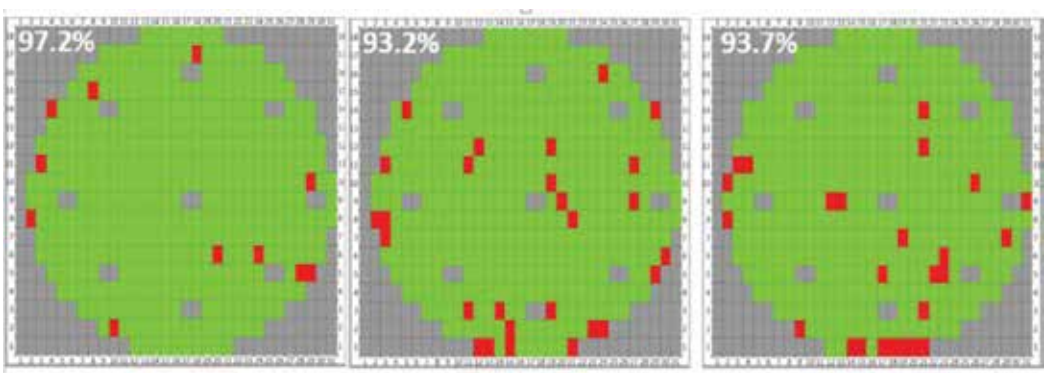

Figure 4. Yield on 6-inch 200A, 650 V JBS diodes. Courtesy: USCi 2017.

volume. Most large silicon manufacturers entering SiC try to leverage their silicon mass production lines. The transition to 6-in. makes this process easier, and an initial investment of $2–30 m is sufficient, since the majority of process steps can share equipment with silicon. The foundry model brings a high level of manufacturing expertise, low process cost from sharing the line with silicon, and the ability to aggregate SiC volume to further drive down prices.

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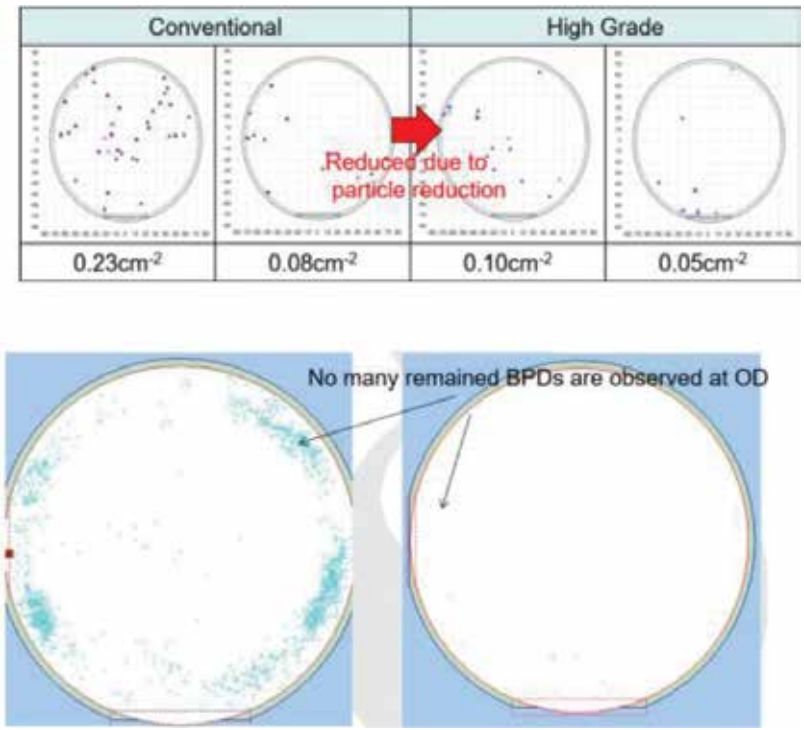

Figure 5. Rapid improvements in epitaxial layer defects. Courtesy: Showa Denko Corporation.

4. Device technology

Progress on device technology and products has been considerable in the last few years. The improvement in RdsA, reliability, chip current ratings, and improved knowledge on how to use the devices in new designs is now bearing fruit. Up to 100A, 1200 V, and 200A, 650 V single chip JBS diodes are now available, bringing SiC diode ratings to silicon soft-recovery diode levels. The improvements in Eon losses by 2× at 150°C through the use of these diodes lead to large loss reduction for hybrid SiC modules even at modest switching frequencies.

In the SiC transistor space, the main device structures in use are shown in **Figure 6**. Trench MOSFET offerings from Rohm and Infineon [5] compete with advanced planar technologies from Wolfspeed, Panasonic [6], Mitsubishi, ST, and GE. Evolution of trench technology is expected to continue the RdsA improvement of SiC MOSFETs, since mobility is improved along the a- and m-faces. Cascode technology from USCi based on trench JFETs provides the lowest RdsA technology SiC switch, configured as a normally-off MOSFET by cascode connection to a custom Si device, designed to present an IGBT/Si MOSFET interface to all users (**Figure 7**).

The use of advanced wafer thinning to reduce substrate resistance together with the dense trench JFET cell technology for SiC [7] has resulted in the introduction of 650 V cascode devices

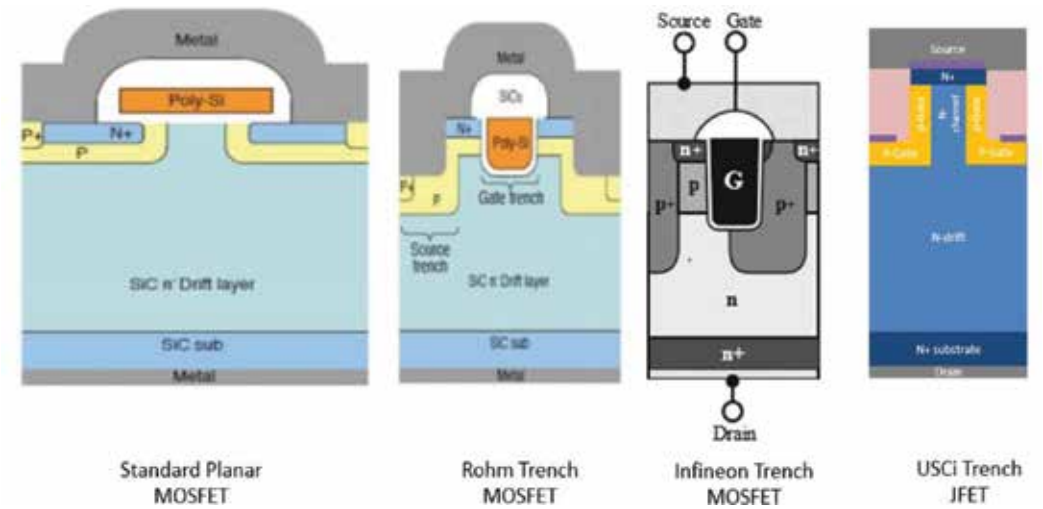

Figure 6. SiC transistor types aavilable in the 650–1200 V class 2016–2017.

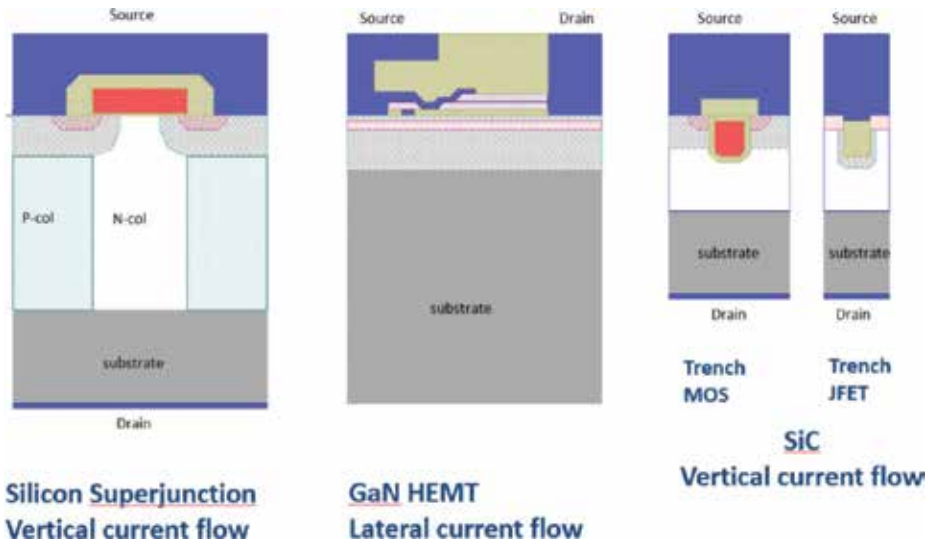

Figure 7. Comparison of transistor technology in the 650 V class 2016–2017.

from USCi that can complete very favorably with incumbent Si superjunction, GaN HEMT, and SiC MOS devices. **Table 1** shows the RdsA of commercially available 650 V devices, with SiC Cascodes providing >10× RdsA improvement over silicon devices, with obvious benefits in cost and lower capacitances. A key improvement with WBG devices is the improved body-diode with very low recovery losses that in turn allows the use of circuits such as totem-pole PFC to push efficiency to new heights. Thermal management for the smaller SiC chips is driving packaging technology enhancements, both in discrete devices and in power modules.

Development of 3300 V MOSFETs at 4 in. and 6 in. [8] indicates that commercial introduction from multiple suppliers may be expected in the next 1–2 years. The horizon for 6.5 kV- and

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Technology	SiC Cascode 650V-45mΩ (UJC6505K)	Commercial SiC MOSFET	Commercial GaN HEMT	Commercial Si Superjunction
R_{DSA}	0.75 mΩ-cm²	2-3 mΩ-cm²	3-7 mΩ-cm²	10 mΩ-cm²
Normalized Die Area	1	2.6X	4X	13X
E_{OSS}	7.5 μJ	32 μJ	12 μJ	14 μJ
Avalanche Capability	YES	YES	NO	YES
Short Circuit	YES	YES	NO	YES

Table 1. Comparative performance of advanced 650 V devices in 2016–2017.

10 kV-rated modules is longer, and the supercascode structure [9] is a very promising alternative, with large benefits in switching speed, diode recovery, and drive simplification as attractive cost points.

5. Reliability

Much has been reported in the last 3–4 years on the rapid improvements in the understanding of the MOS interface in SiC [10]. This has led to much reduced Vth shift in commercial products from leading manufacturers. In addition, the trench MOSFET structure allows the use of thicker gate oxides for better reliability margins, given the better mobility observed on the a- and m-faces of SiC. Progress has been made ensuring the reliability of SiC transistors and diodes to combined moisture and field-dependent degradations by the introduction of devices that can withstand 1000htrs of H3TRB stress at 80% of the rated $V_{DS(MAX)}$. A working group under JEDEC JC-70 is formalizing improved standards for SiC MOSFET testing and qualification, based on the deeper understanding of failure modes and interface physics. In addition, great strides have been made in understanding and mitigating BPD-dependent degradation mechanisms [11]. Most gate oxide issues are not a matter of concern in the cascode structure, since the SiC JFET device has no gate oxide and can therefore operate at higher bulk E-fields without degradation. Furthermore, the Si MOS used in the cascode has a high Vth and a thicker gate oxide, which leads to greater margin between operating and maximum ratings.

SiC MOSFETs and cascodes offer excellent avalanche ratings. SiC devices are also able to withstand repetitive avalanche events, and studies on cascodes have shown that 1E6 cycles at the rated datasheet EAS condition result in no-device degradation, since current flow is in the bulk SiC.

Figure 8 shows a UJC1206K cascode device tested for short-circuit withstand time at starting Tj = 25 and 200°C at Vds = 850 V. The datasheet conditions for SCWT are met for all operating gate voltages and even with Tj = 200°C since the SiC JFET limits the short-circuit current

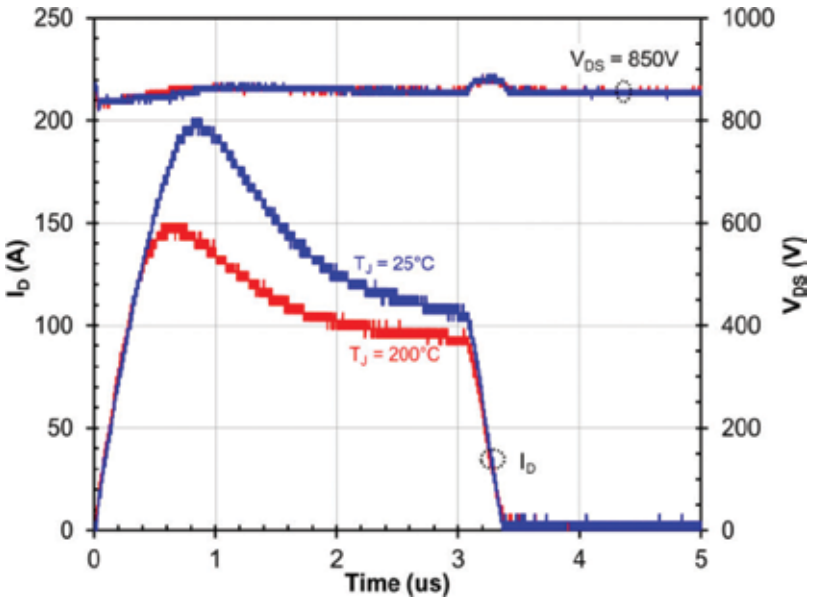

Figure 8. UJC1206K cascode device is capable of handling repetitive short circuits even with starting Tj=200°C. SiC devices will offer robustness exceeding Si IGBTs.

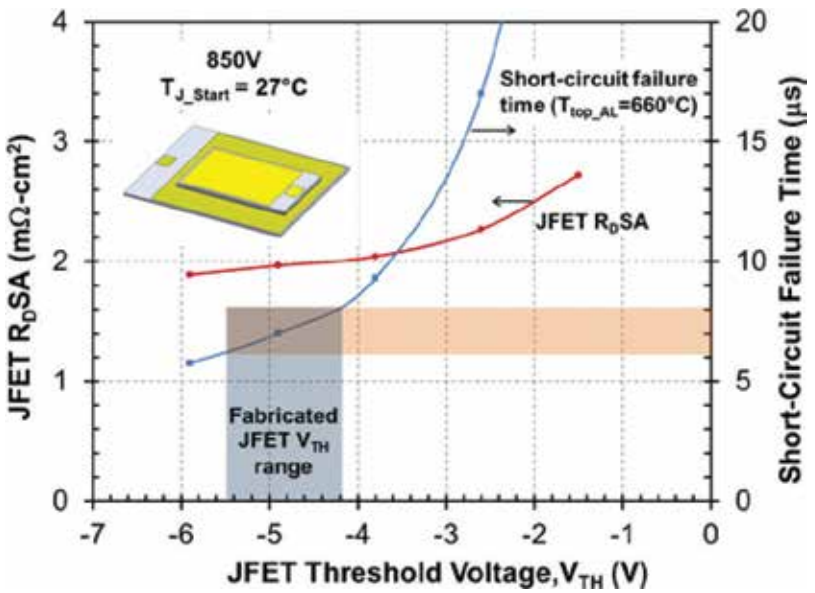

Figure 9. Short circuit time-RdsA trade-off for 1200V Stack cascode with Vbus = 850V. Courtesy USCi 2017.

within the cascode. A study of the 650/1200 V USCi cascodes undergoing 100 repetitions at the rated short-circuit conditions shows no degradation in any device characteristics, whereas SiC MOSFETs typical undergo Vth shifts after such exposure [12]. The trade-off in RdsA to get long

short-circuit withstand times in the cascode is favorable compared to SiC MOSFETs, since the reduction in peak current by tuning JFET Vth does not drastically increase RdsA. **Figure 9** shows that a short-circuit withstand time of 10 μs can be achieved with minimal change in JFET RdsA.

Recent studies of SiC devices have shown better immunity to terrestrial neutron radiation, which is a key problem for high-voltage IGBTs. Much work remains to be done, however, to improve the immunity of heavy ions that affect device operations in space. NASA has led the research into ultra-high temperature operation (500°C-long duration) of SiC JFET devices and ICs, in understanding the degradation mechanisms. At this time, these applications are niche but hold the potential to unlock entirely new businesses for SiC.

6. SiC gate drive

The last few years have also marked the rapid proliferation of gate drive solutions suitable for use for SiC power MOSFETs, with the extended voltage range and strong sink currents. Non-isolated drivers for use with signal isolators, or isolated drivers from multiple vendors, are available, with common mode transient immunity of 100–200 V/ns. However, many more options exist for the better developed ecosystem of Si MOSFET and IGBT drives, which can be used with SiC cascode devices, easing the transition to the use of WBG switches. **Figure 10** shows an important benefit of SiC cascode devices, which cannot only be dropped into Si IGBT/MOSFET circuits but also offer a larger margin between operating and maximum gate voltages, as is prevalent for incumbent silicon devices.

Figure 11 shows a schematic for the gate drive interfaced with a half-bridge connection of two SiC transistors. When the upper device is turned on, the voltage rises across the lower device once its body diode recovers. This fast dV/dt can induce a voltage spike at the gate, due to the Igd displacement current (proportional to C_{gd}.dV/dt), turning-on the lower device, creating a brief shoot-through condition where both transistors are on. This can be avoided by having a low Cgd/Ciss ratio, low internal Rg in the transistor, and a gate driver with a strong current sink or a Miller clamp. Similarly, if the gate driver power supply or the signal barrier allows capacitive coupling between the input and output, injected displacement currents during high dV/dt operations can cause misoperation of the signal processing electronics. Advanced solutions are now available to handle these issues from many analog IC companies (see **Table 2**).

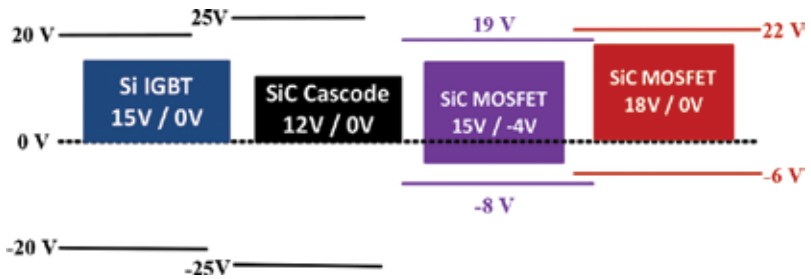

Figure 10. Operating and maximum gate voltages for Si IGBT, SiC cascode, and SiC MOSFET switches.

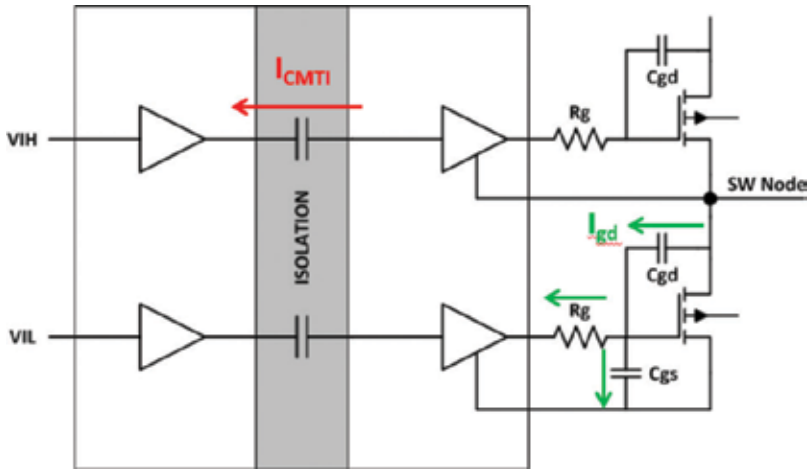

Figure 11. The key challenges of high dV/dt switching is to have gate drivers with strong current sink capability, dV/dt immunity and an isolation barrier with high common mode rejection.

Non isolated single drivers

Manufacturer	Part Num.	Vo range (V)	Source (A)	Sink (A)	Isolation
TI	UCC27531-Q1	10 to 35	2.5	5	No
Microchip	MIC4479YME-TR	4.5 to 32	2.5	2.5	No
IXYS	IXDN609SI	4.5 to 35	9	9	No
Infineon	IR4426SPBF	5 to 20	2.3	3.3	No

Isolated drivers

Manufacturer	Part Num.	Vo range (V)	Source / Sink (A)	Short Circuit Protection	Isolation (Vrms)	CMTI (kV/µs)
Analog Devices	ADuM4120-1	4.5-35	2.3 / 2.3	No	5000	150
Texas Instruments	ISO5852S	15-30	2.5 / 5	Yes	5700	100
Silicon Labs	SI8275	4.2-30	1.8 / 4	No	3000	200
Infineon	1EDI60N12AF	10 to 35	9.4 / 10	No	1200	100

Silicon Labs: SI8275 is a half bridge.

Table 2. A selection of gate drivers for SiC devices and key characteristics.

7. Packaging for SiC

It has been clear since the early days of SiC transistor technology that the high temperature and fast switching capability of SiC switches could not be exploited without the use of low-inductance packaging. However, the initial introduction of discrete devices has used traditional silicon through-hole packages like TO247-3L. Very recently, the range of discrete

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package offerings has been expanded to include the TO247-4L and D2PAK-7L, where the source Kelvin connection allows faster di/dt switching without excessive gate ringing. With the entry of 650 V SiC switches, in the near future, we can expect additional Si packages like the DFN8x8, TOLL, DPAK-3L, and D2PAK-3L to follow. As frequencies rise further, requiring switching at >200 V/ns, use of co-packaged half-bridge elements, as well as co-packaged drivers is planned to replace standard discretes.

Module packaging based on IPM technology is already offered by Mitsubishi, Fuji, and others. Automotive grade IPMs with built-in gate drives minimize losses for higher frequency switching and can serve the 8–25 kW space quite well for power supplies and on-board chargers, albeit at a cost premium.

The potential for hybrid modules has been thoroughly examined, but the expanding offerings of full SiC modules will likely see more growth. While few modules offer Tjmax >175°C today, considerable improvements have been made in inductance, to allow fast switching. **Figure 12**

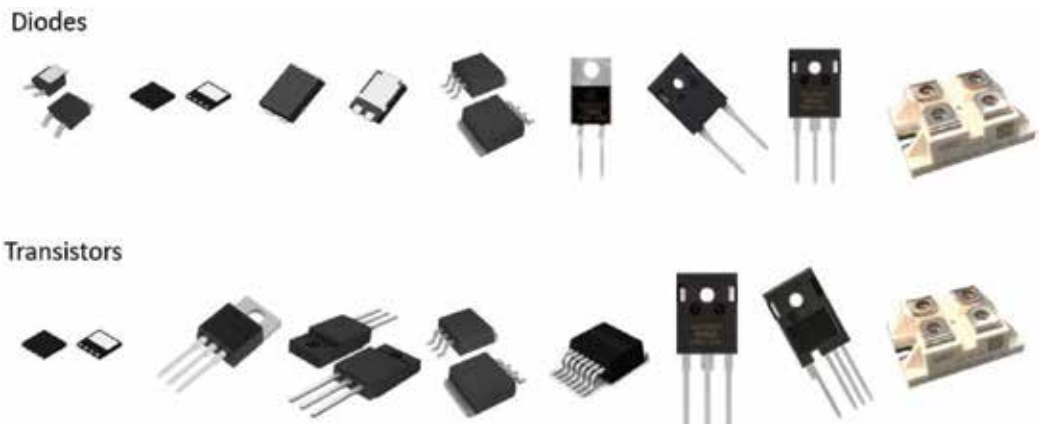

Figure 12. A wide-array of discrete surface mount and thorugh hole packages have become available for discrete SiC devices. For high-speed switching, packages that provide a separate source Kelvin connection are beneficial.

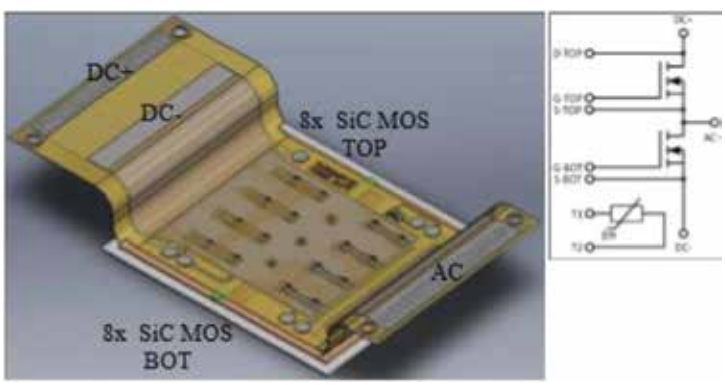

Figure 13. A 400, 1200V half-bridge module with 1.4nH power loop inductance presented by Semikron. Packaging of this type can allow the full use of the high frequency switching benefits of SiC at high power levels.

shows a recent Semikron development that cuts loop inductance to just 1.4 nH in a 400 A, 1200 V half-bridge [13], allowing very fast switching without excessive voltage overshoots and good current sharing. These packaging innovations are key to unlocking the system-level benefits of SiC (**Figures 13** and **14**).

In the automotive space, considerable effort has been expended on double-sided cooling. This technology is already used for Si IGBTs by many car manufacturers and is being actively developed for SiC as well [14]. While the CTE difference between Si and SiC is small, the much higher Young's modulus of SiC leads to higher stresses, requiring careful mechanical package development, especially for double sided cooling extended to 175–200°C temperature ratings.

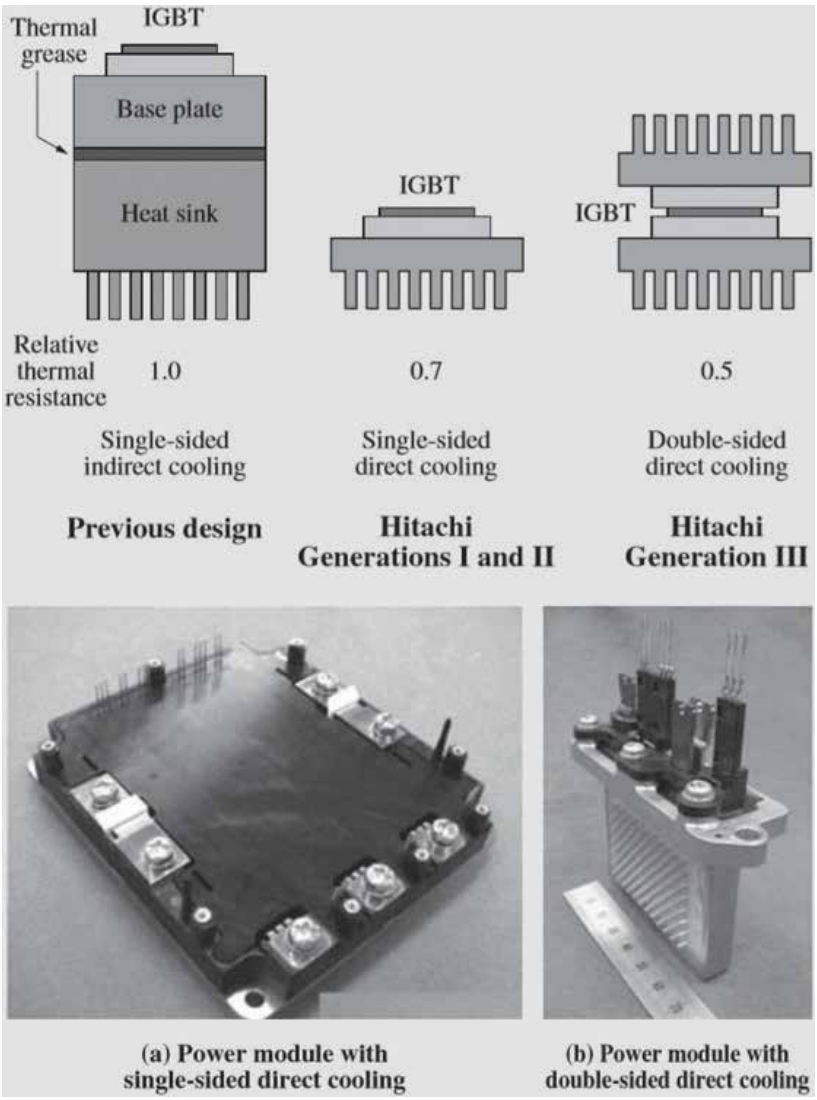

Figure 14. Double-sided cooling technologies developed for silicon IGBTs will be rapidly adapted to SiC MOSFETs.

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8. Application drivers

A roadmap of applications for SiC devices was compiled by the PowerAmerica Institute and described in terms of voltage class and whether they are near, medium, or long term, as shown in **Figure 15**. It can be seen that the near-term applications fall in the 650–1700 V range.

The benefits of SiC Schottky diodes in reducing CCM mode E_{ON} losses in PFC circuits that led to the widespread use of these devices in the last decade continue today. However, the drive to

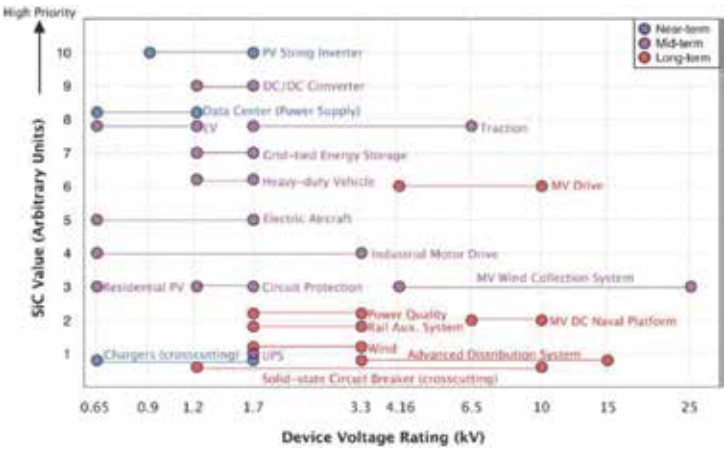

Figure 15. Applications roadmap for SiC devices by voltage rating. Courtesy: PowerAmerica.

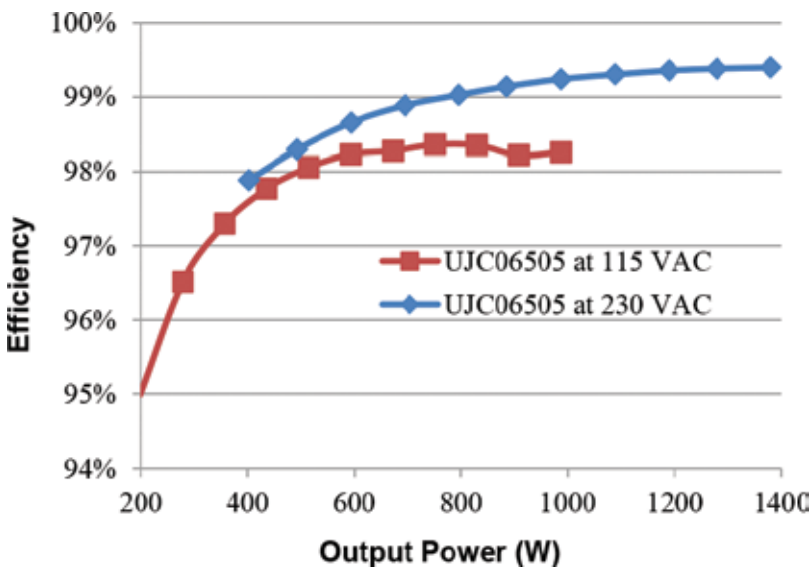

Figure 16. >99% Efficiency on Totem pole Demonstration board with UJC06505K.

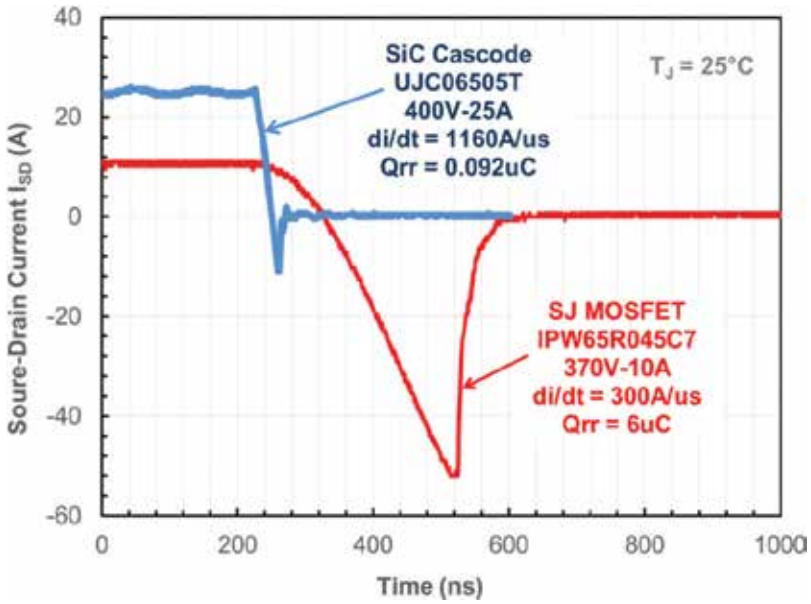

Figure 17. Excellent Qrr for UJC06505K enables hard switching. Low Qrr body diode behavior is a key benefit of SiC MOSFETs and GaN devices over silicon superjunction devices.

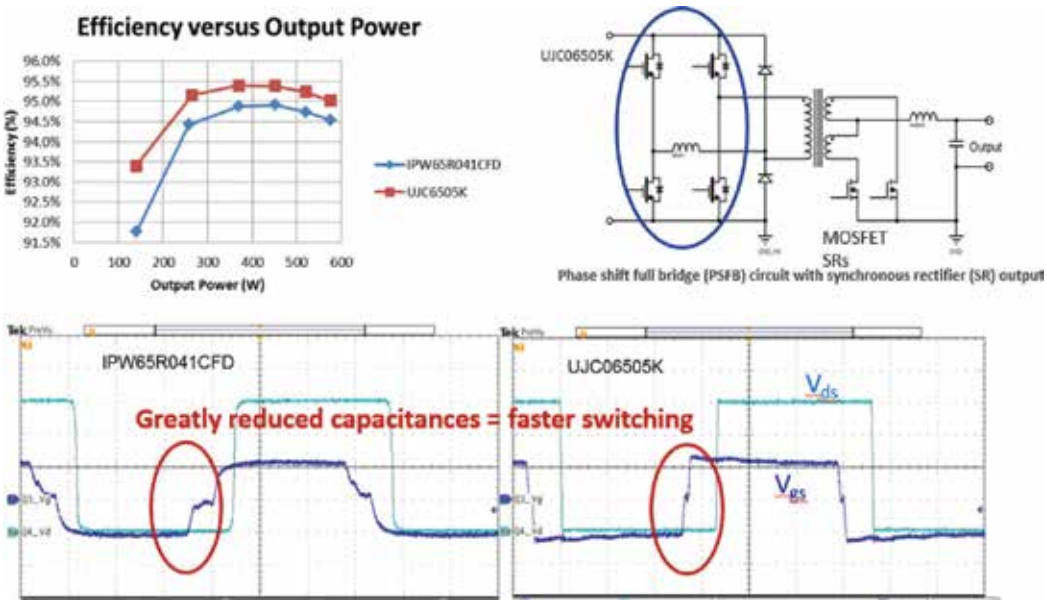

Figure 18. Phase shift full-bridge using SiC cascodes UJC06505K with low capacitances, driven by simple pulse-transformer gate drives at 75kHz. Efficiency benefits at standard operating frequencies are also enabled by SiC.

Figure 19. A 200KW full-SiC converter presented by Fraunhofer. The converter achieves an impressive power density >100W/cm^3 switching at 200kHz, with an efficiency of 98.9%.

eliminate bridge losses [15] has led to the development of the Totem-pole PFC topology. To use this bridgeless circuit in CCM mode, the device required must feature very low-diode recovery losses in addition to basic fast switching capability. **Figure 16** shows the efficiency achieved in a Totem-Pole PFC, and **Figure 17** shows the excellent body diode recovery behavior that makes this possible. For this reason, 650 V SiC devices are likely to compete with GaN devices at >1.5 kW level of server/telecom supplies that require >99% PFC stage efficiency at high frequencies. This lack of diode recovery charge also makes the SiC-based switches useful in avoiding recovery-induced failures in PSFB and LLC applications when ZVS conditions are temporarily lost.

The rapid adoption of 1200 V SiC MOSFET and cascode devices in the charger market for forklifts and vehicle bidirectional on-board chargers can be easily understood based on the very high efficiency achieved with phase-shift full-bridge topology, that benefit from the low conduction and turn-off loss and from the low Coss and Qrr at light loads. **Figure 18** shows the PSFB efficiency and the waveforms resulting from the low capacitance of the SiC devices compared to incumbent superjunction devices. **Figure 19** shows an excellent demonstration of the power density improvements possible with SiC 1200 V switches for high-power conversion applications, needed on space constrained environments like EVs.

9. Conclusion and outlook

The long wait for SiC to reach a tipping point appears to be nearing its end. This is due to steady progress on every front needed to realize large-scale adoption, from the maturation of 6-in. SiC material and a deep understanding of SiC defects to improved, easy-to-use devices with a growing reliability track record. An ecosystem of excellent gate drivers makes design simpler, and improved discrete, IPM, and module packages have become available to allow

the exploitation of the faster switching capability of SiC. These benefits have allowed users to apply circuits previously not possible with Si devices, and this is fueling the growth in the power supply and on-board charger area. With the type of capability now demonstrated with commercial products, there is little doubt that expansion to the automotive inverter will further accelerate the ramp by the early 2020s.

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Chapter 6

GaN-Based Schottky Diode

Yaqi Wang

Additional information is available at the end of the chapter

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Abstract

Schottky diode, also known as Schottky barrier diode (SBD), fabricated on GaN and related III-Nitride materials has been researched intensively and extensively for the past two decades. This chapter reviews the property of GaN material, the advantage of GaN-based SBD, and the Schottky contact to GaN including current transporation theory, Schottky material selection, contact quality and thermal stability. The chapter also discusses about the GaN lateral, quasi-vertical and vertical SBDs, and AlGaN/GaN field effect SBDs: the evolution of the epitaxial structure, processing techniques and device structure. The chapter closes with challenges ahead and gives an outlook on the future development of the GaN SBDs.

Keywords: GaN, AlN, AlGaN, Schottky diode, Schottky barrier diode (SBD), Schottky contact

1. Introduction

Wide band gap (WBG) semiconductor materials are the best candidates for high frequency, high power and high temperature applications because of their superior intrinsic material properties compared to Si, and GaAs (**Table 1**).

Among the WBG materials, SiC and GaN are the most successfully developed in terms of material growth, device fabrication and commercialization. GaN and related III-Nitride materials such as InN and AlN and their alloys have many advantages in optoelectronics. III-Nitride materials have a wide range of direct bandgap from the lower end 1.9 eV (InN) to the high end 6.2 eV (AlN) and can also support multi-quantum well and superlattice structures, enabled by epitaxial thin-film growth technology, primarily metal organic chemical vapor deposition (MOCVD). GaN and AlGaN are also the preferred WBG materials in high

Parameter	Si	GaAs	4H-SiC	GaN
E_g (eV)	1.12	1.42	3.25	3.40
E_c (MV/cm)	0.3	0.4	3.0	4.0
μ_n ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	1500	8500	1000	1250
ε	11.8	12.8	9.7	9.0
V_{sat} (10^7 cm/s)	1	2	2	2.5
λ ($W \cdot cm^{-1} \cdot K^{-1}$)	1.5	0.5	4.9	2.3

E_g: bandgap; E_c: critical electric field; μ_n: electron mobility; ε: dielectric constant; V_{sat}: saturation electron velocity; λ: thermal conductivity.

Table 1. Comparison of material properties of Si, GaAs, 4H-SiC and GaN [1].

frequency applications as two-dimensional electron gas (2DEG) with high carrier concentration and mobility can be formed at the AlGaN/GaN heterointerface by spontaneous and piezoelectric polarization effect [2]. GaN based light emitting diode (LED), GaN based laser diode (LD) and AlGaN/GaN based high-electron-mobility transistor (HEMT) were commercialized in early 1990s, late 1990s and mid 2000s respectively.

In the realm of high power and high temperature applications, as Si based power device is reaching its theoretical limit and cannot meet the increasing demand of key performance metrics, such as high blocking voltage, low switching loss, high switching speed and high operating temperature at the same time, WBG materials has great potential to replace Si in those applications [3].

Specifically, in applications that require high reverse blocking voltage and high switching frequency, SiC and GaN Schottky barrier diodes (SBDs) are preferred over bipolar Si p-i-n diode, whose switching speed is compromised due to long minority carrier lifetime. SiC and GaN are comparable in many aspects: GaN has higher Baliga's figure of merit (BFoM) because of its better electrical properties, while SiC has better thermal conductivity, thus the two materials are in direct competition for the application [4]. SiC SBD was successfully introduced to the market in early 2000s, and gradually matured to displace the Si p-i-n diode. On the other hand, because of the nonoptimal material quality, which once limited the application of its SiC counterpart, GaN SBD still cannot achieve its theoretical performance. Researchers around the world have been continuously working on improving GaN material quality, while exploring novel ways to fabricate GaN SBD with better performance since mid-1990s. Although great progress has been made, significant amount of effort is still need for GaN SBD to overcome the technical challenges, close its performance gap to SiC SBD, and eventually achieve commercial success.

In the following sections of this chapter, several topics are discussed in details:

- *Schottky contacts to GaN*: Theoretical basis, current transportation mechanisms, characterization methods, metal selection and comparison, the impact to contact performance by material and surface quality, and thermal stability of Schottky contact to GaN were

discussed sequentially in this section. The section also covers topics such as nonmetal Schottky contact to GaN, Schottky contact to AlGaN, and Schottky contact to nonpolar GaN.

- *GaN lateral, quasi-vertical and vertical SBDs*: This section covers material growth and epitaxial structure optimization techniques, device fabrication and device structure optimization techniques such as: surface treatment, dielectric deposition, floating metal ring, field plate, ion implanted guard ring and Schottky junction barrier diode.
- *AlGaN/GaN field effect SBDs*: This section discusses about AlGaN/GaN heterojunction formation, material growth and epitaxial structure optimization techniques, device fabrication and device structure optimization techniques that are unique to AlGaN/GaN field effect Schottky barrier diodes such as: dual Schottky anode, Schottky-ohmic-combined anode, gated edge termination, fully recessed Schottky anode and MIS-gated hybrid anode.

A brief summary and outlook on GaN SBD development are presented in the last section.

2. Schottky contacts to GaN

2.1. Theoretical basis of Schottky contact to GaN

Metal–semiconductor contact plays a crucial role in semiconductor devices, such as diodes and transistors. There are two types of metal-semiconductor contact: Ohmic and Schottky. Schottky contact has a rectifying barrier, which is formed when there is an energy level mismatch between the semiconductor and the metal. The difference between the semiconductor electron affinity and metal work function is defined as Schottky barrier height. The band structure before and after Schottky contact formation to n-type semiconductor, such as intrinsic GaN, is shown in **Figure 1**. Fermi levels of the metal and semiconductor need to line up to reach an equilibrium when they are put in contact, and the space charge built at the semiconductor side leads to band bending effect.

There are two carrier transportation mechanisms for an ideal Schottky contact: thermionic emission (TE) and field emission (FE). At a forward bias, the carrier transportation is determined by temperature and the n doping concentration of GaN. A lower temperature and a more highly doped GaN can lead to a higher FE component. As Schottky contact is usually deposited on intrinsic GaN or lightly n doped GaN, and the operation temperature of GaN SBD is usually above room temperature, the dominant transportation mechanism is TE. The current-voltage characteristics of the SBD in the TE regime is given by Eq. (1, 2):

$$\mathrm{I} = \mathrm{I}_0\left\{\exp\left[\frac{q(V - IR_s)}{nkT}\right] - 1\right\} \tag{1}$$

where I_0 is the saturation current:

$$I_0 = AA^*T^2 \exp\left(\frac{-q\Phi_B}{kT}\right) \quad (2)$$

The three most common Schottky contact characterization methods are current-voltage (IV), current-voltage-temperature (I-V-T) and capacitance-voltage (C-V). Key parameters, such as Schottky barrier height (Φ_B), ideality factor (n), effective Richardson's constant (A^*), doping concentration (N_D) and series resistance (R_s) can be extracted from the characterization methods mentioned above.

2.2. Metal Schottky contacts to GaN

Tremendous amount of work on Schottky contacts to GaN was done in mid 1990s, which built solid foundation for later development of vertical and lateral GaN SBDs. Au Schottky contact to n-GaN was first reported by Hacke et al. [5] and Khan et al. [6]. Schottky contact formation of Ni, Pd and Pt to GaN was then extensively studied by various research groups [7–12]. I-V, I-V-T and C-V measurements were performed to find the characteristics of the Schottky contacts, such as ideality factor, effective Richardson coefficient, and Schottky barrier height. **Table 2** shows a brief summary of Schottky barrier heights of common contact metals by the three methods mentioned above.

Liu and Lau reviewed the scattered results reported and suggested the nonideal Schottky contact behavior probably stemmed from surface defect which can cause inhomogeneity in the transport current even within a single device, while material quality and metal-GaN reactions were the other two contributing factors [13]. Hsu et al. performed scanning current–voltage microscopy (SIVM) measurements and found nonuniform spatial reverse leakage distribution within a device. The correlation of SIVM, topographical and TEM images showed that leakage occurred at screw and mixed dislocation [14]. The experiment confirmed surface and material quality is crucial to good Schottky contact formation.

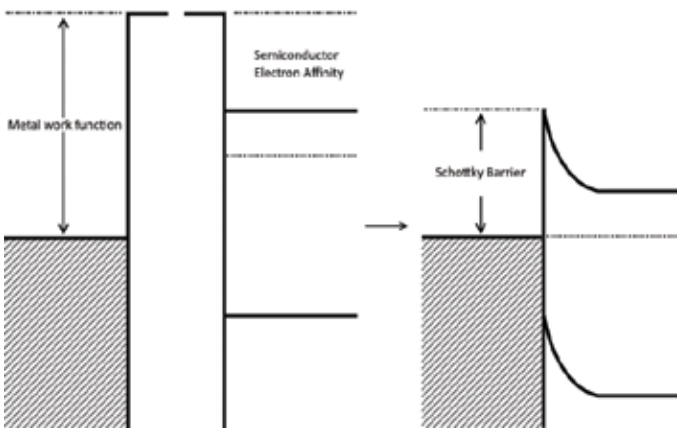

Figure 1. Band structure of Schottky barrier formation [1].

Metal	Φ_b (eV) by I-V	Φ_b (eV) by I-V-T	Φ_b (eV) by C-V	Reported
Au	0.844	—	0.94	Hacke et al. [5]
	0.91	—	1.01	Khan et al. [6]
	1.03	—	1.03	Kalinina et al. [9]
	0.87	0.88	0.98	Ping et al. [10]
				Schmitz et al. [11]
Ni	1.15	—	1.11	Kalinina et al. [9]
	0.95	0.99	1.13	Schmitz et al. [11]
	0.83	0.93	1.03	Liu et al. [12]
Pd	—	0.91	0.94	Guo et al. [7]
	1.11	0.96	1.24	Wang et al. [8]
	0.94	0.92	1.07	Ping et al. [10]
				Schmitz et al. [11]
Pt	—	1.03	1.04	Guo et al. [7]
	1.13	—	1.27	Wang et al. [8]
	1.01	1.08	1.16	Schmitz et al. [11]

Table 2. Summary of Schottky barrier height of Au, Ni, Pd, and Pt to GaN from I-V, I-V-T, and C-V experiment results.

Miller et al. designed an experiment to detect localized leakage path on GaN surface by conductive atomic force microscope (AFM), and developed a surface modification method by selectively applying voltage at the recorded leakage locations to form a thin passivation layer that blocks the leakage path. Schottky contact made on surface modified GaN showed much better reverse leakage characteristics than unmodified GaN [15]. Sang et al. performed detailed analysis on leakage path by photon emission microscopy (PEM), and found the leakage current occurred at polygonal pits, where carbon impurity accumulated and acted as trap in carrier tunneling [16]. The result aligned with the Cao et al.'s finding that low carbon concentration was necessary to achieve high Schottky contact quality, by an experiment correlating contact performance with carbon doping level [17]. Reddy et al. demonstrated a homogeneous Schottky contact to GaN with unity ideality factor and low leakage current by acid treatment. XPS studies showed the treatment removed excess carbon and restored Ga/N composition at the interface [18]. It can be concluded that removal of impurities such as carbon, and/or passivation of leakage path by surface treatment, is effective in improving Schottky contact quality.

Schottky contact thermal stability is important to GaN SBDs, as high operating temperature is desired for power applications. At elevated temperature, Schottky metal reacts with GaN, gradually turning the contact nonrectifying. Guo et al. reported Ni Schottky contact started to react with GaN, forming nickel nitrides, at temperature above 200°C [19]. For noble metal Pd, interdiffusion of the metal and GaN was discovered at 300°C [20]. If stable temperature is defined as temperature at which Schottky contact is still rectifying after 1 hour of annealing,

the highest stable temperature for Ni and Pt was reported to be 500°C [12] and 400°C [21], respectively. Several techniques were applied to improve stability of Schottky contact to GaN. Thermal stability of metal silicide is usually better than elemental metal. The stable temperature was reported to be 600°C for NiSi [12] and PtSi [21], 100–200°C higher than elemental Ni and Pt. Multilayer contact structure with inert and high melting point metal as insert or cap layers can also help to improve the thermal stability of Schottky contact. Stable temperature of Ni/Ta bilayer Schottky contact was reported to be 700°C [22], 200°C higher than pure Ni.

2.3. Nonmetallic Schottky contacts to GaN

ITO and graphene Schottky contacts to GaN were also studied, as they are transparent and have potential applications in optoelectronic devices such as MSM photodetector. Sheu et al. reported ITO Schottky contact to GaN with increasing barrier height from 0.68 eV as deposited to 0.95 eV after annealed at 600°C [23]. Tongay et al. first reported graphene and multilayer graphene (MLG) Schottky contact, with barrier height of 0.74 eV as deposited and 0.70 eV after prolonged annealing at ~ 600°C [24]. The large ideality factor (>2) indicated high contact inhomogeneity. Kim et al. reported improved graphene Schottky contact with 0.9 eV barrier height and 1.32 ideality factor [25].

2.4. Schottky contacts to AlGaN

Schottky contacts need to be made to AlGaN in some AlGaN/GaN field effect SBD applications. Qiao et al. characterized Ni Schottky contact to AlGaN by I-V, C-V and photoemission methods, and found the barrier height increased linearly with Al mole fraction up to 0.23 [26]. Lv et al. applied two-diode model and determined barrier height of Ni Schottky contact to AlGaN/GaN heterostructures by forward I-V measurement [27]. Shin et al. investigated common GaN Schottky metals, such as Au, Ni, Pd and Pt, to AlGaN/GaN heterostructures and found barrier inhomogeneity was related with Schottky metal type [28]. Nonmetallic materials such as TiN was also studied. TiN can be deposited to AlGaN surface by reactive sputtering [29]. The lower barrier height of TiN compared to common Schottky metals enables a lower turn-on voltage, which is preferred in application such as microwave rectification [30].

2.5. Schottky contacts to nonpolar GaN

Schottky contacts made to a-plane and m-plane nonpolar GaN were also studied. Phark et al. studied Pt Schottky contacts to a-plane n-GaN [31]. Yamada et al. fabricated Ni Schottky diode on m-plane n-GaN [32], and compared with the Schottky diode with same structure fabricated on c-plane [33]. Although the carbon concentration of the m-plane GaN was much less than c-plan GaN, the reverse leakage was three orders of magnitude larger due to lower barrier height. To date, it still remains unclear whether c-plane or nonpolar GaN is preferred in Schottky diode application mainly because nonpolar GaN Schottky devices were much less frequently investigated [34].

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3. GaN lateral, quasi-vertical, and vertical SBDs

The extensive study of Schottky contacts to GaN enabled the development of high breakdown GaN SBDs in late 1990s. GaN based SBDs have three common structures: lateral, quasi-vertical and vertical. **Figure 2** shows the schematics of the three structures. Lateral and quasi-vertical SBDs are usually fabricated on GaN grown on a foreign substrate, such as sapphire, SiC and Si. For lateral SBD, Schottky contact and ohmic contact are on the same surface. For quasi-vertical SBDs, a mesa is etched first, followed by ohmic contact deposition on the etched GaN and Schottky contact deposition on top of mesa. Vertical SBDs are usually fabricated on freestanding GaN substrate by depositing ohmic contact on the nitride face and Schottky contact on the gallium face. Lateral SBDs are easy to fabricate and thus are still used as development vehicles for testing new material growth and device processing methods, while quasi-vertical and vertical structures are preferred for practical applications.

3.1. GaN substrate growth and epitaxial structure optimization

Hydride vapor phase epitaxy (HVPE), molecular beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD) are the three most common methods for substrate growth. The GaN thickness, doping level are critical to SBD performance. While a design with a thinner and more highly doped GaN can lead to better on-state resistance and lower turn-on voltage, it has negative impact on breakdown voltage. The ideal substrate for GaN SBD shall have a gradient doping profile, with low dopant concentration on the Schottky side, and high dopant concentration on the ohmic side. However, such structure cannot be well supported by the current GaN material growth technology.

Quasi-vertical and vertical GaN SBDs are usually fabricated on substrates with layer structure, which has a lightly doped GaN drift layer on top of a highly doped low resistivity GaN layer, where Schottky contact and ohmic contact are formed, respectively. The layer structure has been developed on various substrate types. Sheu et al. reported a very thin low-temperate-grown (LTG) cap layer can greatly suppress reverse leakage current [35]. The layer structure consisted of a 30 nm LTG GaN cap layer, a 0.6 μm thick intrinsic GaN layer and a 1 μm thick highly doped GaN layer, grown by MOCVD on sapphire substrate. The highly doped and intrinsic GaN layers were grown at 1060°C, while the LTG GaN cap layer was grown at 550°C.

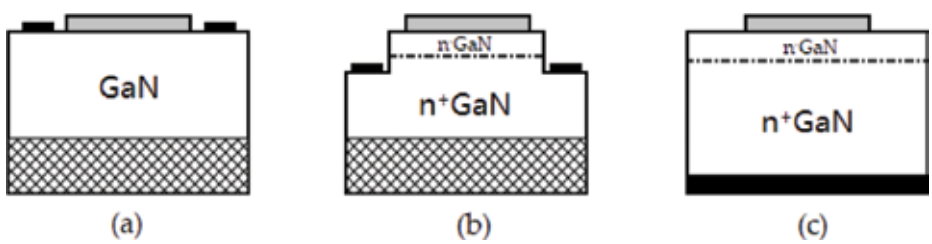

Figure 2. Schematics of (a) lateral, (b) quasi-vertical, and (c) vertical SBDs on GaN: the gray region is Schottky contact, black region is ohmic contact and the grid region is substrate.

Lu et al. reported a method to regrow GaN epitaxial layers by MOCVD on HVPE grown low resistivity freestanding GaN substrate. The layer structure has a 2 μm thick lightly doped GaN lay on a 0.5 μm thick highly doped GaN layer. It was reported that the structure greatly reduced the on-state resistance [36]. Fu et al. made further improvement to MOCVD regrown drift layers on HVPE substrate by introducing double-drift-layer (DDL) design [37]. An additional moderately doped GaN layer was inserted in between the lightly doped top layer and the highly doped bottom layer. It was demonstrated the breakdown voltage was improved with DDL design, while the forward characteristics was not compromised. The DDL design is much close to the ideal structure mentioned above. Cao et al. introduced a graded AlN cap layer on top of the GaN drift layer [38]. The cap layer has a thickness of 5 nm with Al composition from 0–23%. It was reported the cap layer reduced the leakage current by three orders of magnitude and the turn-on voltage from 0.77 to 0.67 V from tunneling effect.

3.2. SBD device fabrication and device structure optimization

The theoretical limit of the key parameters of GaN SBDs, such as breakdown voltage etc., are determined by the substrate structure. However, the SBDs performance reported is still far from the theoretical limit. Premature breakdown and high reverse leakage are the two main major areas that can be improved by better device processing and structure. Surface treatment, dielectric deposition, floating metal ring, field plate, ion implanted guard ring and Schottky junction barrier diode are discussed below.

Mesa etch is a necessary step for quasi-vertical GaN SBD fabrication. The mesa wall quality after etching can greatly affect the breakdown voltage and reverse leakage of the SBD. Surface treatment after mesa etching or material growth is critical for device performance. Bandić et al. first fabricated high breakdown voltage (450 V) lateral and quasi-vertical SBDs using Au as Schottky contact metal. The substrates used in the study consisted of an 8–10 μm GaN drift layer on a very thin (<100 nm) n^+ layer, and were grown by hydride vapor phase epitaxy (HVPE) on sapphire [39]. High leakage current was observed on quasi-vertical SBD structure due to plasma etch damage on mesa wall. Cao et al. explained the forms of plasma-induced damage to GaN as follows: generation of surface defects by ion, dopants passivation by atomic hydrogen, deposition of impurities and creation of nonstoichiometric surfaces [40]. The study also found a subsequent annealing at 750°C under N_2 or photoelectrochemical (PEC) etching in KOH solution to remove ~ 500–600 Å of the surface helped on the mesa wall quality improvement and leakage current reduction. Further study by Cao et al. suggested that the wet KOH etching is more effective than annealing for mesa wall treatment and diode characteristics restoration [41]. The GaN structures used in both studies were grown by RF plasma-assisted MBE on sapphire [40–41]. Zhu et al. fabricated quasi-vertical SBDs with mesa formed by both dry etching with a following KOH mesa wall treatment, and full wet PEC etching [42]. The GaN epitaxial structure with a 2 μm drift layer on top of a 1 μm n^+ GaN layer was grown by low-pressure MOCVD on sapphire substrate. Pt/Au was used as Schottky contact metal. The study demonstrated the device performance with wet-etched mesa is comparable or better than dry-etched. Spradlin et al. used molten KOH etching instead of PEC etching in KOH solution, and showed the molten KOH etching reduced the surface roughness and form etch

pits around defects [43]. The leakage characteristics was improved for SBDs fabricated on both MBE and HVPE grown GaN substrates. It can be concluded that surface treatment, with a variety of techniques such as annealing, PEC etching in KOH solution, and molten KOH etch, is very effective to improve the GaN SBD quality.

Dielectric layer deposition on drift layer top surface or mesa side wall can reduce the arcing effect, thus can improve the breakdown voltage of the GaN SBD. Most common dielectric materials used are SiO_2, SiN_x and Al_2O_3. The layer can be deposited by plasma-enhanced chemical vapor deposition (PECVD), RF sputtering and e-beam evaporation. In Zhu et al.'s work, a dielectric SiO_2 layer was deposited on the mesa wall by PECVD for passivation [42]. Float metal ring (FMR) technique uses an additional metal ring around Schottky contact to reduce electric field crowding at reverse bias. Two parameters: ring width and ring space, are critical to the FMR effectiveness. Schematics of FMR structure is shown in **Figure 3a**. GaN SBDs fabricated with FMR was first reported by Lee et al. A high breakdown voltage of 353 V was obtained on the SBD fabricated with FMR versus only 159 V without FMR [44]. The author also demonstrated the optimized structure by a design of experiment (DOE) with parameters ring width and ring space. Field plate (FP) incorporates both dielectric layer and metal overlay on top of dielectric layer to reduce electric field crowding. Dielectric layer thickness, metal overlay extent and dielectric permittivity are the three key parameters of FP. Schematics of FP structure is shown in **Figure 3b**. Bandić et al. first compared GaN lateral SBD with a field plate on sputtered SiO_2 dielectric layer and without field plate and found the field plate can suppress the leakage current by one to two orders of magnitude. Simulation was performed by Baik et al. to find the optimized FP structure [45]. A minimum metal overlay extent of 5 μm and a minimum dielectric layer thickness of 0.3 μm for SiNx was needed to avoid dielectric breakdown at the FP on GaN cap layer with an unintentional n doping level of 5×10^{16} cm^{-3}. Kang et al. fabricated GaN vertical SBD with Pt/Au Schottky contact and FP on e-beam deposited SiNx dielectric layer based on the simulation result, but to find a much lower experimental breakdown voltage than theoretical because of the GaN surface degradation from device processing [46]. Lei et al. did a comprehensive investigation of the GaN SBD FP design rule by simulation and came with the conclusions: Metal overlay extent beyond maximum depletion depth of GaN under reverse bias do not further improve breakdown voltage; The two competing reverse breakdown modes: GaN breakdown and dielectric breakdown

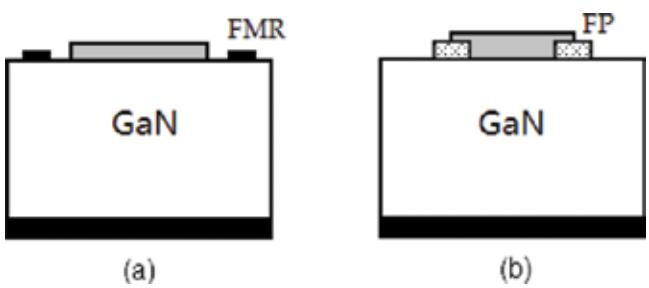

Figure 3. Schematics of (a) FMR and (b) FP structure: the gray region is Schottky contact, black region is ohmic contact, and the dotted region is dielectric.

lead to an optimum dielectric layer thickness; Optimum dielectric layer thickness is related with dielectric permittivity [47]. In summary, both simulation and experiment results demonstrated that addition device structures such as dielectric passivation layer, FRM and FP, can contribute to better GaN SBD performance.

Guard ring formed by ion implantation is also a very effective technique for edge termination: a high resistivity layer can be formed on the surface and help spreading electrical field under reverse bias. There are two types of implantation ion: p-type dopant or noble gas. Zhang et al. reported a p type guard ring by ion implantation of Mg at the edge of the Schottky contact followed by annealing [48]. A high breakdown voltage of ~700 V was achieved on vertical SBD structure with a 75 μm diameter circular Pt/Ti/Au Schottky contact. Laroche et al. reported simulation of multiple p type guard rings with 1 μm, and 5 μm spacing, and found a theoretical breakdown voltage of 700 V with 1 μm spacing, and the breakdown voltage did not further improve when multiple guard rings were applied [49]. Ozbek et al. reported that ion implantation of Ar can greatly improve the breakdown voltage of vertical GaN SBD [50, 51]. Simulation and experiment were carried out to analyze breakdown voltage versus length of implantation region. It was found that 50 μm is the optimum length, leading to a breakdown voltage of 1700 V, about four times higher than unterminated SBD.

Besides guard rings, ion implantation can also be used in fabrication of GaN junction barrier Schottky diode (JBSD). JBSD has been successfully demonstrated in Si and SiC. For n type JBSD, a p^+/n grid structure is used instead of an intrinsic or n^- layer in the drift region. Under forward bias, the p^+ region is not functioning, and the current flows through Schottky contact into the n channel. Under reverse bias, the depletion region spreads around the p^+ well and pinch off the n channel, thus suppresses premature breakdown and excessive leakage current. The p^+ well spacing and depth are important for best JBSD performance. Schematic of p^+ well JBSD is shown in **Figure 4a**. Zhang et al. fabricated GaN JBSD using both p^+ well on n channel and n^+ well on p channel, by ion implantation of Mg and Si into n-GaN and p-GaN respectively [52]. Both types of devices has breakdown voltages of 500 V- 600 V, and the leakage current was reduced 100-fold than conventional SBD fabricated without grid structure. The forward characteristics of the n type JBSD is much better than its p type counterpart. Ion implantation is not the only method to fabricate JBSD. Li et al. demonstrated trench JBSD, which eliminate the ion implantation step [53]. The schematics of the trench JBSD is shown in **Figure 4b**. The major difference between trench JBSD and regular JBSD is the formation of the

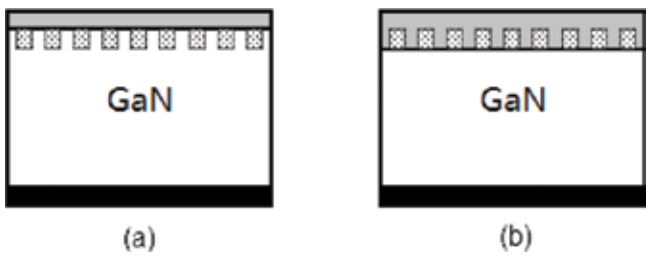

Figure 4. Schematics of (a) JBSD and (b) trench JBSD: the gray region is Schottky contact, black region is ohmic contact, and the dotted region is p^+ doped GaN.

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p^+/n junction. In trench JBSD, a p^+ epitaxy layer is firstly deposited, followed by a selective etching down to nGaN substrate to form trench structure. The Schottky contact is then deposited on the trench. Under reverse bias, the depletion region spread laterally from the p+/n interface and pinch off the Schottky barrier. The study of Li et al. shows about 20 times reduction in the leakage current compared to traditional SBD.

4. AlGaN/GaN field effect SBDs

Spontaneous and piezoelectric polarization can result in built-in electric field in AlGaN/GaN heterostructure. Band bending and alignment of Fermi level in AlGaN and GaN forms a two-dimensional electron gas (2DEG) at the interface. **Figure 5** shows band diagram of the AlGaN/GaN heterostructure. Because of the high carrier mobility of the 2DEG, low on-state resistance can be achieved for device utilizing AlGaN/GaN heterostructure. GaN based High-electron mobility transistor (HEMT) has been developed for power and RF applications and showed significant improvement of performance compared to Si and GaAs.

The AlGaN/GaN heterostructure can also be used in SBD. The concept of GaN field effect Schottky barrier diode (FESBD) was first brought up by Yoshida et al. in 2004 [54], with device schematics shown in **Figure 6**. AlGaN/GaN FESBD shares the same epitaxial structure and device fabrication process with AlGaN/GaN HEMT, making it a perfect diode for monolithic microwave integrated circuit (MMIC) application. Standalone AlGaN/GaN FESBD also has lower cost than GaN vertical SBD on freestanding substrate.

4.1. AlGaN/GaN substrate growth and epitaxial structure optimization

AlGaN/GaN heterostructure is usually grown on foreign substrates such as sapphire, SiC, or Si by MOCVD or MBE. In order to achieve high blocking voltage, low leakage and low on-state resistance at the same time, the epitaxial structure needs to be carefully designed. Several growth techniques have been reported to improve the device performance of AlGaN/GaN FESBD.

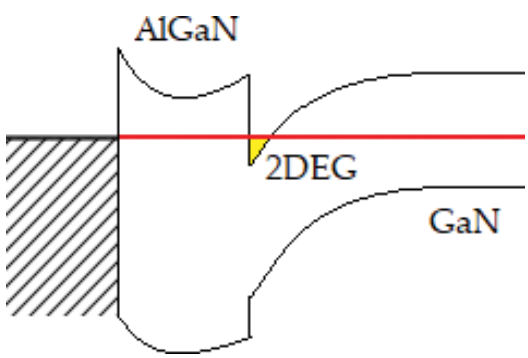

Figure 5. Band structure of the AlGaN/GaN heterostructure.

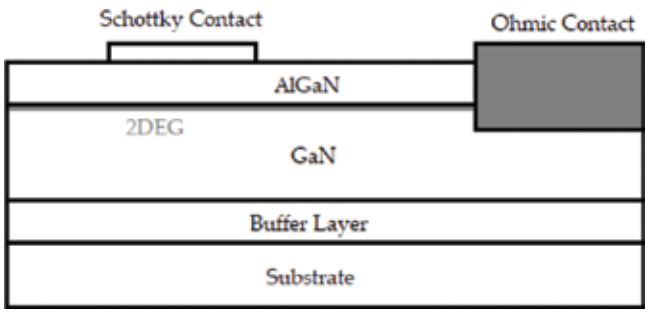

Figure 6. Schematics of AlGaN/GaN FESBD.

A buffer layer structure under the GaN channel layer is crucial because it can reduce the screw dislocation density thus can help on reducing reverse leakage and prevent premature breakdown. Lee et al. systematically investigated the electrical characteristics of the FEBSD with and without a composite buffer layer [55]. The buffer layer consisted of an 800 nm of AlN followed by a 30 nm of AlGaN. The breakdown voltage of the FEBSD with buffer layer was 3489 V, while that of FEBSD without buffer layer was only 382 V.

Similar to GaN SBD, a cap layer can help on the reverse leakage and breakdown voltage in FEBSD. Kamada et al. reported LTG GaN cap layer for edge termination in FEBSD [56]. A 20 nm LTG GaN, a 25 nm AlGaN and a 1 μm GaN were grown on Si substrate by MOCVD. A selective dry etching removed part of the GaN cap layer and exposed AlGaN layer for Schottky contact deposition. The FESBD with the GaN cap layer for edge termination has three order of magnitude lower leakage current than the traditional FESBD. A cap layer on top of barrier layer can also lower the barrier height and the turn-on voltage for better forward characteristics in FEBSD. Lee et al. developed a method to in situ grow a SiCN cap layer on top of the AlGaN barrier [57]. A 2 nm SiCN cap, a 25 nm AlGaN, and a 3 μm GaN were grown on sapphire substrate by MOCVD. It was found that forward current, reverse leakage and breakdown voltage of FESBD with SiCN cap layer were much better than regular FESBD.

4.2. FESBD device fabrication and device structure optimization

Because of the 2DEG feature, the device structure optimization for FESBD is not exactly the same as GaN SBD. Some structures that are widely used in GaN SBD and has been discussed in Section 3, such as dielectric passivation, FMR and FP, can also be used in FESBD, while some structures such as dual Schottky anode, Schottky-ohmic combined anode, recessed Schottky anode, gated edge termination and MIS-gated hybrid anode are unique to FESBD. The unique techniques that are discussed in the following paragraphs of this section share the same mechanism: Current flow path is optimized in the forward regime, while reverse blocking capability is not compromised by depletion of the 2DEG channel.

Yoshida et al. first introduced dual Schottky anode concept [54]. The schematics of the dual Schottky anode is shown in **Figure 7a**. A low Schottky barrier metal Al/Ti was used as lo Schottky barrier metal for better on-voltage, while a high Schottky barrier metal Pt was used to

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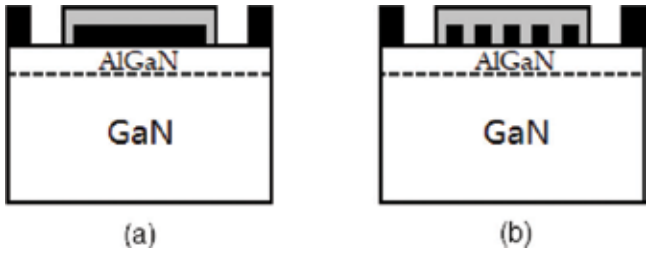

Figure 7. Schematics of AlGaN/GaN FESBD with dual Schottky anode: the gray region is Schottky contact, black region is ohmic contact, and dotted line is 2DEG.

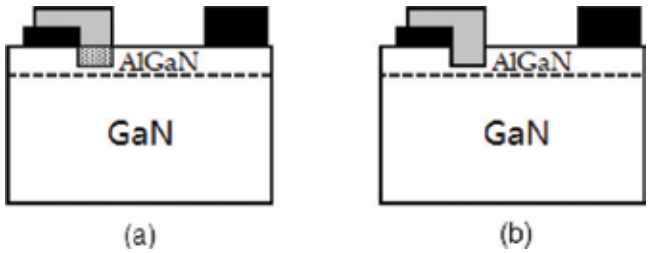

Figure 8. Schematics of AlGaN/GaN FESBD with SOC anode by (a) CF_4 plasma surface treatment (b) recessed Schottky: the gray region is Schottky contact, black region is ohmic contact, dotted region is plasma-treated AlGaN, and dotted line is 2DEG.

pinch off the device under reverse bias. A breakdown voltage of over 400 V was achieved. Park et al. adopted the concept and made improvement by introducing different Schottky and Ohmic contact patterns [58]. Schematics of the device was shown in **Figure 7b**. The on-state resistance was reduced by 25–75% at the cost of up to 3 orders of magnitude increment in leakage current, improved from 5 to 7 orders of magnitude increment with Yoshida's original design that has no pattern. However, the leakage current of the FESBD with dual Schottky anode design cannot be reduced to the same level of regular FESBD with only high Schottky barrier no matter how the contact pattern is optimized because of its normally-on nature.

To further reduce the turn-on voltage and suppress the reverse leakage, Schottky-ohmic combined (SOC) anode technique was introduced. Note that the technique can only be applied to depletion mode (normally-off) FESBD as the device will be shorted by the 2DEG under reverse bias if it is normally-on. As we know, there are two common methods to fabricate depletion mode HEMT: surface treatment and recessed gate. Both methods are also applicable to FESBD, with recessed gate changed to recessed Schottky. Takatani et al. [59] and Chen et al. [60] introduced SOC FESBD with surface treatment. CF_4 plasma was applied to the Schottky region of the FESBD to achieve normally-off mode, as the 2DEG under the Schottky region was depleted by negative fluorine ions. The device structure is illustrated in **Figure 8a**. The technique effectively improved the forward characteristics of the device and did not degrade reverse leakage and breakdown voltage [60]. SOC FESBD with recessed Schottky was also reported by multiple research groups. The device structure is illustrated in **Figure 8b**. Lee et al.

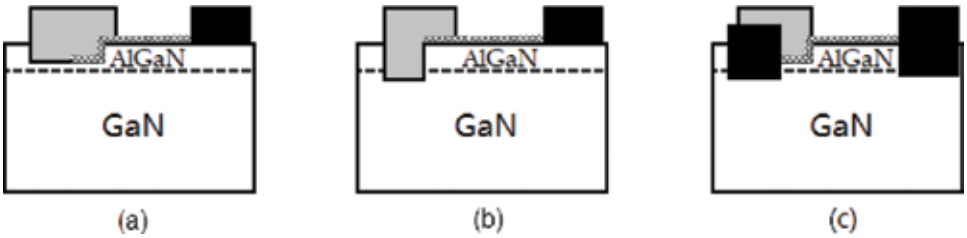

Figure 9. Schematics of AlGaN/GaN FESBD with (a) GET (b) fully recessed Schottky (c) MIS-gated hybrid anode: the gray region is Schottky contact, black region is ohmic contact, crossed region is gate dielectric, and dotted line is 2DEG.

compared it with conventional normally-on FESBD and normally-off FESBD with recessed Schottky but no SOC structure [61]. It was clearly demonstrated that the SOC FESBD with recessed Schottky is far superior to conventional FESBDs in turn-on voltage without breakdown voltage degradation. Recess depth is a very important parameter of SOC FESBD with recessed Schottky. Lee et al. did a comprehensive study of recess depth [62]. An optimized recess depth was found in between half and full thickness of AlGaN layer.

Lenci et al. introduced gated edge termination (GET) as illustrated in **Figure 9a** [63]. A thin dielectric layer was inserted underneath the recessed Schottky contact and formed an MIS gate structure. Under reverse bias, the 2DEG below the gate was pinched off. The reverse leakage current can be significantly reduced by the dielectric layer. The marginal extend-out of the Schottky metal on the dielectric layer formed a FP and reduced the electric field crowding. Bahat-Treidel et al. introduced a fully recessed Schottky anode with a slanted FP, which can significantly reduce the turn-on voltage because of the direct contact of Schottky anode to the 2DEG [64]. The schematics of the device structure is shown in **Figure 9b**. Yao et al. further investigated the current transport mechanism of the full recessed Schottky FESBD and found it was thermal field emission (TFE) instead of TE [65]. The GET and full recessed is compatible with other device optimization techniques. Hu et al. [66] and Zhu et al. [67] combined a 2nd FP technique with GET and fully recessed Schottky, respectively. The dual FP structure improved the breakdown voltage of FESBD with fully recessed Schottky.

Zhou et al. further optimized the device structure by combining the techniques above, and named it MIS-Gated hybrid anode [68]. The schematics of the device structure is shown in **Figure 9c**. It has an SOC anode with GET recessed Schottky, and fully recessed ohmic in direct contact with 2DEG. It also has a fully recessed ohmic contact on the cathode side. High breakdown voltage over 1.1 kV and leakage current as low as 10 μA/mm were achieved.

5. Summary

In this chapter, we gave a broad review of the GaN based Schottky diodes. The competitive position of GaN among the WBG materials in the high temperature, high frequency and high voltage rectifying applications was discussed first, followed with Schottky contact to GaN, and the development of GaN SBD and AlGaN/GaN FESBD in the last two decades. A lot of progress was made; and the best performing GaN based Schottky diode got close to SiC

material limit. However, there are still challenges ahead for the GaN based Schottky diodes: (a) Improvement of the material quality is desired. (b) Novel epitaxial and device structures leveraging state-of-art growth and fabrication techniques are needed. (c) Significant cost reduction from substrate and fabrication is crucial. With continuous effort from academia and industry, GaN based Schottky diodes will mature and be successful commercialized in a foreseeable future.

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Chapter 7

Inductive Power Transfer for Electric Vehicles Using Gallium Nitride Power Transistors

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Additional information is available at the end of the chapter

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Abstract

This chapter will present the application of the GaN Gate Injection Transistor (GIT) in Inductive Power Transfer (IPT) for Electric Vehicles (EV). IPT provides significant benefits over conventional plug-in chargers but suffers from lower efficiency. A high frequency inverter using GaN GIT, which has low on-resistance and gate charge, is implemented to reduce switching and conduction loss, resulting in higher efficiency. Different gate drive strategies will be compared for driving the GaN GIT at high slew rates while ensuring cross-conduction protection. The switching characteristics of the GaN GIT are studied and the inverter is designed to ensure low switching losses, while keeping overshoot and slew rates under control. Experiment results presented will demonstrate that the system efficiency peaks at 95% at 100 kHz operation and 92% at 250 kHz operation for a coil gap of 80 mm at 2 kW output power.

Keywords: gallium nitride, enhancement mode, wireless power transfer, inductive power transfer, electric vehicles, wide bandgap semiconductor application, gate driver

1. Introduction

Development of battery technology and advancement of power electronics has allowed EVs to gain popularity in the recent years, with strong boost to greener environment.

From an environmental conservation perspective, EVs demonstrate benefits above conventional Internal Combustion Engines (ICE) vehicles. EVs provide the energy efficient solution to conventional ICE, with energy efficiencies going as high as 62% compared to 21% for internal combustion vehicles. Pollution due to EVs is lesser as it does not produce emission unlike ICE [1].

Another push for in EVs is the performance benefits. Electric motors have smoother operations and quieter than ICE, while having stronger accelerations, and lesser maintenance [2].

However, there are some battery related challenges facing EVs. Due to limited charge holding capacity of Li-ion batteries, the driving range of EVs are limited compared to ICE vehicles, being able to only travel one-third or half the distance of an ICE vehicle [2]. In addition, the battery charging time is time consuming, with a full charge taking about 4–8 h and fast charge about 30 min compared to 5 min for an ICE vehicle [3]. Despite having higher charge carrying capacity compared to other battery materials, Li-ion batteries for EVs are still very big and bulky. They are expensive and need replacement during the car's lifetime [3, 4].

Inductive Power Transfer (IPT) is the method of wirelessly transferring power. The system for static wireless charging is as shown in **Figure 1**. AC power is drawn from the grid into the system. This power is rectified using a diode bridge to supply a DC voltage. This is followed by a Power Factor Correction (PFC) stage to improve the power factor and step up the voltage to 380 V. The DC input voltage is supplied into an inverter, which converts it in high frequency AC so that power can be transmitted by primary coil to the secondary coil using IPT. The secondary coil will take in the HF AC power and rectify it using the SiC diode bridge into a DC voltage for vehicle charging. IPT for EVs provide a convenience and safety for the user [5, 6]. This system is weatherproof and difficult to vandalism like a plug-in station [4].

However, there are challenges facing wireless charging, such as low efficiency compared to plug-in chargers [4]. This is overcome by using wide bandgap semiconductor materials such as GaN, which is attracting attention for enabling high efficiency, high power density converters [7], rectifiers [8] and inverters [9, 10]. The material properties of GaN such as high critical field, electron mobility and saturation velocity [11] push the boundaries of power electronics performance such as efficiency, power density, reliability and cost [12].

The remainder of the chapter is organized as follows. Section 2 will compare various gate driving methods for driving the GaN GIT. This is followed by Section 3 which will explain the design considerations for apply the GaN GIT in WPT applications. Finally, Section 4 contains experiment results that demonstrate the advantages of using GaN in IPT.

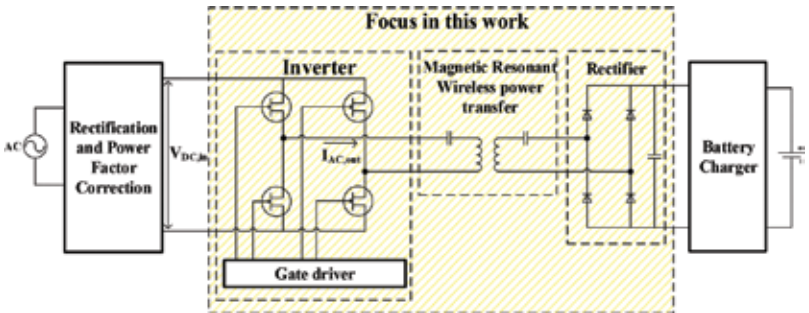

Figure 1. Static wireless charging.

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2. Comparing gate drive methods for driving GaN GIT

Among the various enhancement mode GaN, Gate Injection Transistor (GIT) is one such technology, which is able to achieve normally off operation and high current driving capability [13]. The GaN GIT adopts p-GaN with recessed gate to achieve normally-off. The Hybrid Drain embedded in the GIT (HD-GIT) allows the device to overcome the current collapse [14].

Since the GaN GIT is a normally-off device, it can be driven by conventional gate drive methods like the R-type gate drive is shown in **Figure 2a**. Resistor RA1 facilitates the charging during turn on, while the path along RA2 forms the discharge path during turn off.

To capitalize on the switching performance of the GaN device, the RC-type gate drive method [15] is recommended. This gate drive strategy allows the driving of the GaN GIT's gate at a higher voltage allowing faster slew rate. It produces negative gate voltage during turn off to prevent false turn-on, while using a unipolar supply voltage.

A single channel GaN GIT gate driver Integrated Circuit (IC) (AN34092B) utilizes a novel gate drive strategy to compare against existing gate drive methods is shown in [16]. The simplified gate drive circuit for the GaN GIT gate driver IC, AN34092B [17], is shown in **Figure 3a**. The gate driver IC has 3 output pins, namely OUT1, OUT2 and OUT3. OUT1's purpose is to charge the GaN power transistor during turn ON phase and discharging the speed-up capacitor C1 during turn off. When the device is fully turned on, C1 will block current through OUT1.

OUT2 will continue to supply an adjustable DC current of 2.5–25 mA during conduction phase. Integrated within the IC is an adjustable current source, which is able to provide a constant current during turn ON, that is important for the conductivity modulation of the GaN GIT. It also provides a low impedance path using the active miller clamp function.

OUT3 is responsible for the discharge path by pulling the gate to the negative voltage VEE. The turn off slew rate can be controlled using resistor R2. Another integrated function is a charge pump to provide the negative voltage, VEE, during turn OFF, which is adjustable using an external resistor.

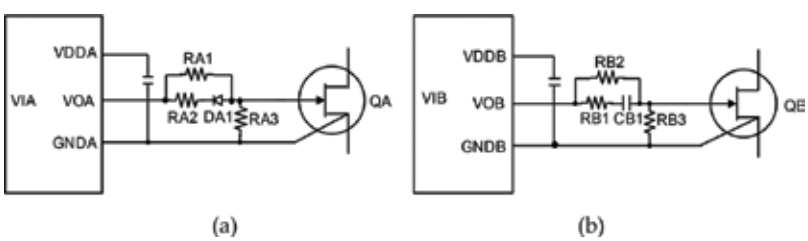

Figure 2. Various gate drive methods: (a) the R-type and (b) the RC-type.

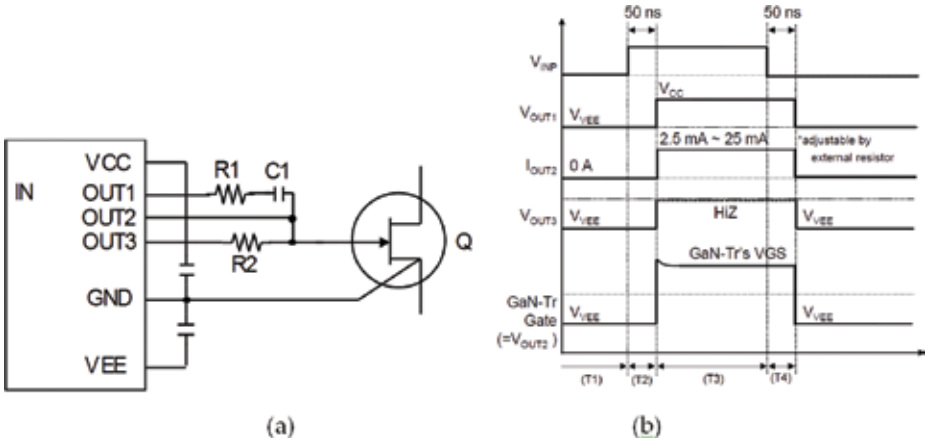

Figure 3. (a) GaN GIT gate driver IC circuit and (b) gate driver timing diagram.

2.1. High slew rate gate drive

Power density and efficiency are important metrics in power electronics. High slew rates allow high operating frequencies, which lead to higher power density due to smaller passive components. In addition, higher slew rates result in an improvement in the switching losses which result in higher efficiency.

The general equation of V_{DS} turn-on and turn-off slew rate is shown in Eqs. (1) and (2) respectively. The fall and rise in the drain-source voltage, $V_{DS,}$ occurs during the charging and discharging of the gate-drain charge, Q_{GD}, at the plateau voltage, V_{pl}. The ability to charge and discharge faster means higher slew rates for the power device.

$$\frac{d\,V_{DS}}{d\,T_{turn\ on}} = \frac{I_{GS} \times V_{Power\ supply}}{Q_{GD}} = \frac{(VDD - V_{pl}) \times V_{Power\ supply}}{R_{gate} \times Q_{GD}} \tag{1}$$

$$\frac{d\,V_{DS}}{d\,T_{turn\ off}} = \frac{I_{GS} \times V_{Power\ supply}}{Q_{GD}} = \frac{(VEE - V_{pl}) \times V_{Power\ supply}}{R_{gate} \times Q_{GD}} \tag{2}$$

Based on Eqs. (1) and (2), slew rates can be improved by controlling gate current or using a device with a small QGD. The high breakdown electric field of GaN material allows the GaN GIT to have smaller die size compared to Si power MOSFETs of similar breakdown voltage, which results in smaller parasitic capacitance and correspondingly smaller QGD. To control the charging and discharging of gate current, one can choose to control the value of the gate resistor or adjust the gate driver source and sink voltage.

2.1.1. Turn-on: dual current source paths for gate protection

To protect the GaN GIT's gate from damage, it is important to keep the gate pulse current and gate pulse charge below the absolute limit. However, controlling the turn-on gate current source through a single path like the R-type gate drive method limits the peak gate current,

which is responsible for high slew rate performance. On the other hand, the GaN GIT driver IC and RC-type gate drive provide two current paths, a high current path during turn-on transients for high slew rate performance and a low current path to keep the GaN GIT in conduction. This is to prevent damaging the gate.

The high current source path of the GaN GIT driver IC and RC-type gate driver comprises a resistor in series with a capacitor. When the power device is fully turned on, the capacitor will block current flow, protecting the gate of the GaN GIT. This allows the GaN GIT driver IC and RC-type gate driver to drive the GaN GIT at a higher supply voltage, resulting in a higher gate current and larger turn-on slew rate. This is supported by Eq. (1), which shows that a higher VDD increases slew rate.

2.1.2. Turn-on: discharging speed-up capacitor to improve turn-on slew rate

For RC circuit, turn-on slew rate is affected by negative voltage of the speed-up capacitor, CB1 on **Figure 2b**. The residue voltage in the capacitor CB1 will reduce the VDDB voltage used to charge the power device. The GaN GIT driver IC resolves this problem with a high speed discharge circuit to discharge C1. So when the gate driver charges the power device during, it is able to charge the GaN GIT gate from the full VDDB rail.

2.1.3. Turn-off: negative voltage

The GaN GIT driver IC and RC type gate drive generates a negative voltage turn-off. The RC-type gate driver relies on the connection of the speed-up capacitor, CB1, to create a negative voltage during turn off. With reference to **Figure 1b**, during turn-on transition, the capacitor CB1 is charged up such that the left hand side is positive relative to the right hand side of CB1. During turn-off, the positive side of CB1 is connected to ground, GNDB, which presents a negative voltage at the gate. This negative voltage slowly decays as it is discharged through RB1 and RB2.

On the other hand, the GaN GIT driver IC has a built in charge pump to generate an adjustable negative rail, VEE, from −3 to −5 V. According to Eq. (2), negative voltage turn-off allows larger gate discharging current leading to larger turn-off slew rates compared to R-type gate drive circuits, which discharge at 0 V.

2.2. Cross conduction protection

Cross conduction is a false turn-on mechanism that occurs when the high side device is turned on during dead time. When the high side device is turned on, the drain of the low side power transistor is pulled up, inducing a current across the gate-drain capacitor of the low side power device. This current causes a voltage across the gate-source pin of the power device as it flows through the gate resistor. Research showed slew rates and gate resistance [18] affects the induced gate voltage. For high slew rate power devices, these are practical challenges which need to be addressed. This work aims to reduce VGS spike voltage without sacrificing slew rate performance. There are various countermeasures to reduce the effects of cross conduction.

2.2.1. Low gate impedance

A common countermeasure using the R-type gate drive for cross conduction protection is to implement a low impedance discharge path through the Schottky barrier diode (DA1) in series with a small resistor (RA2) as shown in **Figure 1a**. During the turn off, this forms a very low impedance path, which sinks the induced current to GND. In this method, the slew rate is dependent on the cross conduction protection.

Unlike the R-type gate drive, which has only one output to sink the gate current, the GaN GIT driver IC has 2 gate sink paths. One path (OUT3) to control the GaN GIT gate discharge current to control the slew rate and another path (OUT2) for active miller clamp function, which implements low gate impedance during the cross conduction period and reduces gate ringing. This unique function allows slew rate control independent of the active miller clamp protection function.

2.2.2. Negative voltage

Implementing a negative gate-source voltage during turn off creates a voltage buffer between V_{GS} and V_{th} to prevent the GaN GIT from turning on when cross conduction occurs. The RC-type gate drive creates a negative voltage across the VGS during turn-off due to the change in polarity of the speed up capacitor CB1. On the other hand, the GaN GIT driver IC has built-in negative voltage rail to create this voltage buffer. These two methods are able to create a negative voltage rail with a unipolar voltage supply, which reduce cost.

2.3. Experiment results of gate drive methods

2.3.1. Experiment setup

The driving methods are tested using a half bridge configuration based on **Figures 2** and **3a** as shown below in **Table 1**. The evaluation was conducted using 600 V, 10A SMD GaN GIT. R-type and RC-type gate drive were tested using SWEVB005-PGA26E19BA half bridge evaluation board (**Figure 4a**), while the GaN GIT gate driver IC (AN34092B) was tested using SWEVB008-PGA26E19BA half bridge evaluation board (**Figure 4b**). The purpose is to keep the parasitic inductance of the gate drive loop and power loop similar across the three evaluation setups.

	VDD (V)	$V_{Negative}$	Component 1	Component 2	Component 3
R-type gate drive	5	Nil	RA1 = 51 Ω	RA2 = 1 Ω	DA1 = SBD
RC-type gate drive	12	−5 V	RB1 = 51 Ω	RB2 = 2700 Ω	CB1 = 1.2 nF
GaN GIT gate driver IC	12	−5 V	R1 = 51 Ω	R2 = 1 Ω	C1 = 120 pF

Table 1. Design parameters and values for experiment.

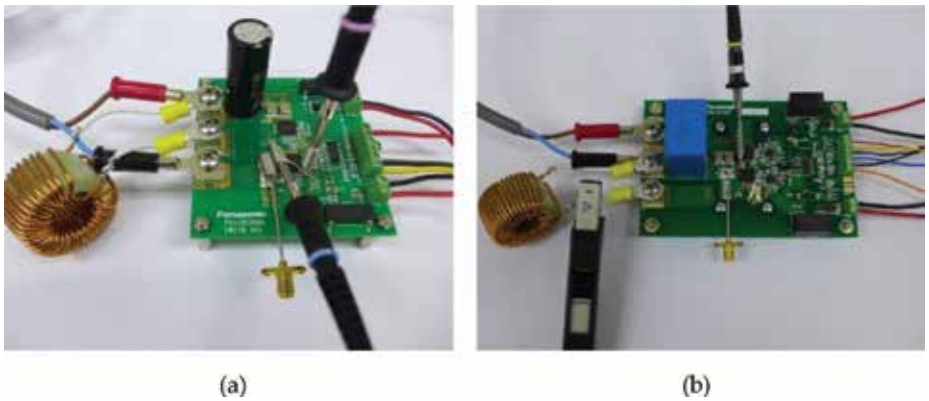

Figure 4. Experiment setup for (a) R-type and RC-type gate drive method and (b) GaN GIT gate driver IC.

Double pulse test was conducted with an inductive load and bus voltage of 400 V. It is tested for load currents at 2.5, 5, 7.5 and 10A. Since it is a half bridge circuit, the slew rates for the low side and high side GaN GIT are measured. The gate-source voltage of the low side is probed during high side test to study the cross conduction protection.

2.3.2. Slew rates results

The waveforms are taken at I_{DS} = 10A and V_{DS} = 400 V. The results for the V_{DS} turn-on and turn-off slew rate were measured from 10 to 90% and waveforms are shown in **Figure 5**. From **Figure 5**, it is observed that the V_{GS} is charged up slower for the R-type gate drive (**Figure 5a**) compared to the RC-type (**Figure 5b**) and GaN GIT gate driver (**Figure 5c**). This is because the RC-type and GaN GIT gate driver charge the gate up with VDD = 12 V, allowing more charge to be supplied compared to the R-type gate drive which have VDD = 5 V supply. Thus, results in a faster VDS slew rate.

With reference to **Figure 5**, it shows that VGS for the R-type gate drive (**Figure 5d**) is turned off at 0 V, while the RC-type (**Figure 5e**) and GaN GIT gate driver (**Figure 5f**) are turned off with a negative voltage. The negative voltage of the RC-type circuit is decaying to 0 V as the capacitor discharges while the GaN GIT gate driver is held at −5 V until the next turn on cycle.

The results for the low side slew rates are shown in **Figure 6**, which illustrate the turn-on (**Figure 6a**) and turn-off (**Figure 6b**) slew rates. From **Figure 6a**, the GaN GIT has the highest turn-on slew rate (97 V/ns) followed by the RC-type (48 V/ns) and finally the R-type (26 V/ns). The gate drive resistor value, which is critical for turn-on slew rate, is fixed at 51 Ω for all three setups to make a fair comparison with the other gate drive methods.

The RC-type and GaN GIT driver are clearly faster than R-type because they are driven at 12 V. GaN GIT driver is faster than the RC-type gate drive because of the discharging speed-up capacitor function and the choice of a smaller speed-up capacitor (C1 = 120 pF vs. CB1 = 1.2 nF). The reason for the larger capacitor for the RC-type gate drive is to increase the RC time constant to slow down the decay of the negative turn-off voltage.

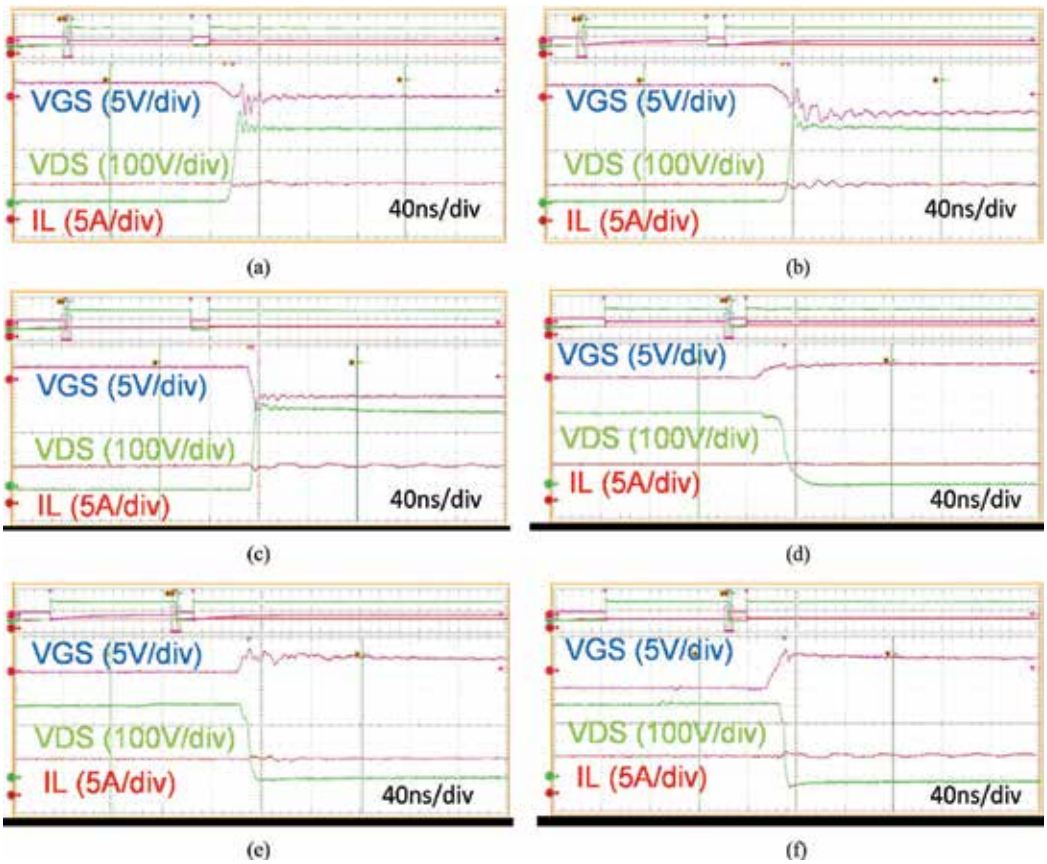

Figure 5. Double pulse waveform for (a) R-type, (b) RC-type and (c) GaN GIT gate driver during turn-off and for (d) R-type, (e) RC-type and (f) GaN GIT gate driver during turn-on.

The turn-off slew rate results is depicted in **Figure 6b**. From the graph, it is shown that slew rate for RC-type and R-type are close, while GaN GIT driver IC outperforms them to achieve

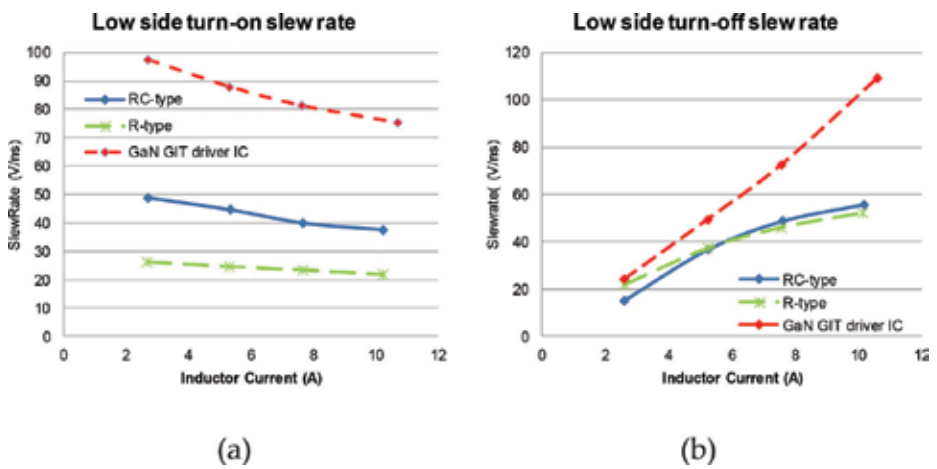

Figure 6. Slew rate measurement results for (a) low side turn-on and (b) low side turn-off.

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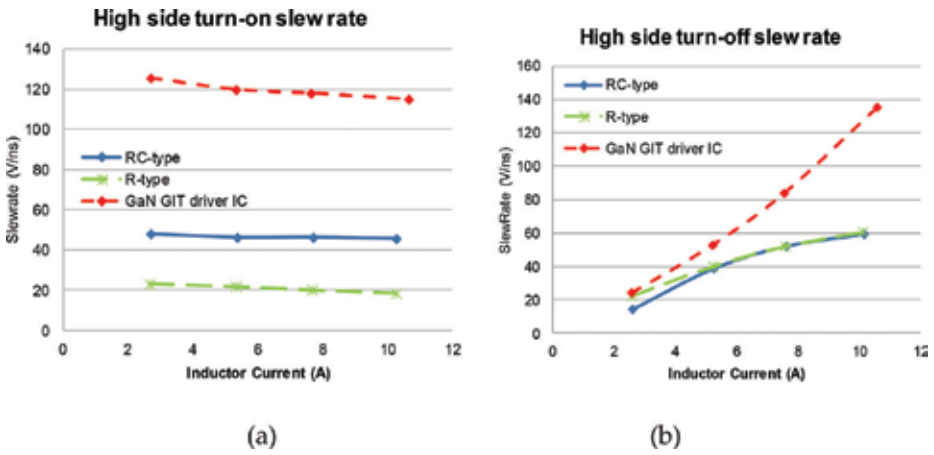

Figure 7. Slew rate measurement results for (a) high side turn-on and (b) high side turn-off.

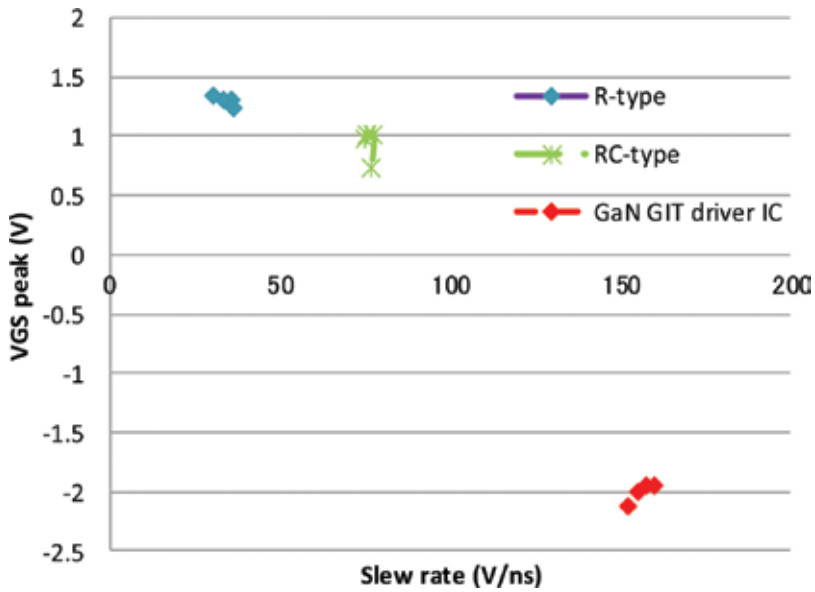

Figure 8. Cross conduction test.

a maximum slew rate of 110 V/ns. While both RC-type and GaN GIT driver IC discharges the gate with negative voltage, the RC-gate drive method has a larger discharge resistance resulting in a slower turn-off slew rate. The R-type gate drive has a low resistance to GND, but discharges to GND instead to a negative voltage. The GaN GIT driver IC capitalizes on low impedance from gate to VEE and a negative voltage to achieve twice the slew rate.

The high side slew rate is shown in **Figure 7**. Results are very similar to the low side results in **Figure 6**, except that the high side results are slightly faster. This is because of the probe capacitance loading on the VGS and VDS pin during low side test that slow down the slew rate measurement results.

2.3.3. Cross conduction protection

The low side VGS spike voltage occurs when high side is turned on is measured and plotted against the slew rates (according to **Figure 7a**) and shown in **Figure 8**. From the results, it shows that the GaN GIT gate driver has the lowest VGS spike voltage, despite higher slew rate operation than the other two methods. All three methods managed to keep this spike voltage below the threshold voltage of the GaN GIT.

3. Switching loss evaluation and gate drive optimization for IPT in EV system

3.1. Power device selection

A common Figure of Merit (FOM) adopted by power semiconductor devices is RonQg. This FOM accounts for the switching and conduction loss such that the lower the FOM, the better the performance. This is a representative of the technology [19]. A comparison of FOM among three state-of-the-art transistors using GaN, SiC and Si are compared and shown in **Table 2**.

GaN GIT has the lowest FOM due to the high critical field of GaN and the High Electron Mobility Transistor (HEMT) structure. The Si vertical MOSFET performs the worst with the highest FOM. This is followed by SiC MOSFETs which perform an order of magnitude better. It is shown that Si Super Junction MOSFETs being able to outperform SiC MOSFETs for RonQg. This is because the Super Junction technology is able to push beyond the theoretical limits of Si.

3.2. Half bridge circuit loss modeling

The total losses in a half bridge circuit contains conduction loss, switching loss, ringing loss and dead time loss of the top and bottom power device and is shown in Eq. (3). The subscript top and bot respectively denote the top and bottom power device.

Material	GaN	Si	Si	SiC	SiC
Technology	Gate Injection Transistor	MOSFET	Super Junction MOSFET	MOSFET	MOSFET
Breakdown voltage (V)	600	600	700	650	1200
Rated current (A)	15	6	18	29	40
R_{on} (mΩ)	65	1000	125	120	80
Q_g (nC)	11	33	35	61	106
$R_{on}Q_g$ (nΩC)	0.715	33	4.38	7.32	8.48

Table 2. FOM comparison between semiconductor devices.

The total conduction loss is shown in Eq. (4) and is influenced by the on-resistance, R_{on}, of the device and application requirements such as drain-source current, I_{DS}, and duty, D. Switching loss, on the other hand, is frequency dependent as shown in Eq. (5). It is affected by the drain-source voltage, V_{DS}, and current during the turn on (t_{on}) and turn off (t_{off}) switching transition. This shows the need for soft switching or fast slew rates for hard switching applications to reduce switching losses.

The ringing loss is obtained from [20] and modified for GaN GIT as shown in Eq. (6). GaN GIT does not have Q_{rr} but still has to discharge drain-source capacitor, C_{DS}, which is represented by the drain source charge, Q_{oss}. Ringing losses are proportionate to frequency and DC-link voltages, V_{bulk}. The turn on ringing loss are affected by the Q_{oss}, while the turn off losses are affected by charges, Q_{Vpeak}, due to the peak ringing voltage V_{peak}. High slew rates and parasitic source drain inductances increase the peak voltage.

The absence of reverse recovery diode implies that dead time, t_{SD}, can be reduced. However, the GaN device will still experience a dead time loss according to Eq. (7). When a reverse current I_{SD} flows through the device, it will have a voltage drop, V_{SD}, during dead time that results in dead time loss.

$$P_{HB\,loss} = P_{cond\,loss} + P_{sw\,loss} + P_{ringing} + P_{dead\,time} \tag{3}$$

$$P_{top\&bot,cond\,loss} = I_{DS}^2 R_{on,top} D + I_{DS}^2 R_{on,bot}(1 - D) \tag{4}$$

$$P_{sw,on\&off} = \frac{1}{2} f V_{DS} I_{DS}\left(t_{on,top} + t_{off,top} + t_{on,bot} + t_{off,bot}\right) \tag{5}$$

$$P_{ringing} = V_{bulk} f\left(Q_{oss,top} + \frac{1}{2} Q_{oss,bot}\right) + \frac{1}{2} f\left(Q_{Vpeak}\left(V_{peak} - 2\,V_{bulk}\right) + Q_{Vin}\,V_{bulk}\right) \tag{6}$$

$$P_{dead\,time} = V_{SD} \times I_{SD} \times t_{SD} \times f \tag{7}$$

3.3. Experimental results and GaN GIT gate driver optimization

Double pulse switching characteristic test, using an inductive load circuit shown in **Figure 9**, is conducted to evaluate the performance of the GaN GIT under EV wireless charging conditions. The GaN GIT is evaluated based on the specifications of the design. The drain-source parameters of the device is tested based on a DC-link voltage of 400 V, with load current varying from 2.5 to 15A. The gate drive voltage is set at 12 V. The value of drain-source voltage/current overshoot, drain-source voltage slew rate and switching losses energy will be measured. The gate drive resistor R1 will be varied from 5.1 to 36 Ω. **Figure 10** shows the waveforms at 400 V and 10A using R1 = 10 Ω.

Parasitic inductance in the gate drive loop should be small to improve the slew rate of the GaN device. One should consider reduction of the source and drain inductances along the

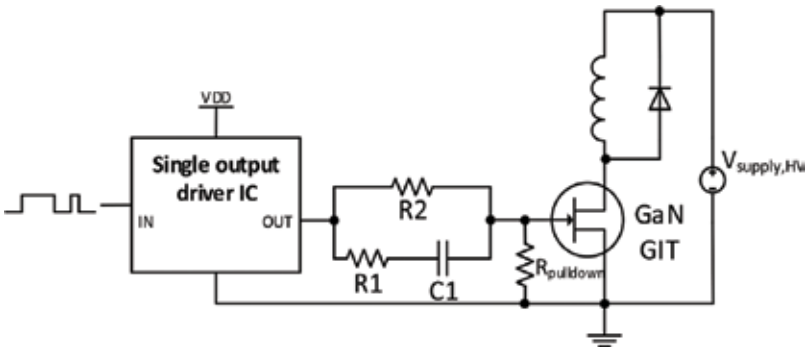

Figure 9. Experimental setup for inductive load circuit for double pulse test.

power loop to reduce the V_{DS} ringing. For realistic results, adopt a freewheeling diode that have a similar reverse recovery charge to the GaN GIT's reverse conduction Q_{DS}.

The turn-off and turn-on switching loss energy per cycle is shown in **Figure 11**. Reducing the gate drive resistor, R1, results in higher gate current, reducing rise and fall time and thus reducing switching losses. As load current increases, the switching loss also increase. These two observations agree with Eq. (5).

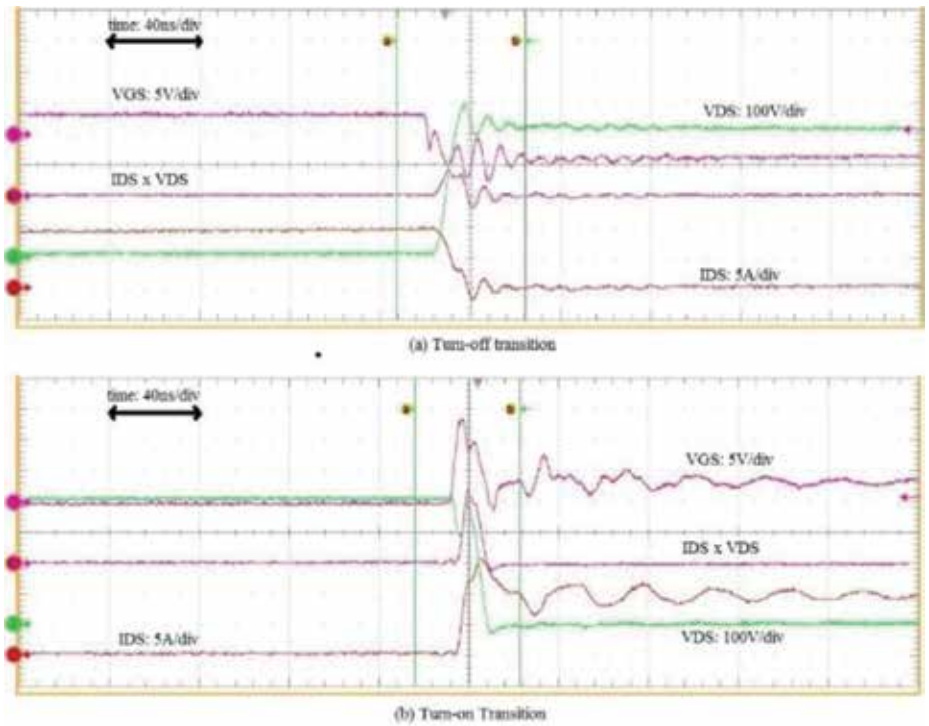

Figure 10. Switching experimental results of 2-pulse test results: (a) turn-off transition for TO-220 GaN GIT and (b) turn-on transition for TO-220 GaN GIT.

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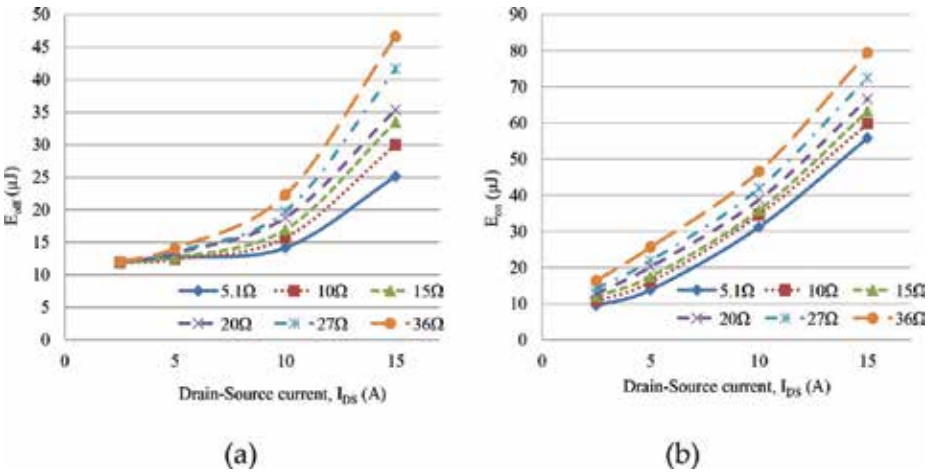

Figure 11. Evaluation results for switching energy per cycle: (a) turn-off switching energy and (b) turn-on switching energy.

The second factor for consideration is the drain-source voltage overshoot. **Figure 12a** and **b** shows the turn-off voltage peak and turn-on current peak respectively, with variation in the load current and the gate drive resistor. Voltage and current overshoot is directly proportional to load current. Reduction in the gate drive resistance increases the overshoot. From the evaluation results, it shows that the observed overshoot is below the absolute voltage and current rating and hence the device is safe.

Finally, we will evaluate the slew rate results in **Figure 13**. **Figure 13a** illustrates the slew rate during the turn off transition. The slew rate increases as the gate drive resistance is reduced and achieves a maximum slew rate of 67 V/ns at 5 Ω. This work utilizes the GaN GIT with TO-220 package which has higher parasitic inductance compared to surface mount packages, resulting in slower slew rates.

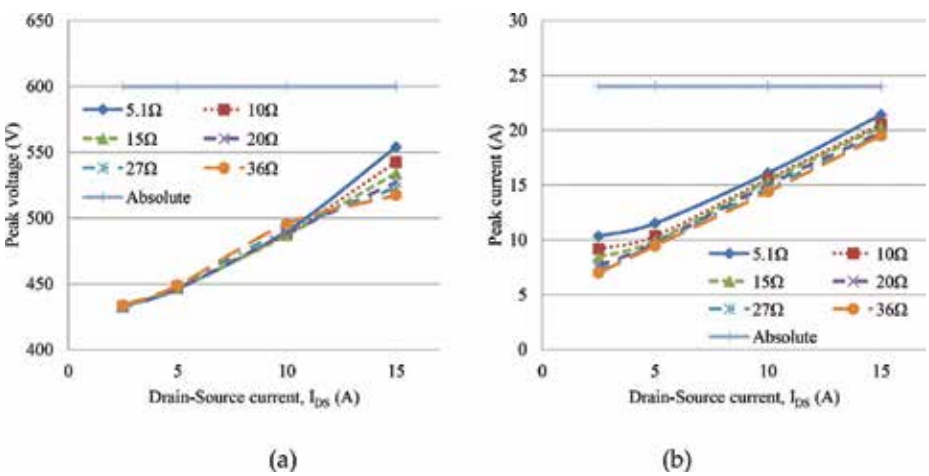

Figure 12. Evaluation results for overshoot: (a) drain source voltage peak vs. absolute rating and (b) drain source current peak vs. absolute rating.

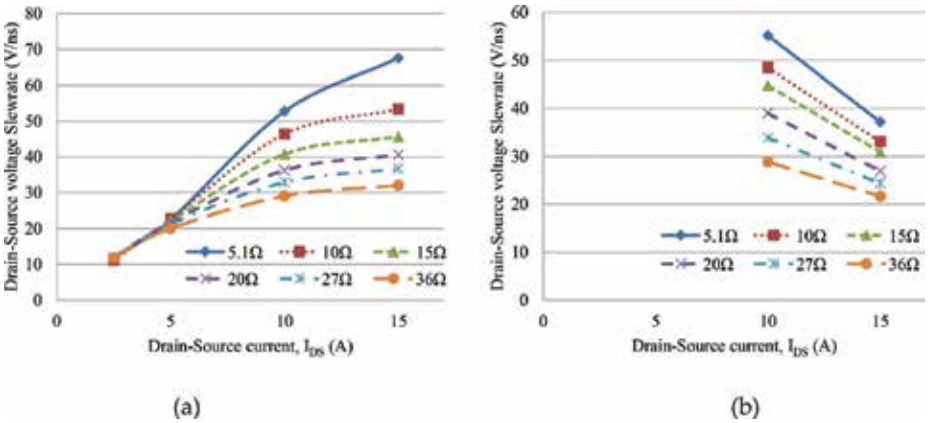

Figure 13. Evaluation results for slew rate: (a) VDS slew rate during turn-off transition and (b) VDS slew rate during turn-on transition.

Figure 13b shows the turn on slew rate. Lower gate drive resistance causes higher slew rates while slew rates drop as load current increases. Due to parasitic inductance within the TO-220 package, a voltage drop is observed across the drain to source nodes when drain source current flows through it, affecting the slew rate measurement of V_{DS} at low load (2.5 and 5A condition). Therefore, only higher load conditions (10 and 15A) are shown.

Based on the evaluation data, the choice of R1 should ensure low total switching energy and peak drain-source voltage. Although the 5 Ω results performed better, it has a slew rate above 50 V/ns. During the design, there were not many isolated half bridge gate drivers, which can handle high slew rate operations, characterized by the parameter called common mode transient immunity (CMTI). The highest CMTI was from ADuM3223 at 50 V/ns. Therefore, while 5 Ω had better evaluation results, we chose 10 Ω so that it can function within the limits of our isolated gate driver.

4. Experiment results of inductive power transfer system

The hardware for the solution is shown in **Figure 14**, comprising of a high frequency inverter, a pair of magnetically coupled coils, a high frequency rectifier on the secondary side and a resistor bank acting as a load. The system is tested from 80 to 150 mm. The input voltage to the inverter is 370VDC, which is the typical output voltage from the PFC stage. In order to ensure the inverter output current is below the current rating of the GaN GIT, the resistor load is set to 47 Ω at 80 mm and 11.5 Ω at 150 mm. This is because variation in coil gap affects the mutual inductance and hence affects the reflected load from the secondary side to the primary side.

The system efficiency from 80 to 150 mm is shown in **Figure 15**. The highest efficiency is obtained at 80 mm at 2.1 kW. As the coil gap increases, the efficiency falls as shown with the peak efficiency occurring at 90.4% at 150 mm. The reason for testing at 150 mm up to 1.5 kW is to operate the inverter below the absolute current limit of the 15A GaN GIT device.

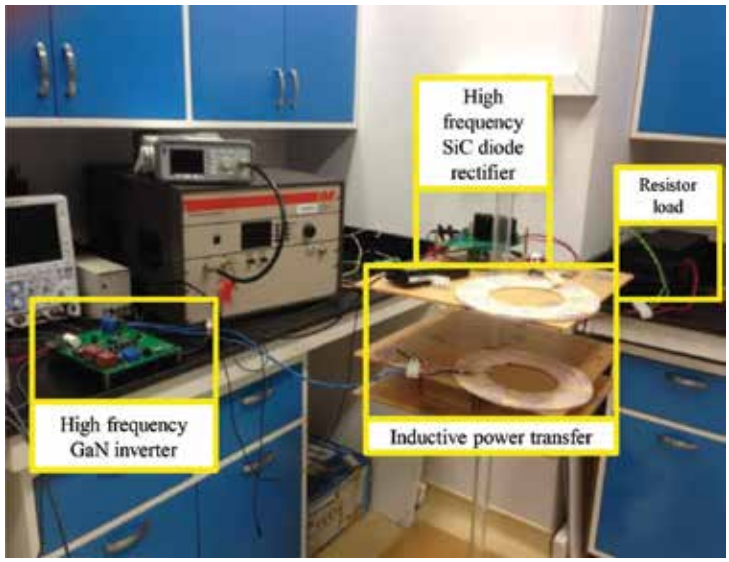

Figure 14. Wireless power transfer experiment setup.

The efficiency breakdowns of each individual stages at 150 and 80 mm are shown in **Figures 16** and **17** respectively. They are tested at an operating frequency 100 kHz. The high frequency inverter maintains its efficiency within the 97–98% region across the varying distances at 2 kW. The coil efficiency falls drastically as the coil gap increases. This is because the increase in distance results in a weaker coupling factor causing a higher secondary current and hence increases the copper loss in the coil. At 80 mm, the efficiency of the rectifier performs well. This is because the SiC diode forward voltage is small relative to output voltage. However, as coil gap increase, the secondary voltage drops, which makes the diode forward voltage loss more significant.

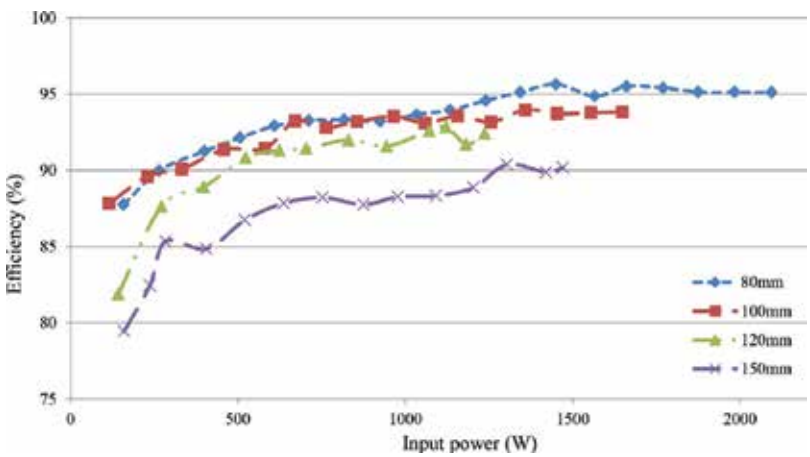

Figure 15. Experimental results: efficiency vs. distance.

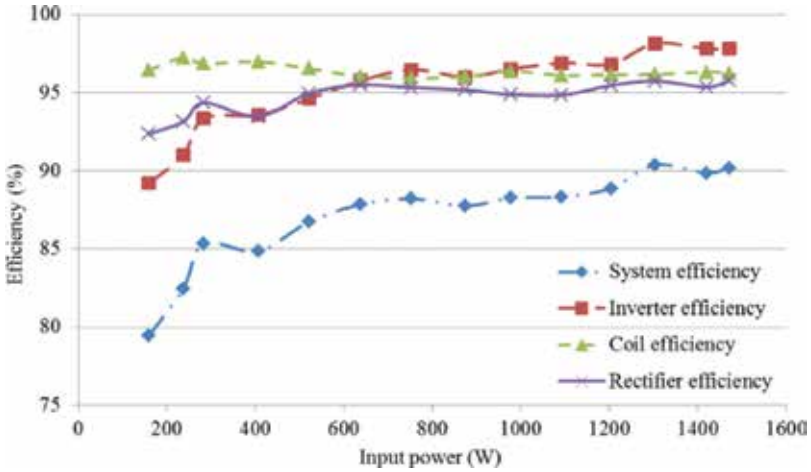

Figure 16. Experimental results: efficiency breakdown at 150 mm.

The waveform of the inverter output current (CH1), inverter output voltage (CH2), IPT output voltage (CH3) and IPT output current (CH4) at 80 mm distance, operating at 100 kHz is shown in **Figure 18**. The figure shows the zoom out version at 20 μs/div on the top and the zoom in image at 2 μs/div on the bottom.

The next experiment compared efficiencies by varying the operating frequency from 100 kHz to 250 kHz at a 80 mm coil gap, evaluating the system up to 2 kW. **Figure 19** illustrates the results and it shows a drop in system efficiency from 95.13 to 91.7% at 2 kW. This efficiency in the inverter fell due to switching losses at higher frequency operation. The IPT coils will experience higher AC resistance due to skin effect as the operating frequency increase by 2.5 times. The rectifier suffers from higher reverse recovery loss at higher frequencies.

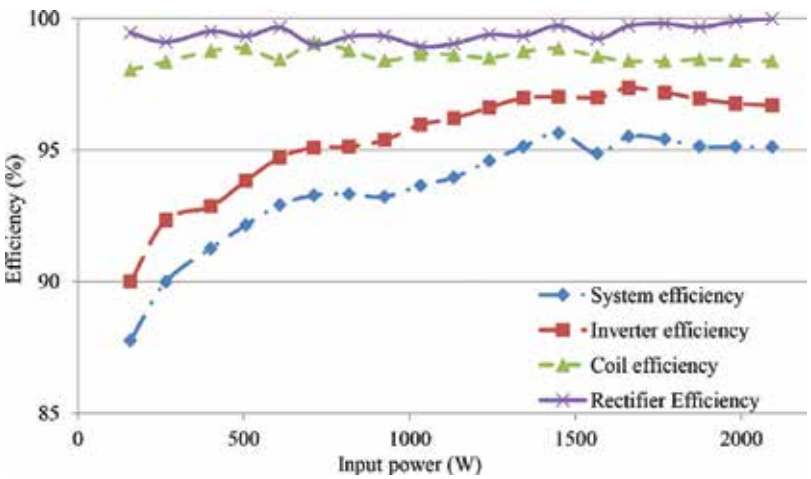

Figure 17. Experimental results: efficiency breakdown at 80 mm.

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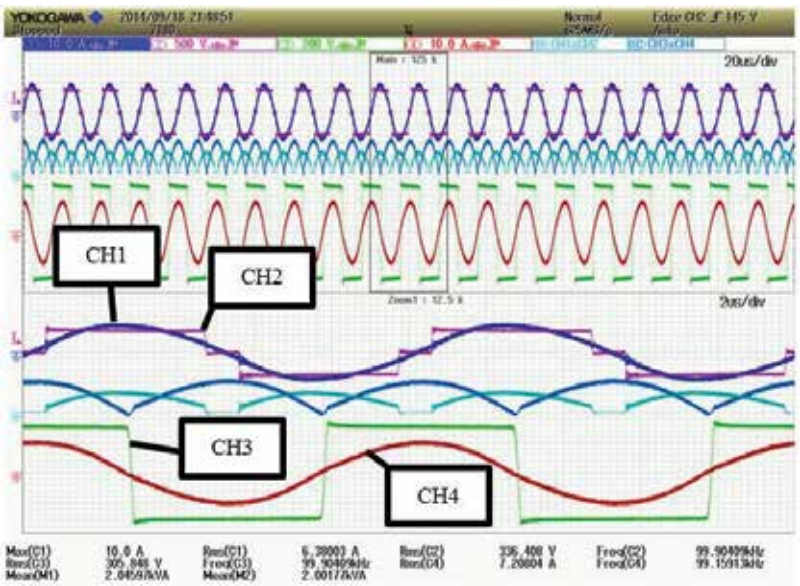

Figure 18. Experimental results of inverter and coil channel 1: inverter output current, channel 2: inverter output voltage, channel 3: IPT output voltage, channel 4: IPT output current.

A similar setup was made using a SiC based high frequency inverter. The efficiency comparison between the GaN based and SiC based system is illustrated in **Figure 20**. The GaN based system outperformed the SiC based system by 1% at 2 kW, which translates to 20 W less heat dissipated on the inverter. This was because of the lower on-resistance and gate charge of the GaN GIT, resulting in lower conduction and switching loss.

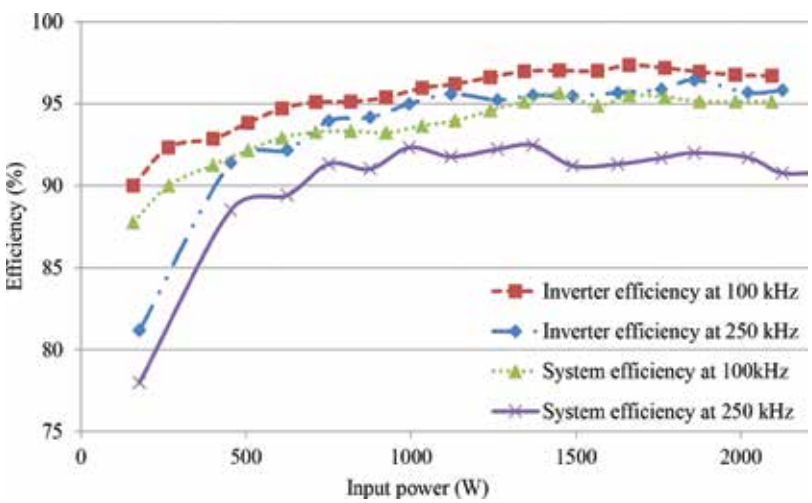

Figure 19. Experimental results: efficiency vs. input power for varying frequencies.

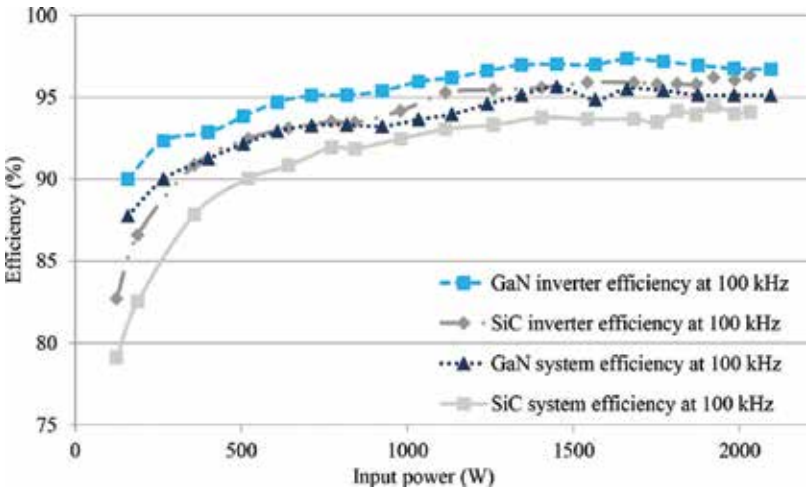

Figure 20. Experimental results: efficiency comparison between GaN and SiC.

5. Conclusion

In this work, a practical high efficiency wireless power transfer system for EV charging application is developed. The GaN GIT introduced is able to provide superior performance and system benefits. Gate drive strategies are introduced with performance evaluation showing that GaN GIT gate driver achieves high slew rate, while still providing protection from cross conduction. Application of GaN GIT is adopted to improve the efficiency of the inverter by optimizing the gate drive circuit. Experimental results prove the efficiency advantage of adopting GaN GIT in high frequency applications such as inductive power transfer for electric vehicle charging.

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SiC and GaN devices have been around for some time. The first dedicated international conference on SiC and related devices, "ICSCRM," was held in Washington, DC, in 1987. But only recently, the commercialization of SiC and GaN devices has happened. Due to its material properties, Si as a semiconductor has limitations in high-temperature, high-voltage, and high-frequency regimes. With the help of SiC and GaN devices, it is possible to realize more efficient power systems. Devices manufactured from SiC and GaN have already been impacting different areas with their ability to outperform Si devices. Some of the examples are the telecommunications, automotive/locomotive, power, and renewable energy industries. To achieve the carbon emission targets set by different countries, it is inevitable to use these new technologies. This book attempts to cover all the important facets related to wide bandgap semiconductor technology, including new challenges posed by it. This book is intended for graduate students, researchers, engineers, and technology experts who have been working in the exciting fields of SiC and GaN power devices.

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