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Industrial and Technological Applications of Power Electronics Systems

Edited by
Ryszard Strzelecki, Galina Demidova and Dmitri Vinnikov

Printed Edition of the Special Issue Published in *Energies*

www.mdpi.com/journal/energies

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This is a reprint of articles from the Special Issue published online in the open access journal *Energies* (ISSN 1996-1073) (available at: https://www.mdpi.com/journal/energies/special_issues/Applications_of_Power_Electronics_Systems).

For citation purposes, cite each article independently as indicated on the article page online and as indicated below:

LastName, A.A.; LastName, B.B.; LastName, C.C. Article Title. *Journal Name* **Year**, *Volume Number*, Page Range.

ISBN 978-3-0365-0822-1 (Hbk)
ISBN 978-3-0365-0823-8 (PDF)

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About the Editors

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Dmitri Vinnikov Guest Editor 3: Prof. Dr. Dmitri Vinnikov Dmitri Vinnikov was born in Tallinn, Estonia, in 1976. He received the Dipl.Eng., M.Sc., and Dr.Sc.techn. degrees in Electrical Engineering from Tallinn University of Technology, Tallinn, Estonia, in 1999, 2001, and 2005, respectively. He is currently a Research Professor and the Head of the Power Electronics Group, Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology (Estonia), and a visiting professor in the Faculty of Control System and Robotics, ITMO University, Saint Petersburg, Russia. He is the Head of R&D and co-founder of Ubik Solutions LLC.— an Estonian start-up company dedicated to innovative & smart power electronics for renewable energy systems. Moreover, he is one of the founders and leading researchers of ZEBE—the Estonian Centre of Excellence, performing research toward the development of zero energy and resource efficient smart buildings and districts. He has authored or co-authored two books, five monographs, and one book chapter, as well as more than 300 published papers on power converter design and development, and is the holder of numerous patents and utility models in this field. His research interests include applied designs of power electronic converters and control systems, renewable energy conversion systems (photovoltaic and wind), impedance-source power converters, and implementation of wide bandgap power semiconductors. D. Vinnikov is a Chair of the IEEE Estonia Section .

Preface to "Industrial and Technological Applications of Power Electronics Systems"

Since the turn of the century, interest in electrical power systems has been growing steadily, in part due to a tendency to move from directly controlled to intelligent autonomous energy systems. In particular, the increasing presence of renewable energy sources and the development of novel technologies, which demand active and often ultra-precise power supply systems, have generated extensive research in the area of advanced power electronics systems. The importance and scope of the application of regulated power sources in various technological systems are also growing, e.g., using plasma, ultrasounds, and superconductors. Furthermore, researchers pay great attention to loads in these systems, which are mostly represented by various types of electric drives that should be energy efficient. Hence, the main role in many modern technologies and industrial systems is to diversify power electronics converters by applying new topologies, components, and smart controls, where emphasis is placed on such merits as wide input voltage, load regulation range, improved quality of the input and output parameters, high control flexibility, and low cost. To promote research, and accelerate the transfer of knowledge and experience in the above areas, we propose a Special Issue of Energies on industrial and technological applications of power electronics systems. An important premise of this Special Issue would be the synergy effect derived from a combination of views and approaches from various power electronics application areas.

Ryszard Strzelecki, Galina Demidova , Dmitri Vinnikov
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Article

A Parallel Estimation System of Stator Resistance and Rotor Speed for Active Disturbance Rejection Control of Six-Phase Induction Motor

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Received: 3 February 2020; Accepted: 24 February 2020; Published: 2 March 2020

Abstract: In this paper, a parallel estimation system of the stator resistance and the rotor speed is proposed in speed sensorless six-phase induction motor (6PIM) drive. First, a full-order observer is presented to provide the stator current and the rotor flux. Then, an adaptive control law is designed using the Lyapunov stability theorem to estimate the rotor speed. In parallel, a stator resistance identification scheme is proposed using more degrees of freedom of the 6PIM, which is also based on the Lyapunov stability theorem. The main advantage of the proposed method is that the stator resistance adaptation is completely decoupled from the rotor speed estimation algorithm. To increase the robustness of the drive system against external disturbances, noises, and parameter uncertainties, an active disturbance rejection controller (ADRC) is introduced in direct torque control (DTC) of the 6PIM. The experimental results clarify the effectiveness of the proposed approaches.

Keywords: active disturbance rejection controller (ADRC); direct torque control (DTC); full-order observer; sensorless; six-phase induction motor (6PIM); stator resistance estimator

1. Introduction

Three-phase induction motor drives have become a mature technology in the last years, but investigations into concepts of multiphase induction motor drives are still taking place. Multiphase drive systems have a nearly 40-year history of research and study due to their promising advantages against the conventional three-phase systems. The phase redundancy of the multiphase drives provides extra merits such as fault-tolerant operation, series-connected multimotor drive systems, asymmetry and braking systems. Six-phase induction motors (6PIMs) are known for its fault-tolerant capability, low rate of inverter switches, and low DC-link voltage utilization compared with its three-phase one [1–3]. On the other hand, the modular three-phase structure of the 6PIM allows the use of well-known three-phase technologies. The 6PIM is successfully used in special applications, such as electric ships, electric aircrafts, electric vehicles, and melt pumps, where the high reliability and continuity of the operation are critical factors for the system [4]. The phase redundancy of the 6PIM provides the ability of the open-phase fault-tolerant operation without any extra electronic components [5,6].

Among different structures of the 6PIM [4], the asymmetrical 6PIM with double isolated neutral points, which consists of two sets of three-phase windings spatially shifted by 30 electrical degrees,

has attracted the interest of many researchers [7–10]. The traditional three-phase control strategies, including switching table-based direct torque control (ST-DTC) [7], modulation-based DTC [8], the field-oriented control (FOC) [9], and finite control set-model predictive control (FCS-MPC) [10], can be extended to 6PIM (or other multi-phase machines) with some modifications to use more freedom degrees that exist in multi-phase machines. DTC is a well-accepted technique due to its simplicity, quick dynamics, and robustness [11]. The modulation-based DTC strategy offers better phase current, torque, and flux response. On the contrary, this method has more complexity against conventional ST-DTC. The ST-DTC approach has straightforward and simple structure, but it is completely overshadowed by low-order harmonics due to unused voltage vectors in the losses subspaces. To overcome this restriction, the idea of duty cycle control is introduced by several researchers [12,13].

The rapid development of intelligent and high-performance control technologies has also brought about changes in the adjustable speed drive system for different industrial applications [14,15]. To operate safely and reliably under different conditions, there is a lot of debate nowadays about the main control strategy of the system [16,17]. Among different high-performance control strategies of drive systems, the DTC strategy has a straightforward algorithm. The DTC technique is inherently speed sensorless. Nevertheless, if an outer speed loop is added to the DTC, the speed value is also necessary. Sensorless three/multi-phase induction machine drives are widely addressed in the technical literature due to multiple shortcomings of shaft encoders [18–23]. To investigate the instability problem of the traditional rotor flux-based model reference adaptive system (MRAS) speed estimators in the regenerating-mode low-speed operation, a stator current-based and back electromotive force-based MRASs are addressed in [19,20], respectively. In [21], two modified adaptation mechanisms are proposed to replace the classical proportional-integral (PI) regulator. The full-order Luenberger and Kalman filter observers are discussed in [22,23], respectively. Providing a DTC drive system with parallel identification of the rotor speed and the stator resistance is a challenging task because the operation of the DTC scheme is severely dependent on the stator resistance. This problem is sporadically reported for three-phase induction machines (3PIMs) [24,25], where the rotor speed and the stator resistance estimators encounter an overlap due to limited freedom degrees of 3PIM. In this paper, the problem of parallel estimation is investigated using more freedom degrees of 6PIM.

The outer speed control loop of the DTC scheme conventionally contains the PI regulator to obtain torque command from speed error. In general, the control law of a PID regulator is a linear combination of proportional-integral-derivative terms, which is suitable for linear systems. For nonlinear systems, such as the 6PIM drive system, the PI regulator has been given a lot of attention due to its simplicity. However, it suffers from multiple problems including: (1) tuning of its parameters; (2) high sensitivity against noise and external disturbances; and (3) loss of efficiency due to oversimplified control law [26,27]. One promising technique to relatively get rid of the drawbacks of PI regulator is active disturbance rejection controller (ADRC) [26,28]. The ADRC is a nonlinear control scheme, which provides a robust control against noises, external disturbances, and parameter uncertainties. For these reasons, the ADRC technique has recently attracted more attention for electric drive systems. To address this issue, a modified FOC scheme based on first-order ADRCs for current and speed control loops is proposed in [29]. A combined active disturbance rejection and sliding-mode controller for an induction motor is presented to achieve total robustness [30].

The aim of this paper is to present an ADRC-based DTC scheme for sensorless 6PIM drives. The speed estimator is based on adaptive full-order observer, and its control law is designed using Lyapunov stability theorem. Besides the speed estimation system, a stator resistance estimator is proposed using additional degrees of freedom of the 6PIM to enhance the robustness of the sensorless DTC strategy against stator resistance uncertainties. The adaptation law for the stator resistance estimator is derived using the Lyapunov stability theorem to ensure its overall convergence.

The rest of this paper is organized as follows. Section 2 introduces the mathematical model of the 6PIM. Section 3 presents the design procedure of the adaptive full-order observer, the speed estimator,

and the stator resistance estimator. The DTC scheme of the 6PIM is discussed in Section 4, which includes the ST-DTC scheme, and ADRC in DTC. The experimental results are presented in Section 5. Finally, Section 6 summarizes the findings and concludes the paper.

2. Dynamic Model of 6PIM

There are two popular approaches for modeling of the multi-phase machines: (1) multiple d–q approach [9]; (2) vector space decomposition (VSD) approach [31]. The first method is exclusively used for modular three-phase structures-based multi-phase machines such as six-phase and nine-phase machines. However, the second method can be used for all types of multi-phase machines. In this research, the VSD approach is used, where a 6PIM with distributed windings is modeled in the three orthogonal subspaces, i.e., the $\alpha - \beta$, $z_1 - z_2$ and $o_1 - o_2$. Among them, only the $\alpha - \beta$ variables are in relation with electromechanical energy conversion, while $z_1 - z_2$ and $o_1 - o_2$ variables do not actively contribute to the torque production.

The schematic diagram of a six-phase voltage source inverter (VSI)-fed an 6PIM with two isolated neutral points is shown in Figure 1. The transfer between the normal $a - x - b - y - c - z$ variables and $\alpha - \beta - z_1 - z_2 - o_1 - o_2$ variables is performed by $\boldsymbol{T}_6$ transformation matrix as follows [31]:

$$\boldsymbol{T}_6 = \frac{1}{3}\begin{bmatrix} 1 & \frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 \\ 1 & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{2} & \frac{\sqrt{3}}{2} & -1 \\ 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \end{bmatrix} \tag{1}$$

By applying $\boldsymbol{T}_6$ matrix to the voltage equations in the original six-dimensional system, the 6PIM model can be represented in the three orthogonal submodels, identified as $\alpha - \beta$, $z_1 - z_2$, and $o_1 - o_2$. The voltage space vector equations of the 6PIM in the $\alpha - \beta$ subspace are written as follows:

$$\boldsymbol{v}_s = R_s \boldsymbol{i}_s + p\boldsymbol{\Psi}_s \tag{2}$$

$$0 = R_r \boldsymbol{i}_r + p\boldsymbol{\Psi}_r - j\omega_r \boldsymbol{\Psi}_r \tag{3}$$

The flux linkages are

$$\boldsymbol{\Psi}_s = L_s \boldsymbol{i}_s + L_m \boldsymbol{i}_r \tag{4}$$

$$\boldsymbol{\Psi}_r = L_m \boldsymbol{i}_s + L_r \boldsymbol{i}_r \tag{5}$$

where $\boldsymbol{v}$, $\boldsymbol{i}$, $\boldsymbol{\Psi}$, R, and L represent voltage, current, flux linkage, resistance, and inductance, respectively, for stator (s subscript) and rotor (r subscript) quantities, and p denotes derivative operator. The electromagnetic torque produced by the 6PIM is expressed as

$$T_e = 3P\boldsymbol{\Psi}_s \otimes \boldsymbol{i}_s \tag{6}$$

where P is pole pairs and $\otimes$ denotes the cross product.

The 6PIM voltage equations in the $z_1 - z_2$ subspace are the same as a passive R-L circuit as follows:

$$v_{sz1} = R_s i_{sz1} + L_{ls} p i_{sz1} \tag{7}$$

$$v_{sz2} = R_s i_{sz2} + L_{ls} p i_{sz2} \tag{8}$$

where L_{ls} is stator leakage inductance.

On the presumption that the stator mutual leakage inductances can be neglected, the 6PIM model in the $o_1 - o_2$ subspace has the same form of the $z_1 - z_2$ subspace. However, the applied 6PIM with

two isolated neutral points avoids zero-sequence currents because it contains two sets of balanced three-phase windings.

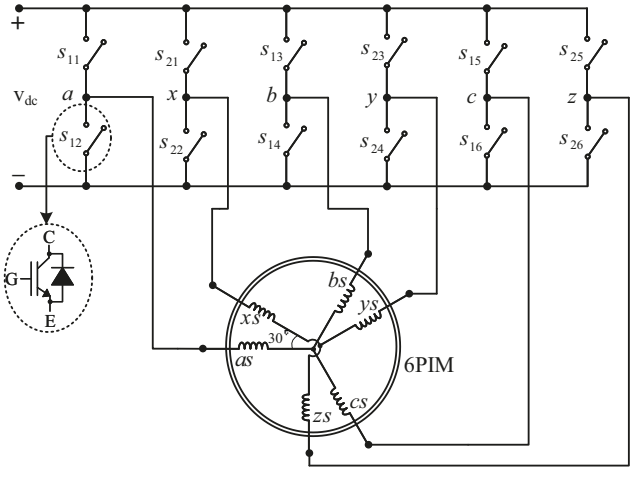


Figure 1. Six-phase two-level VSI-fed 6PIM.

3. Adaptive Full-Order Observer

The block diagram of the proposed R_s and ω_r estimators based on the adaptive state observer is shown in Figure 2. It contains the stator current and rotor flux observers, the stator resistance identifier, and the rotor speed estimator, which are discussed below.

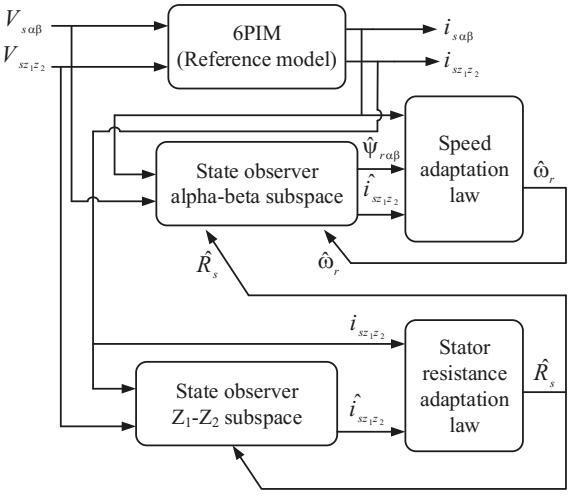


Figure 2. The block diagram of the proposed parallel estimation system of the stator resistance and the rotor speed based on an adaptive full-order observer.

3.1. Stator Current and Rotor Flux Observers

The general form of state-space model of the 6PIM in the $\alpha - \beta$ subspace is

$$\begin{cases} \dot{x}_1 = A_1 x_1 + B_1 u_1 \\ y_1 = C_1 x + D_1 u_1 \end{cases} \tag{9}$$

Assuming stator current and rotor flux as state variables and using Equations (2) and (3), the elements of state-space representation in $\alpha - \beta$ subspace will be

$$x_1 = \begin{bmatrix} i_{s\alpha} & i_{s\beta} & \psi_{r\alpha} & \psi_{r\beta} \end{bmatrix}^T \tag{10}$$

$$A_1 = \begin{bmatrix} (-\frac{R_s}{\sigma L_s} - \frac{1-\sigma}{\sigma T_r})I & \frac{L_m}{\sigma L_s L_r}(\frac{1}{T_r}I - \omega_r J) \\ \frac{L_m}{T_r}I & -\frac{1}{T_r}I + \omega_r J \end{bmatrix} \tag{11}$$

$$B_1 = \begin{bmatrix} \frac{1}{\sigma L_s}I & O \end{bmatrix}^T \tag{12}$$

$$u_1 = \begin{bmatrix} v_{s\alpha} & v_{s\beta} \end{bmatrix}^T \tag{13}$$

$$y_1 = \begin{bmatrix} i_{s\alpha} & i_{s\beta} \end{bmatrix}^T \tag{14}$$

$$C_1 = \begin{bmatrix} I & O \end{bmatrix} \tag{15}$$

with

$$I = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, J = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}, O = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{16}$$

where $T_r = L_r / R_r$ is rotor time constant and $\sigma = 1 - L_m^2 / L_s L_r$ is leakage coefficient.

The state observer of the 6PIM has a similar form of state-space representation except that an additional compensation term based on error of measurable states and observer gain matrix is added to it. The state observer can be written as

$$\begin{cases} \dot{\hat{x}}_1 = \hat{A}_1 \hat{x}_1 + B_1 u_1 + G_1(\boldsymbol{i}_s - \hat{\boldsymbol{i}}_s) \\ \hat{y}_1 = C_1 \hat{x}_1 \end{cases} \tag{17}$$

where the marker $\hat{}$ indicates the estimated values, and G_1 is the observer gain matrix. The matrix A_1 contains unknown parameters of the 6PIM such as the rotor speed and the stator resistance. These parameters can be estimated by the designing of a suitable adaptation control law with a nonlinear theorem such as a Lyapunov stability theorem. It is worth mentioning here that the matrix A_1 also contains the rotor time constant. However, simultaneous estimation of the rotor speed, the rotor time constant, and the stator resistance is challenging because of persistency of excitation conditions problem [32]. Some techniques have recently been developed based on signal injection to provide persistent excitation [33], which suffer from steady-state torque and speed ripples. In this paper, the stator resistance is estimated from additional degrees of freedom of the 6PIM, while the rotor speed is provided using the 6PIM equations in $\alpha - \beta$ subspace. This procedure provides the stator resistance independent from the rotor speed.

The observer gain matrix G_1 must be designed to ensure stability and good dynamic response of the observer at a wide range of the speeds. Using pole-placement method, the elements of matrix G_1 is provided as [22,34]

$$G_1 = \begin{bmatrix} g_1 & g_2 & g_3 & g_4 \\ -g_2 & g_1 & -g_4 & g_3 \end{bmatrix}^T \tag{18}$$

where

$$\begin{cases} g_1 = (1 - K_{po})(R_s L_r^2 + R_r L_m^2) / \sigma L_s L_r^2 \\ g_2 = (K_{po} - 1)\hat{\omega}_r \\ g_3 = (K_{po} - 1)(R_s L_s - K_{po} R_s L_r) / L_m \\ g_4 = (1 - K_{po})\hat{\omega}_r \sigma L_s L_r / L_m \end{cases} \tag{19}$$

where $K_{po} > 0$ is observer constant gain.

3.2. Stator Resistance Identification

In this paper, a stator resistance adaptation system is proposed using the machine model in the $z_1 - z_2$ subspace. This method can be utilized for any multi-phase machines. It is completely decoupled from the rotor speed and the rotor time constant, whereas most of the conventional stator resistance estimators, developed for three-phase machines, are related to these parameters. The proposed R_s estimator only depends on the stator leakage inductance L_{ls}, which can be approximately assumed to be constant.

The state-space model of 6PIM in the $z_1 - z_2$ subspace, with consideration of i_{sz1} and i_{sz2} as the state variables, can be derived from Equations (7) and (8) as follows:

$$\begin{bmatrix} \dot{i}_{sz1} \\ \dot{i}_{sz2} \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L_{ls}} & 0 \\ 0 & -\frac{R_s}{L_{ls}} \end{bmatrix} \begin{bmatrix} i_{sz1} \\ i_{sz2} \end{bmatrix} + \frac{1}{L_{ls}} \begin{bmatrix} v_{sz1} \\ v_{sz2} \end{bmatrix}$$
$$\begin{bmatrix} i_{sz1} \\ i_{sz2} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_{sz1} \\ i_{sz2} \end{bmatrix} \tag{20}$$

In this case, the proposed states observer is given by

$$\begin{cases} \dot{\hat{x}}_2 = \hat{A}_2 \hat{x}_2 + B_2 u_2 \\ \hat{y}_2 = C_2 \hat{x}_2 \end{cases} \tag{21}$$

It should be noted that a correction term $G_2(\boldsymbol{x_2} - \hat{\boldsymbol{x}}_2)$ is neglected in Equation (21) due to the inherent stability of the observer.

The proposed adaptation law for the stator resistance estimation is

$$\hat{R}_s = K_{pr} \epsilon_{R_S} + K_{ir} \int \epsilon_{R_S} dt \tag{22}$$

where K_{ir} and K_{pr} are the integral and proportional gains, respectively, and ϵ_{R_S} is the stator resistance error signal

$$\epsilon_{R_S} = \hat{i}_{sz1}(i_{sz1} - \hat{i}_{sz1}) + \hat{i}_{sz2}(i_{sz2} - \hat{i}_{sz2}) \tag{23}$$

The proof for the stator resistance adaptation law is presented in Appendix A.

3.3. Rotor Speed Estimation

In order to design the speed adaptation law, it is considered as an unknown parameter. First, an appropriate positive definite function is chosen as the Lyapunov candidate. Then, the adaptation law is obtained using the Lyapunov criterion to ensure asymptotic stability of the system. The speed adaptation law is

$$\hat{\omega}_r = K_{p\omega} \epsilon_\omega + K_{i\omega} \int \epsilon_\omega dt \tag{24}$$

where $K_{p\omega}$ and $K_{i\omega}$ are proportional and integral gains, respectively, and ϵ_ω is the speed error signal as follows:

$$\epsilon_\omega = (i_{s\alpha} - \hat{i}_{s\alpha})\hat{\psi}_{r\beta} - (i_{s\beta} - \hat{i}_{s\beta})\hat{\psi}_{r\alpha} \tag{25}$$

The proof for the speed adaptation law is presented in Appendix B.

4. DTC of 6PIM

4.1. ST-DTC Scheme

A six-phase VSI contains overall $2^6 = 64$ different voltage space vectors, 60 active, and four zero vectors, where the active voltage vectors are distributed in four non-zero levels depicted in Figure 3. The electrical angle of each sectors is 30°. The 6PIM phase-to-neutral voltages can be calculated as

$$\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_x \\ V_y \\ V_z \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 & 0 & 0 & 0 \\ -1 & 2 & -1 & 0 & 0 & 0 \\ -1 & -1 & 2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2 & -1 & -1 \\ 0 & 0 & 0 & -1 & 2 & -1 \\ 0 & 0 & 0 & -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \\ S_x \\ S_y \\ S_z \end{bmatrix} \tag{26}$$

where $S_i = \{0, 1\}, i = \{a, x, b, y, c, z\}$ is the switching state. When $S_i = 1$ ($S_i = 0$), the corresponding stator terminal is connected to positive (negative) DC-link rail. The voltage space vectors are given by

$$v_s = \frac{1}{3}[V_a + aV_x + a^4V_b + a^5V_y + a^8V_c + a^9V_z] \tag{27}$$

$$v_z = \frac{1}{3}[V_a + a^5V_x + a^8V_b + aV_y + a^4V_c + a^9V_z] \tag{28}$$

where $v_z = v_{sz1} + jv_{sz2}$ and $a = e^{j\pi/6}$.

The flux estimator is obtained from

$$\psi_{s\alpha} = \int (v_{s\alpha} - \hat{R}_s i_{s\alpha}) dt \tag{29}$$

$$\psi_{s\beta} = \int (v_{s\beta} - \hat{R}_s i_{s\beta}) dt \tag{30}$$

and the toque estimator is obtained from (6). In the traditional ST-DTC, the torque and stator flux errors are applied to hysteresis regulators to provide the sign of torque (ϵ_T) and stator flux (ϵ_ψ). According to gained signals and also the position of stator flux, a proper large voltage vector is selected based on Table 1 during each sampling period. From Figure 3, the corresponding voltage vectors in the $z_1 - z_2$ subspace will produce large current harmonics, when only large voltage vectors are used to control the torque and flux. Hence, it can alleviate the current harmonics through reduction of the $z_1 - z_2$ components by applying a combined voltage vector during each sampling period. This technique is referred to as duty cycle control, where a virtual vector (synthesized by large and medium voltage space vectors) is applied to the inverter in each sampling period because the large and medium voltage vectors are in the opposite direction in the $z_1 - z_2$ subspace (see Figure 3). The duration of the applied vectors is calculated in order to reduce the average volt-seconds in the $z_1 - z_2$ subspace [4]. The block diagram of the proposed sensorless DTC strategy with the adaptive full-order observer is shown in Figure 4a. In this figure, the speed control loop is based on the ADRC strategy, which will be discussed in the next subsection.

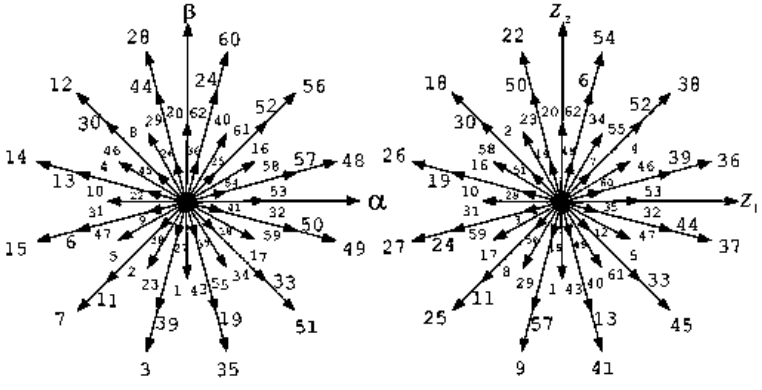
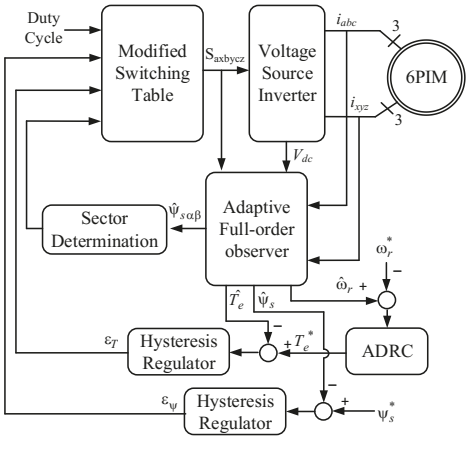


Figure 3. The $\alpha - \beta$ (top side) and the $z_1 - z_2$ (down side) vector subspaces for a six-phase VSI.

Table 1. Switching table of DTC strategy.

ϵ_T	ϵ_ψ	Selected Voltage *
1	1	V_{m+1}
1	0	V_{m+4}
0	1	V_0
0	0	V_0
−1	1	V_{m-2}
−1	0	V_{m-5}

* m is sector number.



(**a**)

Figure 4. *Cont*.

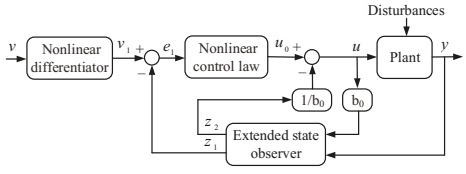


Figure 4. Block diagram of (**a**) the proposed sensorless DTC strategy; (**b**) ADRC.

4.2. ADRC in DTC

To enhance the robustness of the DTC technique against external disturbances and measurement noises, the ADRC is proposed to replace with the conventional PI regulator in the outer speed control loop. The block diagram of ADRC is shown in Figure 4b. It consists of three main elements: (1) nonlinear differentiator; (2) extended state observer; (3) nonlinear control law.

In some industrial applications, the command values are changed as step function, which is not suitable for the control system because of a sudden jump of output and control signals. To solve this problem, the nonlinear differentiator is used, which makes a reasonable transient profile from command signals for tracking [26]. The nonlinear differentiator can be expressed by

$$\begin{cases} v_1(k+1) = v_1(k) + hv_2(k) \\ v_2(k+1) = v_2(k) + hf_1(v_1(k) - v(k), v_2(k), r_0, h_0) \end{cases} \tag{31}$$

where f_1 is a nonlinear function as

$$f_1(v_1(k), v_2(k), r_0, h_0) = -\begin{cases} a(k)/h_0 & |a(k)| \le r_0 h_0 \\ r_0 \text{sign}(a(k)) & |a(k)| > r_0 h_0 \end{cases} \tag{32}$$

with

$$a(k) = \begin{cases} v_2(k) + y_0(k)/h_0 & |a(k)| \le r_0 h_0^2 \\ v_2(k) + (a_0(k) - r_0 h_0)/2 & |a(k)| > r_0 h_0^2 \end{cases}$$

$$y_0(k) = v_1(k) + h_0 v_2(k)$$

$$a_0(k) = \sqrt{(r_0 h_0)^2 + 8r_0|y_0(k)|}$$

where r_0 and h_0 are the parameters of the nonlinear differentiator, and h is sampling period.

The extended state observer is an enhanced version of feedback linearization method to compensate the total disturbances of the system. Using this observer, the state feedback term can be estimated online; hence, it is an adaptive robust observer against model uncertainties and external disturbances. The extended state observer is represented as follows:

$$\begin{cases} z_1(k+1) = z_1(k) + h[z_2(k) - \beta_1 f_2(e(k), \alpha_1, \delta_1) + b_0 u(k)] \\ z_2(k+1) = z_2(k) - h\beta_2 f_2(e(k), \alpha_1, \delta_1) \\ e(k) = z_1(k) - y(k) \end{cases} \tag{33}$$

where the nonlinear function f_2 is defined as

$$f_2(e(k), \alpha, \delta) = \begin{cases} e(k)/\delta^{1-\alpha} & |e(k)| \le \delta \\ |e(k)|^{\alpha} \text{sign}(e(k)) & |e(k)| > \delta \end{cases} \tag{34}$$

where α_1, δ_1, β_1, β_2, and b_0 are the parameters of the extended state observer.

The conventional PI controller is based on the linear combination of proportional and integral terms of error, which may degrade the performance of the DTC scheme. Different nonlinear combination of error can be presented to overcome this problem. In this paper, the following nonlinear control law is used:

$$\begin{cases} e_1(k) = v_1(k) - z_1(k) \\ u_0(k) = \beta_3 f_2(e_1(k), \alpha_2, \delta_2) \\ u(k) = u_0(k) - z_2(k)/b_0 \end{cases} \quad (35)$$

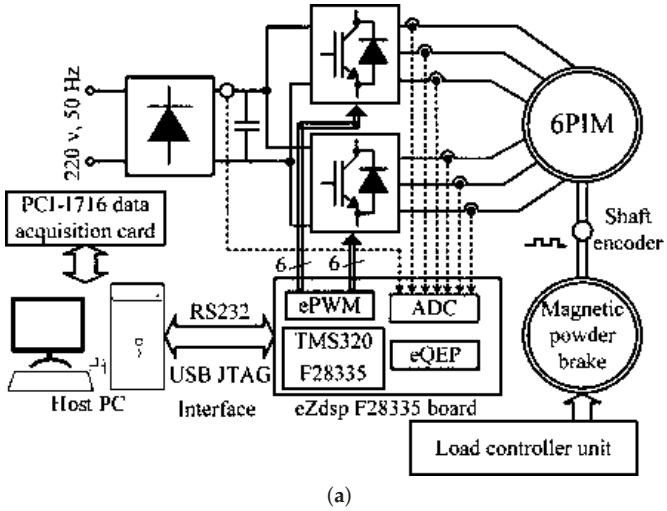
where α_2, β_3, and δ_2 are the parameters of nonlinear control law.

5. Experimental Validation

5.1. Description of Experimental Setup

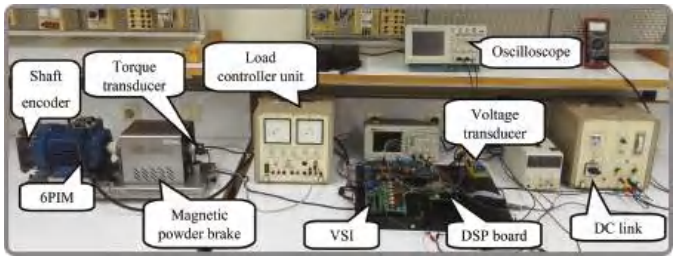
The schematic and photograph of the experimental setup are shown in Figure 5a,b, respectively. The principal elements are

- a TMS320F28335-based digital signal processor (DSP) board.
- two custom-made two-level three-phase VSIs based on BUP 314D IGBTs and LEM LTS 6-NP current transducers.
- an LEM LV25-P voltage transducer.
- an Autonics incremental shaft encoder.
- a magnetic powder brake mechanically coupled to the 6PIM.
- a bridge rectifier.
- a 1-hp three-phase induction motor, which has been rewound to provide an asymmetrical 6PIM. The specifications of the 6PIM are shown in Table 2.



(**a**)

Figure 5. *Cont.*



(**b**)

Figure 5. Experimental setup (**a**) schematic (**b**) photograph.

Table 2. The parameters of 6PIM.

Symbol	Quantity	Value
T_n	Nominal torque	2 Nm
P	Pole pairs	1
R_s	Stator resistance	4.08 Ω
R_r	Rotor resistance	3.73 Ω
L_s	Stator inductance	443.6 mH
L_r	Rotor inductance	443.6 mH
L_m	Magnetizing inductance	429.8 mH
J	Moment of inertia	0.000718 kg·m^2

5.2. Experimental Results

The performance of the proposed sensorless DTC strategy has been experimentally surveyed using DSP platform, programmed through Code Composer Studio (CCS v.3.3) and MATLAB. The IQmath and digital motor control (DMC) libraries have been used to provide optimized code. A 10 kHz sampling frequency with a 2 μs dead-band has been adopted. The experimental results have been captured using an Advantech PCI-1716 data acquisition card (DAQ) and serial port with LABVIEW and MATLAB, respectively. The serial communications interface (SCI) module has been employed to provide a serial connection between host PC and DSP. An incremental shaft encoder has been used to verify the performance of the speed estimation algorithm. All of the experiments have been carried out in sensorless mode as well as closed-loop adaptation of the stator resistance under various test scenarios, emphasizing on the low-speed region.

The experimental results of the proposed parallel estimation system of stator resistance and rotor speed under 50% initial stator resistance mismatch are shown in Figure 6. The speed command is 7% rated speed under rated load torque. In this test, the electric drive is allowed to start with a wrong stator resistance. This causes an error in estimated electromagnetic torque and actual speed. However, the estimated speed and the stator flux follow their reference values because of the controller action. It can be seen that the estimation error of the speed and the electromagnetic torque due to detuned stator resistance are removed within short seconds after activation of the stator resistance estimator at $t = 5$ s.

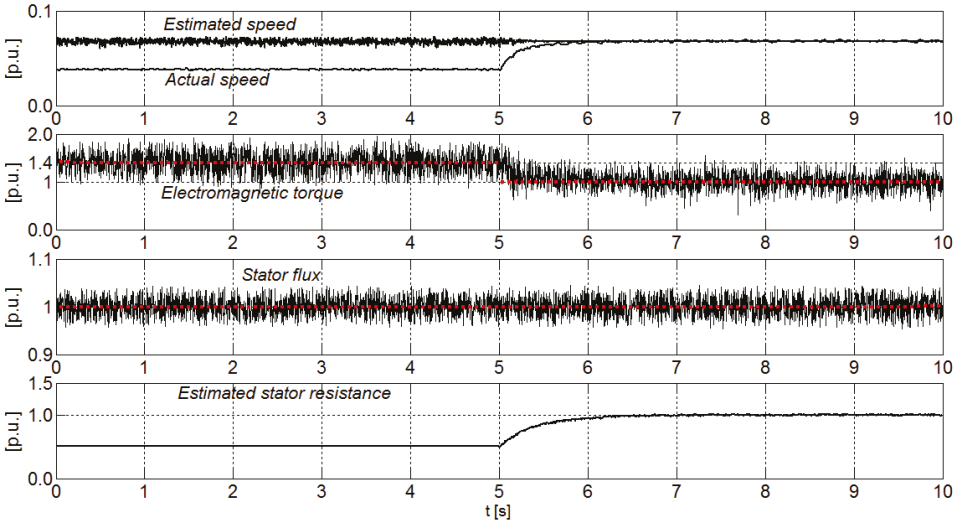
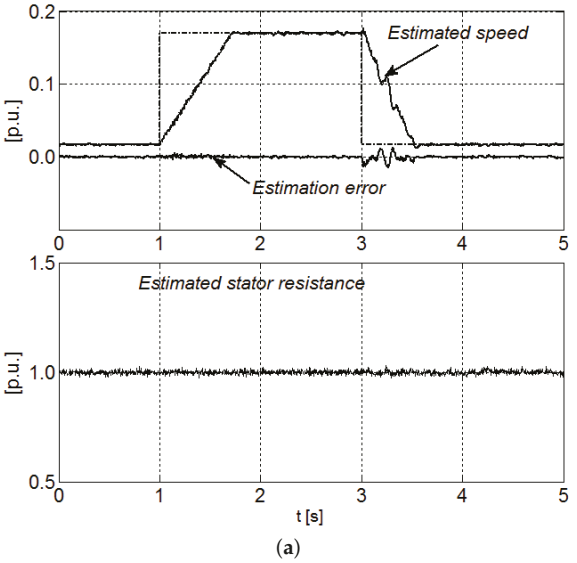


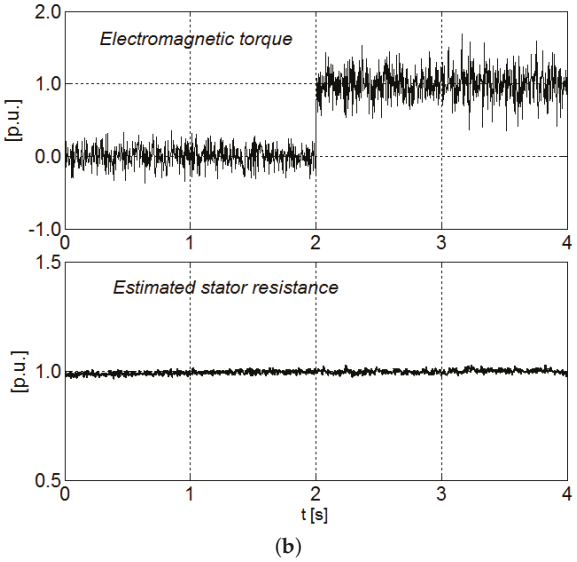
Figure 6. Experimental results of the proposed parallel estimation system under initial mismatch of stator resistance.

As already mentioned, the proposed parallel estimation system has the merit of avoiding overlap between stator resistance and rotor speed estimators, whereby the stator resistance is independently estimated from rotor speed using additional freedom degrees of 6PIM. The experimental results of estimated stator resistance under speed changes and load change are shown in Figure 7a,b, respectively. In Figure 7a, the speed command is changed as a step function from a very low speed to 17% rated speed, and, in Figure 7b, a load torque is suddenly applied to the motor at $t = 2$ s. It can be clearly adjudged that the adaptation process of stator resistance is independent of speed and load torque changes.

Disturbance-free operation of the ADRC-based speed controller is evaluated through a comparative study of its performance and the conventional PI regulator. The experimental results for the estimated speed under sudden load torque changes at 7% rated speed when the conventional PI and introduced ADRC are utilized as speed controllers are shown in Figure 8. As can be seen, applying the external load torque to the 6PIM leads to a larger overshoot (undershoot), when the conventional PI regulator is employed. The ADRC properly improves the disturbance rejecting capability, which in turn provides a robust performance against load torque changes.



(**a**)



(**b**)

Figure 7. Experimental results of the estimated stator resistance under (**a**) speed changes (**b**) load torque change.

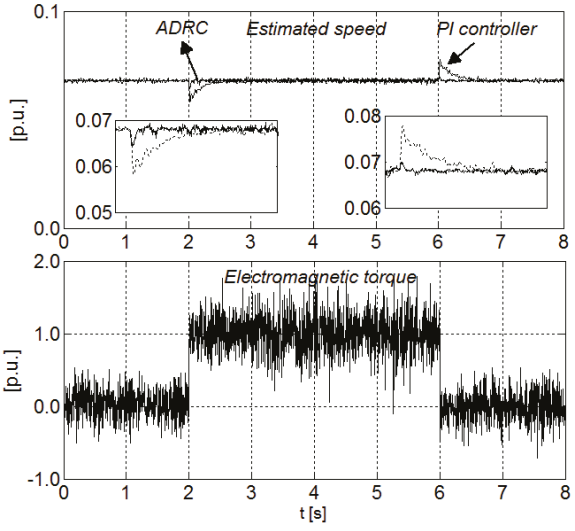


Figure 8. Experimental results of the estimated speed with PI and ADRC-based speed controllers under load changes.

6. Conclusions

Multiphase electrical machines and drives have different advantages over their traditional three phase counterparts. In recent years, multiple research works have been published to explore the specific advantages of multiphase machines and drives. In this regard, a parallel estimation system of the stator resistance and the rotor speed for direct torque-controlled 6PIM was proposed in this paper. The speed estimator is based on an adaptive full-order observer, which estimates the speed signal using the 6PIM model in the $\alpha - \beta$ subspace, while the stator resistance estimator employs the 6PIM model in the $z_1 - z_2$ subspace. Hence, the stator resistance is identified independently of the rotor speed. The rotor speed- and the stator resistance-adaptation laws were derived using the Lyapunov stability theorem. The performance of the proposed sensorless DTC was experimentally investigated, where the obtained results confirmed its capabilities in terms of accuracy as well as no overlap between the stator resistance and the rotor speed estimators. In order to provide a robust performance for the DTC technique against external load torques, the PI regulator was replaced by an ADRC, as a well-known disturbance-free controller. The better performance of the DTC scheme based on ADRC was verified through a comparative study with the conventional PI regulator.

Author Contributions: Conceptualization, methodology, validation, formal analysis, writing–original draft preparation, H.H., M.H.H.; writing—review and editing, resources, A.R.; project administration, T.V.; investigation, A.K.; funding acquisition, D.V.L.; supervision, A.B. All authors have read and agreed to the published version of the manuscript.

Funding: The research has been supported by the Estonian Research Council under grant PSG453 "Digital twin for propulsion drive of autonomous electric vehicle" and was financially supported by Government of Russian Federation (Grant 08-08).

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A. The Design of Adaption Law for Stator Resistance Estimation

The quadratic Lyapunov function for asymptotic stability of the proposed stator resistance estimation system is defined as

$$\boldsymbol{V}_r = \boldsymbol{e_r}^T \boldsymbol{e_r} + \frac{\Delta R_s^2}{\lambda_r} \tag{A1}$$

where λ_r is a positive constant, $\Delta R_s = \hat{R}_s - R_s$, $\hat{R}_s$ is the estimated stator resistance, R_s is the real stator resistance, and $\boldsymbol{e}_r$ is the error matrix of the state variables in the $z_1 - z_2$ subspace as

$$\boldsymbol{e}_r = \boldsymbol{x}_2 - \hat{\boldsymbol{x}}_2 = \begin{bmatrix} i_{sz1} - \hat{i}_{sz1} & i_{sz2} - \hat{i}_{sz2} \end{bmatrix}^T \tag{A2}$$

The asymptotic stability of the stator resistance estimator is assured when the Lyapunov candidate function $\boldsymbol{V}_r$ is positive definite as well as its time derivative $p\boldsymbol{V}_r$ is negative definite. The time derivative of the Lyapunov candidate function is calculated as

$$p\boldsymbol{V}_r = \boldsymbol{e}_r^T p\boldsymbol{e}_r + p\boldsymbol{e}_r^T \boldsymbol{e}_r + \frac{2}{\lambda_r} \Delta R_s p\hat{R}_s \tag{A3}$$

With some mathematical manipulation, Equation (A3) can be written as

$$\begin{aligned} p\boldsymbol{V}_r = {} & \boldsymbol{e}_r^T (A_2 + A_2^T)\boldsymbol{e}_r - [\boldsymbol{e}_r^T \Delta A_2 \hat{x} + \hat{x}_2^T \Delta A_2^T \boldsymbol{e}_r] \\ & + \frac{2}{\lambda_r} \Delta R_s p\hat{R}_s \end{aligned} \tag{A4}$$

The first term of Equation (A4) is inherently negative definite. The stability of the system is eventually assured, when the sum of the last two terms of Equation (A4) is zero as

$$\frac{2}{\lambda_r} \Delta R_s p\hat{R}_s - [\boldsymbol{e}_r^T \Delta A_2 \hat{x}_2 + \hat{x}_2^T \Delta A_2^T \boldsymbol{e}_r] = 0 \tag{A5}$$

which leads to

$$\hat{R}_s = -\frac{\lambda_r}{2} \int \epsilon_{R_S} dt \tag{A6}$$

where the tuning signal ϵ_{R_S} is

$$\epsilon_{R_S} = \hat{i}_{sz1}(i_{sz1} - \hat{i}_{sz1}) + \hat{i}_{sz2}(i_{sz2} - \hat{i}_{sz2}) \tag{A7}$$

A PI regulator is employed to enhance the dynamic behaviour of the proposed estimator, instead of Equation (A6) as

$$\hat{R}_s = K_{pr}\epsilon_{R_S} + K_{ir} \int \epsilon_{R_S} dt \tag{A8}$$

where K_{ir} and K_{pr} are the integral and proportional constants.

Appendix B. The Design of Adaption Law for Speed Estimation

The Lyapunov candidate function for asymptotic stability of the speed estimation system is

$$\boldsymbol{V}_\omega = \boldsymbol{e}_\omega^T \boldsymbol{e}_\omega + \frac{\Delta\omega_r^2}{\lambda_\omega} \tag{A9}$$

where λ_ω is a positive constant, $\Delta\omega_r = \hat{\omega}_r - \omega_r$, and $\boldsymbol{e}_\omega$ is the error matrix of the estimated and real values in $\alpha - \beta$ subspace as

$$\begin{aligned} \boldsymbol{e}_\omega &= \boldsymbol{x}_1 - \hat{\boldsymbol{x}}_1 \\ &= \begin{bmatrix} i_{s\alpha} - \hat{i}_{s\alpha} & i_{s\beta} - \hat{i}_{s\beta} & \psi_{r\alpha} - \hat{\psi}_{r\alpha} & \psi_{r\beta} - \hat{\psi}_{r\beta} \end{bmatrix}^T \end{aligned} \tag{A10}$$

In this case, the first-order time derivative of Lyapunov function can be deduced as

$$pV_\omega = e_\omega^T[(A_1 - G_1C_1) + (A_1 - G_1C_1)^T]e_\omega + (e_\omega \Delta A_2 \hat{x}_2 + \hat{x}_2 \Delta A^T e_\omega) + \frac{2}{\lambda_\omega}\Delta\omega_r p\hat{\omega}_r \quad \text{(A11)}$$

The first term of Equation (A11) is guaranteed to be negative definite by suitable adopting of observer gain matrix G_1. The Lyapunov stability criterion is satisfied, if the sum of second and third terms of Equation (A11) is zero. With some calculations, the adaptation law for speed estimator is acquired as

$$\hat{\omega}_r = K_{p\omega}\epsilon_\omega + K_{i\omega}\int \epsilon_\omega dt \quad \text{(A12)}$$

where the tuning signal ϵ_ω is

$$\epsilon_\omega = (i_{s\alpha} - \hat{i}_{s\alpha})\hat{\psi}_{r\beta} - (i_{s\beta} - \hat{i}_{s\beta})\hat{\psi}_{r\alpha} \quad \text{(A13)}$$

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Adaptive Maximum Torque per Ampere Control of Sensorless Permanent Magnet Motor Drives

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Received: 16 August 2020; Accepted: 24 September 2020; Published: 27 September 2020

Abstract: Interior permanent magnet synchronous motor (IPMSM) efficiency can be improved by using maximum torque per ampere control (MTPA). MTPA control utilizes both alignment and reluctance torques and usually requires information about the magnetization map of the electrical machine. This paper proposes an adaptive MTPA algorithm for sensorless control systems of IPMSM drives, which is applicable in industrial and commercial drives. This algorithm enhances conventional control schemes, where the output of the speed controller is the commanded stator current and the direct current is calculated using an MTPA equation; therefore, it can be easily implemented in the previously developed drives. The proposed algorithm does not use any motor parameters for the calculation of the MTPA trajectory, which is important for systems operating in changing environmental conditions, because motor inductances and flux linkage strongly depend on the stator current and the rotor temperature, respectively. The proposed algorithm continuously varies the current phase and in such a way it tries to minimize the magnitude of the stator current at the applied load torque. The main contribution of this paper is the development of a technique to overcome the main disadvantage of seeking algorithms–the necessity of a precision information about the rotor position. The proposed method was verified experimentally.

Keywords: interior permanent magnet motors; maximum torque per ampere; sensorless control; adaptive control

1. Introduction

Interior permanent magnet synchronous motors (IPMSM), compared with machines of other types, have higher torque to weight ratios, higher efficiency, output power per volume and mass per volume values, which make them attractive for use in compact drives, high-efficient drives, drives with high dynamics, etc. At the same time, the high price of rare-earth metals, which are necessary for producing strong magnets, restricts the popularity of permanent magnet (PM) motors. However, over the past decade, the price of rare-earth magnets has decreased; therefore, the area usage of PM motors is widening. As a result, they attract more attention, and many researchers have investigated the control systems of these machines.

The main feature of IPMSMs is their asymmetry along direct and quadrature axes, which creates reluctance torque. At the same time, permanent magnet synchronous machines (PMSM), which have equal direct and quadrature inductance and idle load conditions, demonstrate magnetic asymmetry at load; thus, they may also produce reluctance torque. As a result, modern efficient control systems must consider these facts and utilize the reluctance torque of the PM motors by employing one of the maximum torque per ampere (MTPA) techniques.

Information on rotor position is required to control PM motors; therefore, precision and high-performance drives are equipped with position encoders, whose resolution depends on the

desired dynamic and precision of control. At the same time, low-cost systems and motor drives with higher reliability have a tendency to eliminate additional parts, especially moving parts, such as speed and position encoders. Therefore, sensorless control algorithms have almost become a standard in these applications [1,2]. Therefore, modern control systems of PM motors, in order to be used in a variety of applications, have to be sensorless [3] and must be able to implement MTPA techniques [4,5].

An analysis of the operating conditions of PM motors and their impact on the motor parameters showed that motor direct and quadrature inductances strongly depend on the motor stator current and may decrease due to steel saturation by more than 50% [6]. At the same time, the temperature of the rotor impacts the flux linkage of magnets and may decrease it by 10% [7]. Furthermore, magnet degradation during the lifetime of the motor may also decrease the flux linkage by 15%. As a result, it would be beneficial to develop an MTPA algorithm, which can adapt to the variations in motor parameter and provide efficient control of the motor, despite its environment.

The conventional MTPA approach involves the calculation of one of the MTPA equations—e.g., Equation (1) obtained from motor equations:

$$i_d = -\frac{\psi_m}{4\left(L_d - L_q\right)} - \sqrt{\frac{\psi_m^2}{16\left(L_d - L_q\right)^2} + \frac{I_s^2}{2}}, \tag{1}$$

where I_s represents the stator current, ψ_m represents the permanent magnet flux linkage, L_d and L_q represent the d-axis and q-axis inductances, respectively, and i_d stands for the direct current component providing the MTPA. This approach is simple and can be easily implemented in a sensorless control systems and is discussed and studied in [8–12]; however, such techniques are sensitive to the variation in motor parameter due to operating conditions. For example, the accurate knowledge of motor parameters was required in [10], but the change in the motor inductances due to the saturation effect was not taken into account.

To solve this problem, different adaptive MTPA techniques were proposed. The authors of [13,14] proposed to enhance the conventional MTPA algorithm with on-line estimation techniques of motor inductances; however, these papers do not suggest a solution for the flux-linkage estimation. Furthermore, these methods need fine-tuning, and the control system has to be equipped with a high-speed processor capable of executing additional calculations at every calculation step, together with basic control routines.

The authors of [15] proposed a method with a fast dynamic response, which uses a recursive least squares (RLS) parameters estimator to track the MTPA trajectory. However, this method calculates many square roots, which significantly load a microcontroller unit (MCU), even with optimizations; therefore, the use of this method is limited.

A group of methods described in [16,17] proposes several similar MTPA techniques which are based on the high-frequency signal injection and the analysis of response. These methods do not need motor parameters, but high-frequency signals cause noises and vibrations, which are undesirable in many drives.

To overcome this problem, the authors of [18–21] proposed an interesting technique called the virtual signal injection (VSI). This method detects the MTPA trajectory analytically by the injection of a virtual signal into a motor model. It does not use motor parameters and does not inject real signals into the system; therefore, undesired noise and vibrations are excluded. However, despite perfect reported results of VSI methods, we do not share the optimism of the authors. We found that these algorithms were very sensitive to the variation in stator resistance, which is not a problem in other algorithms, including the conventional one.

Another approach used for tracking the MTPA trajectory is seeking algorithms, which do not use motor parameters and can effectively operate in a changing environment. An example of this technique is described in [22], where the authors continuously varied the phases of the stator current

and tracked the minimum of the current magnitude. The main disadvantages of this idea are lower dynamics and the necessity of a position encoder.

After a detailed analysis of the pros and cons of the existing techniques, the authors found that the seeking algorithm reported in [22] is the best candidate for developing a motor drive, provided that it can be adapted to the operation without a position encoder.

2. MTPA Seeking Algorithm

The seeking algorithm reported in [22], which was selected for further improvements, continuously varies the phase of the stator current γ to provide the minimum stator current I_s for the given torque. The flowchart of this method is shown in Figure 1. It can be clearly seen that in each calculation step, the motor phase is modified by a small disturbance angle $\Delta\gamma$, and the resulting value γ is checked to be inside the limits. After that, the new value of the phase of the stator current is applied, and the control system waits until the end of transient. After that, the tuning algorithm measures the average magnitude of the stator current over the calculation step and compares it to the value measured at the previous step.

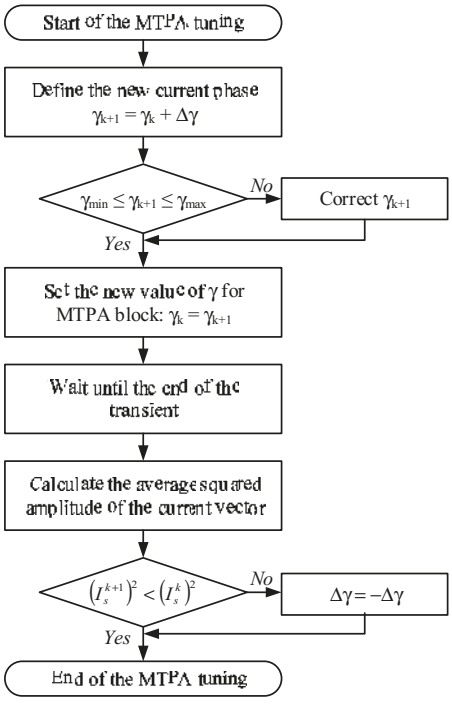

Figure 1. Flowchart of the MTPA seeking algorithm.

If the current value obtained at the current calculation step is less than the same value from the previous step, the stator current has been rotated in the correct direction, and vice versa. If the stator current has been rotated to the incorrect direction, the sign of disturbance value $\Delta\gamma$ is reversed, and in the next step the stator vector will be rotated in the proper direction. This process is illustrated in Figure 2, where the current vector rotates to track the constant torque loci.

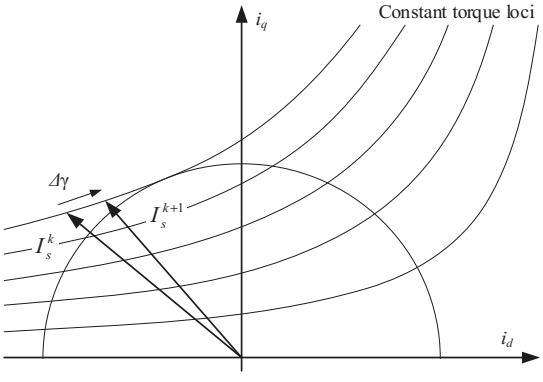

Figure 2. Variation of stator current phase.

This seeking algorithm has the advantages of being insensitive to motor parameter variation and the possibility of being easily implemented in the previously developed control schemes.

At the same time, this technique demonstrates excellent results only when the rotor position is measured precisely, and may fail when a significant error appear. As can be seen from Figure 2, the minimum current for the constant torque curve is not strongly pronounced, and the variation of the stator current angle causes only minor changes to the current magnitude. This problem is illustrated by the data in Table 1, calculated for the test motor, the parameters of which are given in the section below. The table illustrates the increase in the magnitude of the stator current when its angle varies with the step of one degree. As can be seen, the variation in stator current is quite small and lies below one percent for a range of ±5°. Therefore, to detect the minimum stator current, it is very important to know the rotor position precisely. Unfortunately, sensorless drives contain a position error with a typical value of 5°–10°, which varies over revolution and restricts the operation of the seeking algorithm in sensorless systems. The original algorithm [22] at the calculation step k applies the stator current with a phase γ_k. In the next calculation step $k + 1$, the algorithm applies the stator current with a phase γ_{k+1}, which differs from the γ_k at the fixed disturbance angle $\Delta\gamma$. During each calculation step, the algorithm measures (integrates) the magnitude of the stator current and then compares these magnitudes. The lower current magnitude corresponds to the phase angle being closer to the true MTPA angle. Thus, if the position error is not constant, the stator current is applied at different phase angles during each calculation step; therefore, its magnitude varies, producing incorrect measurements of the current. In order to overcome this problem and use the advantages of the seeking technique, an advanced method was proposed, which makes the operation of the seeking algorithm in sensorless drives possible.

Table 1. Increase in Stator Current due to Angle Variation.

Angle	Increase, %	Angle	Increase, %
$\gamma + 1°$	0.02	$\gamma - 1°$	0.02
$\gamma + 2°$	0.09	$\gamma - 2°$	0.10
$\gamma + 3°$	0.19	$\gamma - 3°$	0.22
$\gamma + 4°$	0.33	$\gamma - 4°$	0.39
$\gamma + 5°$	0.56	$\gamma - 5°$	0.62

3. Proposed Enhanced Algorithm

As mentioned earlier, the main problem with the implementation of the seeking algorithms in the sensorless systems is the absence of precision of information on the rotor position. The typical position estimation error of the back-EMF-based estimator is shown in Figure 3. This picture demonstrates

that the estimation error is significant for the seeking technique described. The proposed algorithm belongs to the perturb and observe methods, which involves modifying one parameter of the system and analyzing its response by measuring another parameter. Algorithms such as these may fail if another disturbance appears in the system and impacts the measured parameter. At the same time, our experiments showed that the average value of the position estimation error is stable and mainly depends on the variation in the relationship between the direct and quadrature inductances, while instant error depends on disturbance factors, such as cyclic mechanical load, non-sinusoidal back-emf, etc. Therefore, the previously developed seeking algorithm may operate properly if its calculation step contains an integer number of electrical revolutions. In that case, the average position error at consequent calculation steps will be the same, and the average current magnitudes may be compared. Stator resistance variation due to temperature change affects the average error value, but the seeking algorithm compensates for this error.

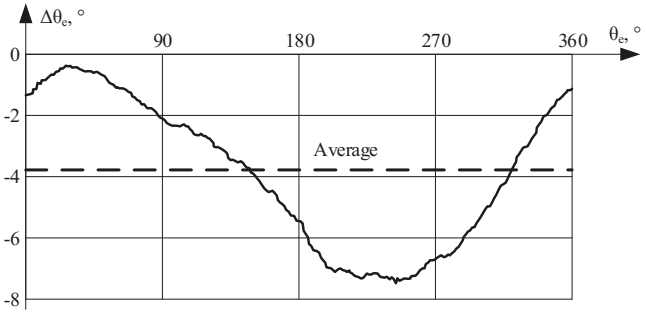

Figure 3. Rotor position estimation error.

The number of electrical revolutions that are contained in one calculation step is denoted as N. Then, the maximum calculation time is denoted as T_{max}. These parameters define the minimum motor speed n_{min}, where the proposed algorithm can operate. If the motor speed n is less than the minimum speed n_{min}, the tuning algorithm must be stopped. Then, the length of the current calculation step T_{cs}^{k} is defined and compared to the length of the previous calculation step T_{cs}^{k-1}. If they are the same, the calculations at these intervals may be compared, otherwise they may not. If the consecutive calculation steps are different, the tuning algorithm calculates the squared amplitude of the stator current for the current measurement interval $\left(I_s^k\right)^2$ and proceeds to the next step. If the length of the previous calculation step and the length of the current calculation step are the same, the tuning algorithm defines the new MTPA angle γ in the same manner as a basic algorithm, measures the squared amplitude of stator current $\left(I_s^k\right)^2$, and compares it to the same value from the previous iteration $\left(I_s^{k-1}\right)^2$. If the squared amplitude of the stator current at the current step is less, it means that the MTPA angle γ was modified in the correct direction, and the same disturbance value will be applied in the next step. If the MTPA angle γ was modified in the wrong direction, then the sign of disturbance value $\Delta\gamma$ in the next step will be reversed. A flowchart of the proposed algorithm is shown in Figure 4.

This algorithm is quite simple, and the most important things are the proper selection of N and T_{max}, which define the errors, the dynamic response of the algorithm, and its minimum operating speed. The higher the number of electrical revolutions in the calculation step, the more reliable and stable the algorithm operates; however, at the same time, its dynamic response decreases. These parameters are suggested to be selected experimentally by monitoring the performance of the tuning algorithm.

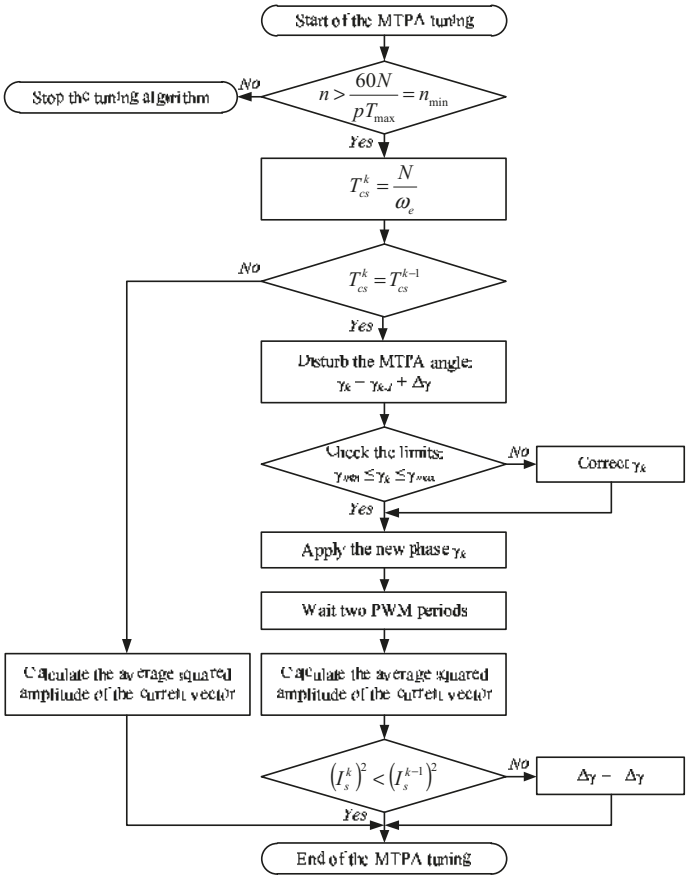

Figure 4. Flowchart of the proposed algorithm.

4. Experimental Setup

The experimental motor used in the experiments is the mass production (MP) device, the parameters of which are given in Table 2. However, these inductances strongly depend on the motor current and vary, as shown in Figure 5.

Table 2. Motor Rated Parameters.

Parameter	Value	Units
Number of poles	2P = 6	-
Rated speed	2000	rpm
Phase resistance	1.5	Ohm
d-axis inductance	54	mH
q-axis inductance	95	mH
Back-EMF constant	0.15	V·s/rad

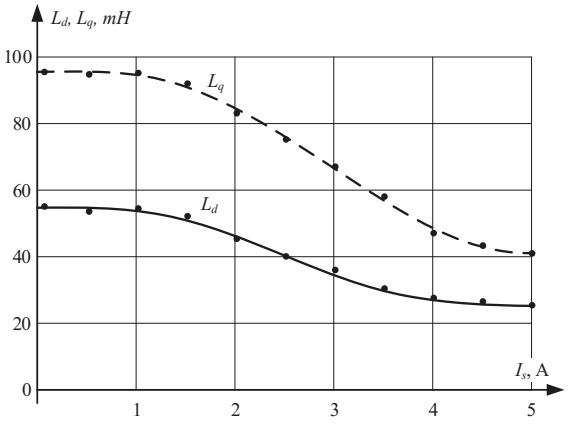

Figure 5. Motor inductances vs. current.

The control system used in the experiment is the same as in MP versions described in [23] (Figure 6). It drives the IPM motor, using the sensorless control, which nowadays can be considered to be a standard for many appliances. This control is based on the back-EMF estimation methods discussed in [24], which is enhanced by the initial position estimation necessary for excluding the reverse rotation while starting. The performance of the implemented estimation algorithm was verified using a quadrature encoder, which proved that the algorithm perfectly operates in the speed range over 10 Hz, with the estimation error being not more than several electrical degrees.

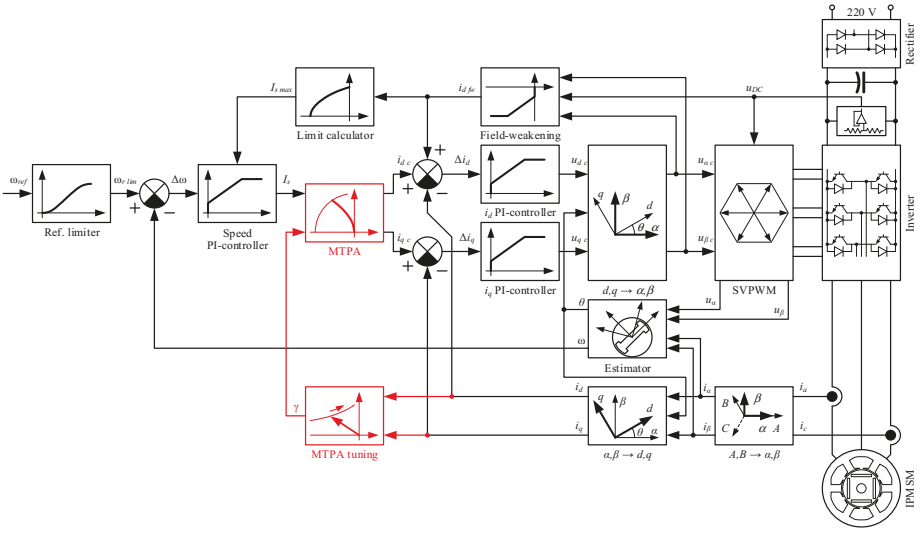

Figure 6. Structure of the sensorless control scheme of the IPM motor drive.

The inverter used for driving the motor is based on the smart power module FSAM10SH60 from "Fairchild" (10 A/600 V), which contains six IGBTs and embedded gate drivers. This drive was developed for a standard 220–240 V, 50/60 Hz supply source. The control system of the drive under test is based on a 60 MIPS Cortex-M3 microcontroller, which operates the inverter at 10 kHz PWM.

This system is equipped with two current sensors and a DC-link voltage sensor, whose signals are processed by a 12-bit ADC of the microcontroller, with a sampling time of 100 µs.

The control system of the experimental drive is a conventional vector control system without the position encoder used in MP devices. It involves an outer speed loop and two inner current loops implemented in the *dq* reference frame, where the electrical position and speed are provided by the estimator. The experimental drive implements open-loop starting and acceleration with immediate closing and the reinitialization of the controllers.

The control system measures two phase currents and DC-link voltage, which are then transformed into phase currents and voltages, respectively. After that, the three phase values, *abc*, are converted into two axis stationary reference frames αβ, using the Clarke transformation:

$$\begin{bmatrix} X_\alpha \\ X_\alpha \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{2}$$

where *X* denotes any converted value. The conversion gain of 2/3 provides equality of amplitudes in *abc* and *αβ* reference frames, which is easier for tuning. Then, the values are transformed into a synchronous *dq* reference frame using the Park transformation:

$$\begin{bmatrix} X_d \\ X_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} X_\alpha \\ X_\alpha \end{bmatrix} \tag{3}$$

where θ represents the angle of angular displacement.

The control system uses a field-weakening controller, which increases the maximum speed by up to +50% of the rated velocity by weakening the field of the rotor with i_d current. The drive under test also includes an MTPA block for increasing efficiency and decreasing stator current. This MTPA block receives the stator current from the speed controller and then converts it into direct and quadrature components.

The only difference between the experimental and the conventional systems is the presence of the MTPA tuning block with the proposed algorithm, which outputs the MTPA angle of the decomposition of the commanded stator current. These changes, including additional block and corresponding connections, are shown in red in Figure 6.

5. Experimental Results

5.1. Experimental Setup and Load Motor

The test jig used in our experiments included a load motor, represented by an HG-SR202, 2 kW AC servomotor from Mitsubishi Electric, which was equipped with an incremental position encoder. This motor was controlled using the MR-J4-200, an AC servo amplifier from Mitsubishi Electric, operated in the torque control mode. The AC servo amplifier and the inverter were connected to the PC, which was used to control the experiment and monitoring the data. This experimental setup is shown in Figure 7.

5.2. Motor Characteristics

At the beginning of our experimental work, the real characteristics of the motor were found. This experiment was performed using the test jig shown in Figure 7, where an incremental position encoder with a resolution of 4096 pulses was used. Motor inductances were found in several points for different values of stator current at the MTPA condition. They are shown in Figure 5, which demonstrates that saturation significantly impacts their values.

The motor MTPA characteristics were detected with a step of 1°, and they are demonstrated in Figure 8. It can be clearly seen that the experimental MTPA curve deviates from the theoretical curve

at higher currents due to the saturation effect. Therefore, this fact must be taken into account when developing an efficient control system.

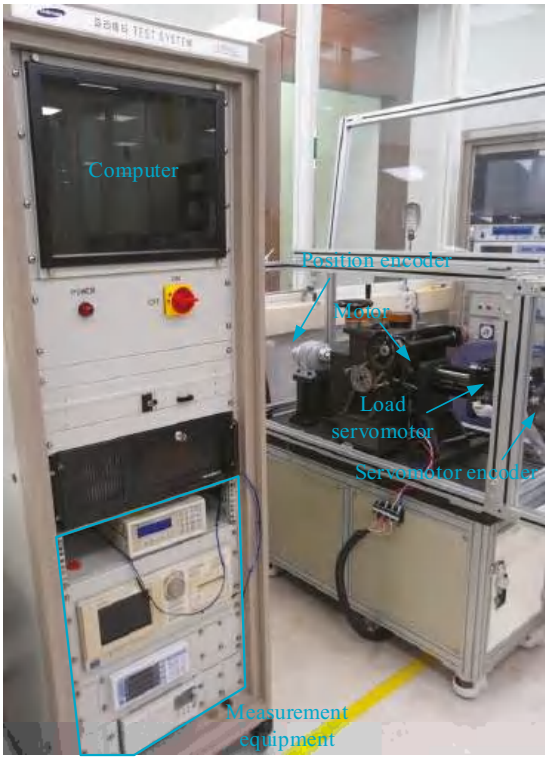

Figure 7. Experimental setup.

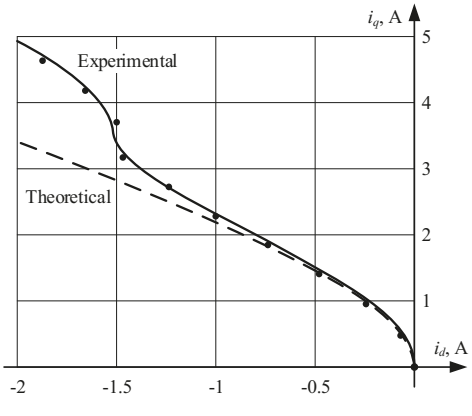

Figure 8. Theoretical and experimental MTPA curves.

5.3. The Performance of the Developed Algorithm

The proposed MTPA tuning algorithm was tested using the test bench described above. The load torque was programmed as a function with several steps, shown in Figure 9 so that the detection of the MTPA angle at different conditions can be dynamically monitored. A step-changing function with the following steps was used: 1, 2, 2.5, 3, 3.5, and 4 Nm. The values of the steps at lower currents are higher because the MTPA angle in this region changes faster, and it is easier to track it. At the same time, at a higher load, the steps are lower to check the behavior of the proposed algorithm in that region in more detail.

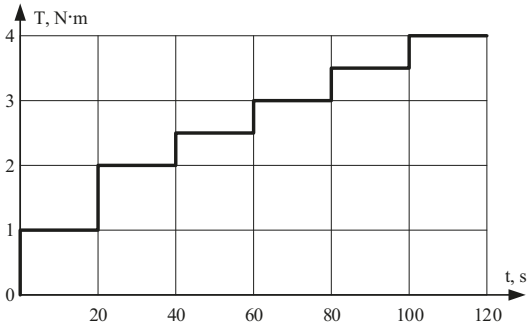

Figure 9. Commanded load torque.

When selecting the parameters of the algorithm, it was assumed that the MP sensorless drives rarely operate at a speed below 900 rpm, as they are focused on the total efficiency more than on a fast dynamic. At the same time, the higher number of electrical revolutions N used as a calculation step provides better stability and avoids side effects. Therefore, the maximum calculation time, as T_{max} = 0.5 s, and minimum operating speed as n = 600 rpm, were selected, which results in N from 15 revolutions or less. After several experiments, the disturbance angle $\Delta\gamma$ equal to 3° was selected, which was a compromise between precision and the algorithm's stability. The lower value of $\Delta\gamma$ makes it difficult to detect the current changes in our system; therefore, 3 degrees is a tradeoff value between the tolerance and quality of control. At the same time, in other systems, especially with motors of higher magnetic asymmetry, the lower values of $\Delta\gamma$ can be used.

The operation of a tuning algorithm at 900 rpm with N = 15 is shown in Figure 10, which demonstrates the proper detection of the MTPA angle. However, the defined value of γ contains some spikes. The results of the same experiment at 1500 rpm are presented in Figure 11, which proves the correct operation of the developed algorithm and demonstrates a lower number of spikes—i.e., it has higher stability. In the next experiment, the calculation step was increased to 30 electrical revolutions, and the results of this test are provided in Figure 12. It is observed that the stability of the proposed algorithm increased, and the defined MTPA angle almost did not contain significant deviations.

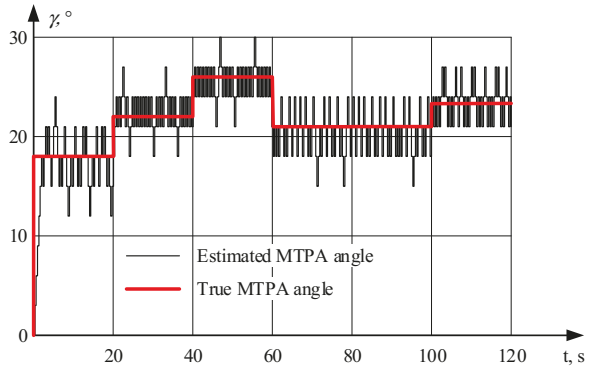

Figure 10. MTPA angle defined at 900 rpm with $N = 15$.

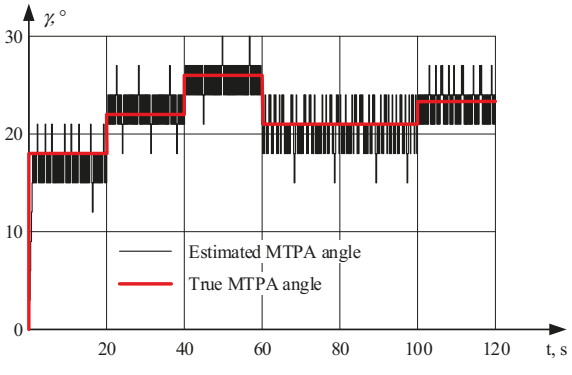

Figure 11. MTPA angle defined at 1500 rpm with $N = 15$.

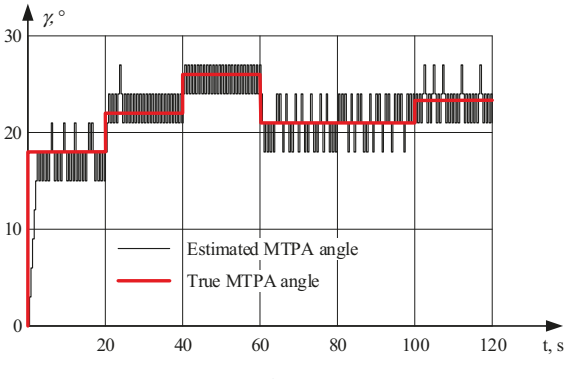

Figure 12. MTPA angle defined at 1500 rpm with $N = 30$.

6. Conclusions

This paper proposes the adaptive MTPA control algorithm capable of operating in sensorless drives. This algorithm does not use any motor parameters and conventional equations; therefore, it is insensitive to the motor parameter variation due to the operating conditions. The proposed method uses a seeking technique, which continuously varies the phase of the stator current and tracks the minimum of its magnitude. It is designed to be used in conventional control systems; therefore, it can

be easily embedded in previously developed motor drives. Experimental results provided in this paper prove the feasibility of the developed algorithm and its perfect operation, despite the motor operating conditions. The proposed algorithm was implemented in the drives with reciprocating compressors and put into mass production.

Author Contributions: General idea, A.D.; Simulation software, A.D. and A.A.; Software implementation and experimental verification, A.D.; Methodology, A.A.; Data analysis, A.D. and A.A.; Writing original draft, A.D.; Writing—review and editing, A.A. Both authors have read and agreed to the published version of the manuscript.

Funding: This research is supported by the Russian Science Foundation grant (Project № 16-19-10618).

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

AC	Alternating Current
ADC	Analog to Digital Converter
DC	Direct Current
EMF	Electromotive Force
IGBT	Insulated-Gate Bipolar Transistor
IPMSM	Interior Permanent Magnet Synchronous Motor
MCU	Microcontroller Unit
MIPS	Million Instructions Per Second
MP	Mass Production
MTPA	Maximum Torque Per Ampere
PC	Personal Computer
PM	Permanent Magnet
PMSM	Permanent Magnet Synchronous Machine
PWM	Pulse-Width Modulation
RLS	Recursive Least Squares

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Fault Diagnosis of PMSG Stator Inter-Turn Fault Using Extended Kalman Filter and Unscented Kalman Filter

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Received: 28 April 2020; Accepted: 4 June 2020; Published: 9 June 2020

Abstract: Since the permeant magnet synchronous generator (PMSG) has many applications in particular safety-critical applications, enhancing PMSG availability has become essential. An effective tool for enhancing PMSG availability and reliability is continuous monitoring and diagnosis of the machine. Therefore, designing a robust fault diagnosis (FD) and fault tolerant system (FTS) of PMSG is essential for such applications. This paper describes an FD method that monitors online stator winding partial inter-turn faults in PMSGs. The fault appears in the direct and quadrature (dq)-frame equations of the machine. The extended Kalman filter (EKF) and unscented Kalman filter (UKF) were used to detect the percentage and the place of the fault. The proposed techniques have been simulated for different fault scenarios using Matlab®/Simulink®. The results of the EKF estimation responses simulation were validated with the practical implementation results of tests that were performed with a prototype PMSG used in the Arab Academy For Science and Technology (AAST) machine lab. The results showed impressive responses with different operating conditions when exposed to different fault states to prevent the development of complete failure.

Keywords: extended Kalman filter (EKF); permanent magnet synchronous generator (PMSG); fault diagnosis (FD); stator inter-turn short circuit

1. Introduction

In the last decade, the permeant magnet synchronous generator (PMSG) has been used in many industries, especially, for renewable energy applications [1–3], aircraft [4,5], and propulsion systems [6]. Consequently, this has generated growing concern about the operation reliability of the PMSG, especially in safety critical applications like the shaft generators (SG) in marine applications.

The PMSG faults inexorably decrease the reliability of the system, which may lead to malfunction or a failure in the system. Moreover, most PMSG applications are safety-critical, which makes the presence of fault an unwanted option. Mechanical, magnetic, and electrical faults are the major types of faults that may occur in a PMSG [7]. Extensive research has examined the detection of mechanical faults, which is the most usual fault in the PMSG; these faults can be divided into eccentricity faults [8–10], and bearing faults [11–14], based on [15], the bearing faults represent from 40 to 50% of the total faults while the eccentricity fault represents from 5 to 10% in the machines. Further research has considered the detection of demagnetization faults [16–18]. Both types of faults cause torque to unbalance; followed by an increase in the overall temperature of the machine. The high temperature may cause the deterioration of the stator winding insulation, which may lead to the presence of a stator

inter-turn fault [19–22], based on [21], the stator electrical faults represent 38% of the total faults in the machines. All these papers have focused on the stator winding inter-turn fault in any phase, which is a particular case fault that, if not addressed, affects the machine's voltage magnitude and balance, and may lead to other catastrophic failures.

Fault diagnosis (FD) techniques were used to detect the place and severity of the fault, followed by isolation with minimal losses. This can be divided into three main approaches: signal-based, artificial intelligence-based, and model-based techniques [7,23]. First are the signal-based techniques; they emphasize the analysis of the measured signal to detect the presence of specific frequency components relating to the fault. Moreover, it requires knowledge of the fault signatures, this knowledge can be acquired from the stator voltage and current, torque signal, and similar variables [7]. The advantages of these methods are the non-dependency on a specific model [24]. However, if the signal contains many harmonics, it may give an erratic estimation for fault. Furthermore, it needs a batch set of samples to analyze the signal; this causes a delay in time in determining a fault estimation. Wavelet transform (WT) is one of these methods that is presented in [25] and [26]. Additionally, Hilbert Hang transform (HHT) and Wigner–Ville have been shown to produce considerable results [17,27]. Also, the vibroacoustic techniques are used in condition monitoring for the machines in [28] and [29].

Secondly, artificial intelligence (AI) methods have been extensively studied in the fault diagnosis of electrical machines. These techniques require a deep understanding of fault signatures under several faulty conditions. However, it needs a set of logged data for the definite fault, which may be undetermined. In addition, some of these techniques do not cope with the online monitoring required for inter-turn short circuit detection due to the computational burden taking time for these techniques to fulfill the FD. Neural networks (NN) [30,31], particle swarm optimization [32], and fuzzy logic [33,34] are AI methods that have been used in stator windings FD of PMSG. A lot of researchers have used a combination of them, such as using the neuro-fuzzy technique [35] or using the AI technique with the signal base technique, such as using the wavelet transform (WT) with the adaptive neuro-fuzzy inference system (ANFIS) in [25].

The third choice is model-based FD techniques, which require the use of a system model. These techniques give the precise estimation of the fault if the mathematical model used is accurate, so they can estimate parameters that are hard to measure [36,37]. Moreover, these techniques offer online parameter identification with the required fast response for taking action. However, these techniques require an accurate model for the system to make a robust estimation in all operating conditions, which is so rare to find, this means that the model-based technique is not used in a lot of complex systems. In [38], the recursive least square (RLS) method is used to estimate the stator inter-turn faults, and the technique provides good response and early detection for the fault. The extended Kalman filter (EKF) has been used in [20,39–41], for the detection of the fault in PMSG and the induction motor (IM). Other researches take into account the use of unscented Kalman filter (UKF) in parameters estimation of PMSG, as an enhancement tool for the control system [42]. The model-based technique is also used in the industrial process control fault diagnoses in [37,43]. In [44], the research presented uses the graph of the process to find an accurate model for the system.

In this contribution, a comparison between the use of the EKF and the UKF is presented in the fault diagnosis of the stator inter-turn faults for PMSG, which has not been addressed before in any other research work. The mathematical model and the equivalent circuit in both healthy and faulty states were implemented based on the model in [21,40]. The procedures of fault percentage and location estimation using EKF and UKF are presented, and the simulation results of parameter estimation in both healthy and faulty conditions, showing the response of both techniques in the case of inter-turn short circuits through several operating conditions and scenarios, are discussed. Moreover, two scenarios were proposed for the decision-making process based on the severity of the fault. The results were validated by applying a practical emulation for the fault in a laboratory prototype machine and discussed.

2. The Faulty PMSG Model

The model was implemented in the direct and quadrature (dq-frame) in [39], in both states, healthy and faulty.

2.1. PMSG Healthy State Model

The healthy state represents the machine in the case of no fault; in this case, the internal current outgoing from the machine is the same current consumed from the load. Figure 1 shows the equivalent circuit of the machine in the abc-frame, R_s and L_s are the stator resistance and inductance. E_a,E_b,E_c, are the induced voltages, and the output current from the generator is represented by I_a, I_b,I_c.

To simplify the model, the equations of the machine should be converted to the dq-frame. Figure 2 shows the equivalent circuit of the machine in the dq-frame. L_d and L_q are the direct and quadrature inductance, I'_{sd} and I'_{sq} is the internal direct and quadrature current of the generator respectively, I_{sd} and I_{sq} are the terminal direct and quadrature current of the generator respectively, the V_{sd} and V_{sq} are the direct and quadrature stator terminal voltages, and ω_e is the electrical angular speed that can be related to rotor mechanical angular speed ω_m. All the equations representing the machine on the dq-frame are given in [39].

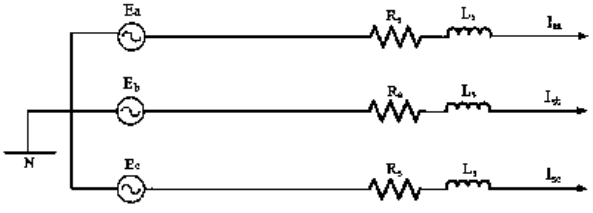

Figure 1. The equivalent circuit of healthy permeant magnet synchronous generator (PMSG) in the abc-frame.

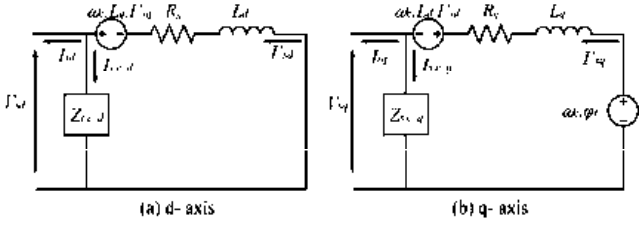

Figure 2. The equivalent circuit of healthy PMSG in the dq-frame.

2.2. PMSG Faulty State Model

In the case of a PMSG stator winding fault, the number of turns in a certain phase is reduced due to the deterioration in the stator winding insulation, which causes a short circuit in this phase. Most stator winding insulation failures are caused by high temperatures and overloading. When a stator winding short circuit happens, the value of generator impedance changes, consequently the amplitude of stator current harmonics will increase, the torque will drag, and potential overheating will appear, and so on, this symptom may lead to complete failure if the fault was not addressed.

The short circuit current $[I_{s/c}]_{\mathrm{dq}}$ is generated inside the machine as shown in Figure 3 due to the presence of the short circuit impedance $Z_{s/c}$ in any phase; this impedance value changes according to the ratio between the number of inter-turn short-circuit windings and the total number of turns in one healthy phase. Figure 4 shows the equivalent circuit of the faulty machine in the dq-frame. The mathematical equations representing the faulty state model of the PMSG in dq-frame are given in [39].

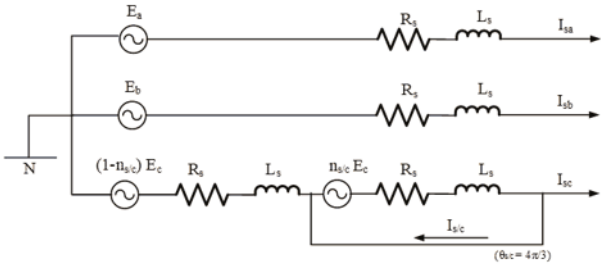

Figure 3. The short circuit turns ratio representation.

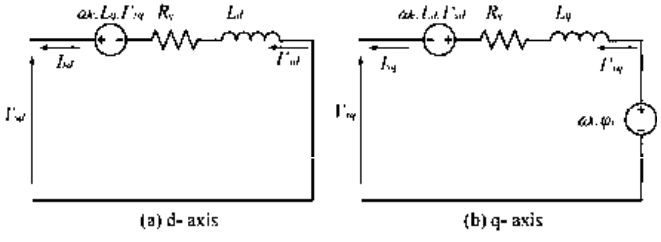

Figure 4. The equivalent circuit of the faulty state PMSG in the dq-frame.

3. Parameter Estimation Procedures

The general faulty PMSG state-space model and EKF algorithm are presented in this section.

3.1. General PMSG State-Space Model

To use the EKF and UKF techniques to estimate the presence of the fault, the precise state-space model of the machine should be highlighted. Based on [39], the state-space model equation of the faulty machine can be written as:

$$\begin{cases} \dot{x}_m(t) = A_m \cdot x_m(t) + B_m \cdot u_m(t) + W_m(t) \\ y_m(t) = C_m \cdot x_m(t) + D_m \cdot u_m(t) + V_m(t) \end{cases} \quad (1)$$

where:

$$x_m(t) = \begin{bmatrix} I'_{sd} & I'_{sq} \end{bmatrix}^T \; u_m(t) = \begin{bmatrix} V_{sd} & V_{sq} & \varphi_f \end{bmatrix}^T A_m = \begin{bmatrix} -\frac{R_s}{L_d} & \omega_e \cdot \frac{L_q}{L_d} \\ -\omega_e \cdot \frac{L_d}{L_q} & -\frac{R_s}{L_q} \end{bmatrix}$$

$$B_m = \begin{bmatrix} -\frac{1}{L_d} & 0 & 0 \\ 0 & -\frac{1}{L_q} & \frac{\omega_e}{L_q} \end{bmatrix} \quad C_m = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

$$D_m = \begin{bmatrix} D_1 & 0 \end{bmatrix}^T \; D_1 = -\sum_{k=1}^{3} \frac{2 \cdot n_{s/c\,k}}{(3 - 2 \cdot n_{s/c\,k}) \cdot R_s} \cdot P(\theta)^T \cdot Q(\theta_{s/c\;k}) \cdot P(\theta)$$

where

$$P(\theta) = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \quad (2)$$

$$Q(\theta_{S/C}) = \begin{bmatrix} cos^2\theta_{S/C} & sin\theta_{S/C} \cdot cos\theta_{S/C} \\ sin\theta_{S/C} \cdot cos\theta_{S/C} & sin^2\theta_{S/C} \end{bmatrix} \quad (3)$$

The extension of the model states to estimate the presence of a fault in any phase is compulsory for the estimation process of EKF and UKF, the new states of the model become as follows:

$$\widetilde{X}_e(t) = \begin{bmatrix} X(t) \\ \lambda(t) \end{bmatrix} = \begin{bmatrix} I'_{sd} & I'_{sq} & n_{A\,s/c} & n_{B\,s/c} & n_{C\,s/c} \end{bmatrix}^T \tag{4}$$

where $\widetilde{X}_e(t)$ is the estimated state; After that, the model equations are linearized around a definite operating point followed by discretization at a sampling time *Ts*, the model expressed as:

$$\begin{bmatrix} \dot{I}'_{sd} \\ \dot{I}'_{sq} \\ \dot{n}_{A\,s/c} \\ \dot{n}_{B\,s/c} \\ \dot{n}_{C\,s/c} \end{bmatrix} = \begin{bmatrix} 1 - T_s\frac{R_s}{L_d} & T_s{\cdot}w_e{\cdot}\frac{L_q}{L_d} & 0 & 0 & 0 \\ -T_s{\cdot}w_e{\cdot}\frac{L_d}{L_q} & 1 - T_s\frac{R_s}{L_q} & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I'_{sd} \\ I'_{sq} \\ n_{A\,s/c} \\ n_{B\,s/c} \\ n_{C\,s/c} \end{bmatrix} + \begin{bmatrix} -\frac{T_s}{L_d} & 0 & 0 \\ 0 & -\frac{T_s}{L_q} & \frac{\omega_e}{L_q} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{sd} \\ V_{sq} \\ \varphi_f \end{bmatrix} \tag{5}$$

3.2. Extended Kalman Filter Algorithm

The EKF gives an approximation of the optimal estimate. The non-linearity of the system's dynamics is approximated by a linearized version of the non-linear system model around the last state estimate. As in many cases, if the nonlinear system is approximately linearized, the EKF may not perform well [20]. If there is a bad initial guess regarding the underlying system's state, then this may cause a bad estimation. The first step in the EKF algorithm is the prediction step equations, which consist of state prediction and error covariance matrix update, and the second step is the correction step which corrects the predicted state estimate and it's covariance matrix as in Figure 5. Consider applying EKF to estimate the parameter λ_k in the PMSG system, the discrete linearized state-space model of PMSG is expressed as:

$$\begin{cases} \widetilde{X}_{e_{k+1}} = \widetilde{F}_k\,\widetilde{X}_{e_k} + W_k \\ \widetilde{Y}_k = \widetilde{H}_k\,\widetilde{X}_{e_k} + V_k \end{cases} \tag{6}$$

where

$$\begin{cases} \widetilde{F}_K = \begin{bmatrix} 1 + T_s A(\lambda_k) & T_s\left(\frac{\partial A(\lambda_k}{\partial \lambda_k} X_k + \frac{\partial B(\lambda_k}{\partial \lambda_k} U_k\right) \\ 0 & I \end{bmatrix} \\ \widetilde{H}_K = \left[C(\lambda_k)\ \left(\frac{\partial C(\lambda_k}{\partial \lambda_k} X_k + \frac{\partial D(\lambda_k}{\partial \lambda_k} U_k\right)\right] \end{cases} \tag{7}$$

$\widetilde{F}_K$ and $\widetilde{H}_K$ represent the state and output equations of the discrete linearized model. By substituting matrix A and B in (4) into (6), $\widetilde{F}_K$ and $\widetilde{H}_K$ in case of, $n_{A\,s/c}$, $n_{B\,s/c}$, $n_{C\,s/c}$, as an estimated parameter will be:

$$\widetilde{F}_K = \begin{bmatrix} 1 - T_s\frac{R_s}{L_d} & T_s{\cdot}\omega_e{\cdot}\frac{L_q}{L_d} & 0 & 0 & 0 \\ -T_s{\cdot}\omega_e{\cdot}\frac{L_d}{L_q} & 1 - T_s\frac{R_s}{L_d} & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \widetilde{H}_K = \begin{bmatrix} 1 & 0 & S_A \times q_1 & S_B \times q_1 & S_C \times q_1 \\ 0 & 1 & S_A \times q_2 & S_B \times q_2 & S_C \times q_2 \end{bmatrix} \tag{8}$$

where

$$S_A = -6/\left((3 - 2n_{A\,s/c})^2 \times R_s\right)\ S_B = -6/\left((3 - 2n_{B\,s/c})^2 \times R_s\right)$$

$$S_C = -6/\left((3 - 2n_{C\,s/c})^2 \times R_s\right)\ \begin{bmatrix} q_1 \\ q_2 \end{bmatrix} = \left[P(\theta)^T{\cdot}Q\left(\theta_{\frac{s}{c}\,k}\right){\cdot}P(\theta)\right]_{2x2}{\cdot}\begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix}$$

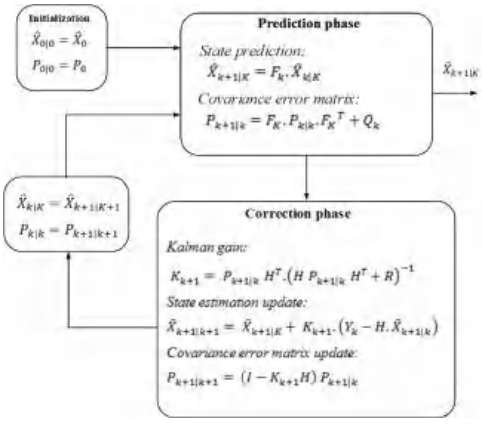

Figure 5. Extended Kalman filter (EKF) algorithm equations.

3.3. Unscented Kalman Filter Algorithm

Instead of using linearized equations using the Jacobin matrix to approximate the nonlinear model as the EKF approach, the UKF generates a finite set of sigma points to compute the predicted states and measurements and the associated covariance matrices [45]. Mathematically, the UKF process can be described as in Figure 6.

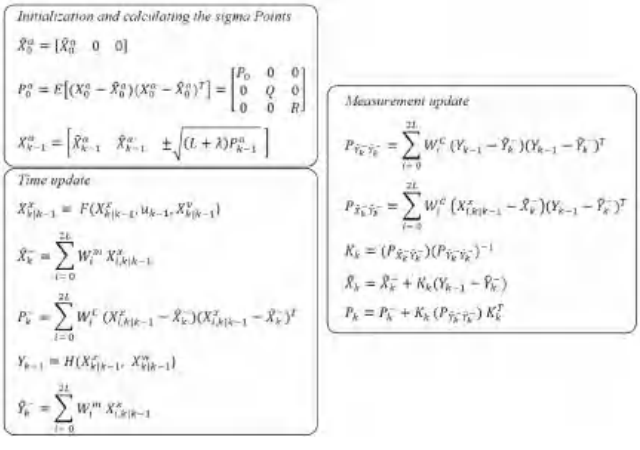

Figure 6. Unscented Kalman filter (UKF) algorithm equations.

Where W_i^m and W_i^c are weighting factors and they are equal to.

$$W_i^m = W_i^C = 1/2(L+\lambda) \tag{9}$$

where L is the state dimension and $\lambda = \alpha^2((L+k)-L)$, α can be tuned from 10^{-4} to 1 and k usually was chosen to be 0.

Figure 7 shows the block diagram of the fault diagnosis online monitoring for the PMSG.

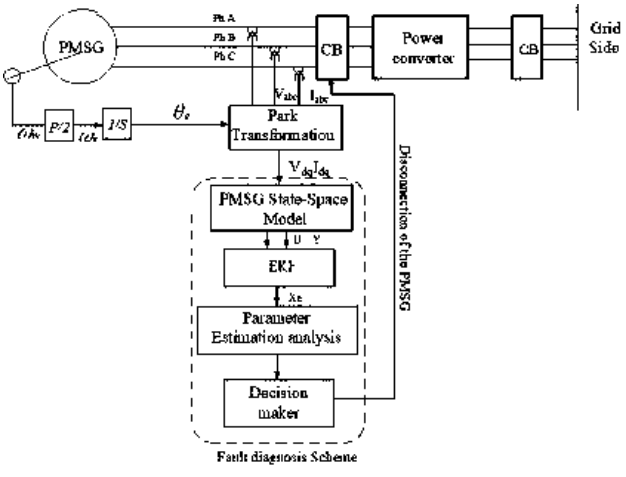

Figure 7. PMSG fault diagnosis on-line monitoring block diagram.

3.4. The Covariance Matrices Tuning

The noises covariance matrices are diagonals, Q can be divided into two matrices: q_x (for measured states) and q_λ (for the estimated parameters). Thus, Q and R can be expressed as:

$$\begin{cases} Q = q_x \cdot \begin{bmatrix} I_m & 0 \\ 0 & \frac{q_\lambda}{q_x} \cdot I_n \end{bmatrix} \\ R = r \cdot I_m \end{cases} \tag{10}$$

where m is the state's x numbers and n is estimated parameters λ numbers, q_x and r could be determined by measuring the variance of noises on input σ_u^2 and output signals σ_y^2 [20], they are expressed as Equation (9) and the ratio q_λ / q_x is set by the evolution time constant of the estimated parameters (τ) as expressed in Equation (10).

$$\begin{cases} q_x = \left(\frac{\partial f_k}{\partial u_k}\right)^2 \cdot \sigma_u^2 \\ r = \left(\frac{\partial H_k}{\partial X_k}\right)^2 \cdot \sigma_y^2 \end{cases} \tag{11}$$

$$\sqrt{\frac{q_\lambda}{q_x}} \approx \frac{T_s}{\tau \cdot \sqrt{\sum_{i=1}^{n} \left(\left|\frac{\partial f_{k_i}}{\partial u_k}\right| \cdot \left|\frac{\partial h_{k_i}}{\partial X_k}\right|\right)^2}} \tag{12}$$

4. Simulation Results

The machine parameters were taken from the nameplate of the generator, as shown in Table 1, the equations of the generator were used to simulate the output of the machine with different operating points, and the simulation run at sampling time $T_s = 100$ us.

Table 1. The PMSG parameters used.

Parameter	Symbol	Value
Nominal Power	P	1500 W
Nominal current	I_s	5 A
Nominal Voltage	V_s	100 v
Nominal Frequency	f	50 Hz
Stator resistance	R_s	1.2 Ω
Direct *axis* magnetizing inductance	L_d	4 mH
Quadrature *axis* magnetizing inductance	L_q	3 mH
Nominal Torque	T_m	9.7 Nm
Rotation speed	N_m	1500 rpm
Number of pole pairs	p	2
Total moment of system inertia	J	0.11 kgm^2

4.1. EKF VS. UKF Response

Figure 8 shows the instantaneous internal current of phase A of the machine at RMS load current of 0.75 A and frequency of 30 Hz; a simulated inter-turn fault was implemented at t = 0.5 s, this fault caused an increase in the current inside the machine, respectively, the voltage in the faulty phase decreased by a small amount and the machine started to become hotter. The current reached an RMS value of 1.63 in the case of $n_{A\,s/c}$ = 4%, which is more than double the used load current. Also, the current reached an RMS value of 4.6 A in the case of $n_{A\,s/c}$ = 16%, which is more than 6 times the load current (0.75 A). This implies the importance of taking fast action to save the machine from damage.

Figure 9 shows the estimation response of EKF and UKF in either a healthy or faulty state; it was noticed that the UKF technique gives more precise values for the fault estimation than the EKF. As the PMSG model used is a linearized and discretized model around a specified operating point in the case of EKF, the error in the estimation varies non-linearly with the value of the short circuit turns ratio. Besides, the covariance matrices (Q and R) were chosen, which play an important role in the quality of the estimation. Also, the presence of sensor errors and the use of a phased locked loop (PLL) in the estimation of the angular position θ cause error in the estimated parameters. Figure 10 shows the error-index, which indicates the values of the inter-turn short circuit that the EKF and UKF techniques will estimate varies the percentage of error. It was noticed that the UKF had much less error than the EKF, especially for short circuit turns ratios greater than 20%, the highest error detected in case of using UKF was at $n_{A\,s/c}$ = 4% and reached 0.3%, however, the EKF estimation error reach 23.72% at $n_{A\,s/c}$ = 100%, the lowest estimation error detected by EKF was at $n_{\,s/c}$ = 16%.

The dynamic time response of detecting the fault was 0.02 s, which is very fast (approximately equal to 1.5 periodic cycles related to the used frequency). The covariance matrix Q, in this case, was tuned by time constant τ = 5 ms, which increased the dynamic response; however, it increased the presence of noise in the estimation action. Figure 11 illustrates the effect of τ on the estimation time, and it was noticed that when the τ = 10 ms, the estimation response reached a steady-state after 0.02 s with the presence of noise, however, when the τ = 80 ms, the estimation response reached a steady-state after 0.2 s but with filtering action. Figure 12 shows the dynamic estimation responses versus the parameter estimation evolution time constant (τ); the detection time increased linearly with the increase of the τ value.

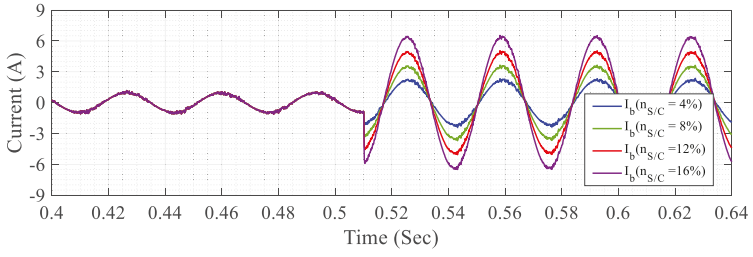

Figure 8. The instantaneous currents of phase A in case of inter-turn fault at 0.72 A load and 30 Hz frequency.

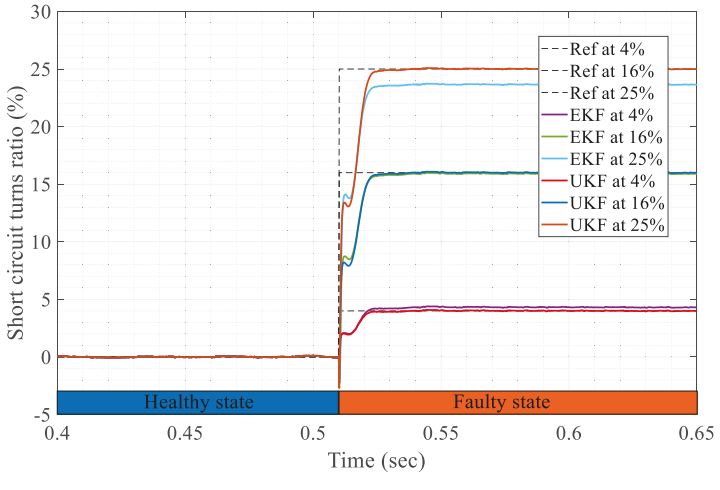

Figure 9. EKF estimation response in phase A at a load of 0.72 A and a frequency of 30 Hz.

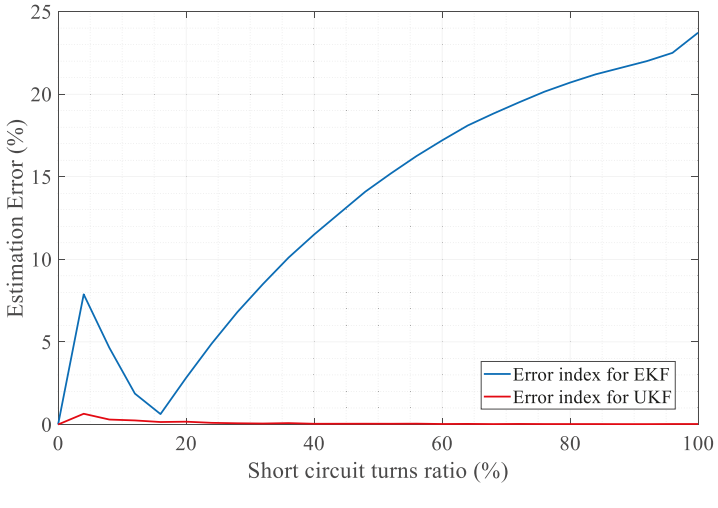

Figure 10. Error Index of the estimated parameter $n_{s/c}$.

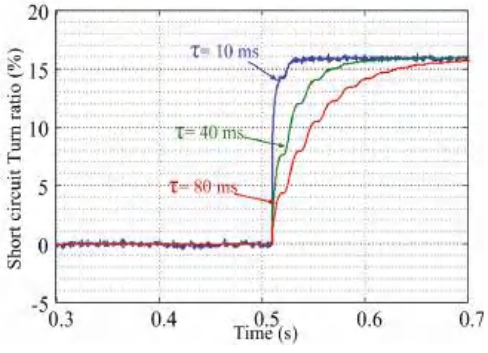

Figure 11. Estimation of 16% short circuit turn ratio in phase B in case of different τ.

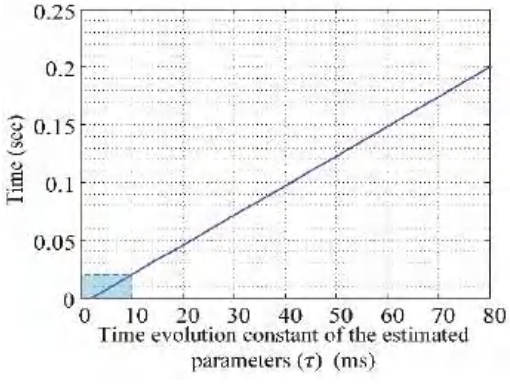

Figure 12. Index of the estimated parameters $n_{s/c}$.

4.2. Robustness Tests

The technique was tested in different operating conditions and showed a robust response; the same tests are done in cases of practical implementation, and are listed as the following:

Test 1: Variation of load current variation from 0.75 A to 3 A by 0.75 A step at a constant frequency of 30 Hz.

Test 2: Variation of frequency from 20 Hz to 50 Hz, with a 10 Hz step.

4.3. Load Variation Test

Figure 13 shows the estimated internal instantaneous currents in the presence of a 16% stator inter-turn short circuit in phase A in case of load variation from 0.75 to 3 A with a rate of 1 Hz. In the case of a 16% stator inter-turn fault, the current reached an RMS value of 5.3 A when I_{Load} = 1.5 A, and it reached an RMS value of 6 A when the I_{Load} = 2.25 A. This confirms the increase of fault severity as load current increases; this form of the fault requires fast action.

Figures 14 and 15 show the estimation response of EKF and UKF in load current variation from I_{Load} = 0.75 A to 3 A condition in the presence of 4%, 8%, 12%, and 16% stator inter-turn short circuit by a rate of 1 Hz. The time constant of the estimated parameters (τ) was chosen to be 10 ms based on the measured value of the input signal noises variance ($ó_x$). The estimation for both techniques show a constant response with the load variation with different short circuit values.

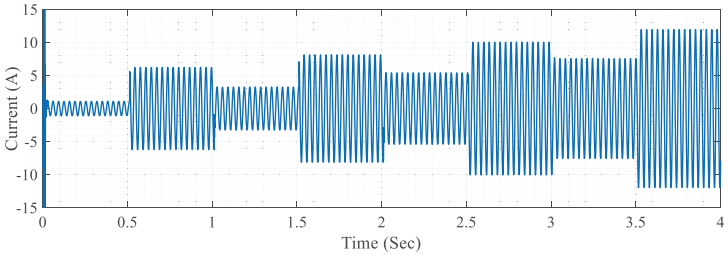

Figure 13. The instantaneous currents of phase A in case of fault at constant frequency of 30 Hz and current variation from 0.75 A to 3 A with step of 0.75 A.

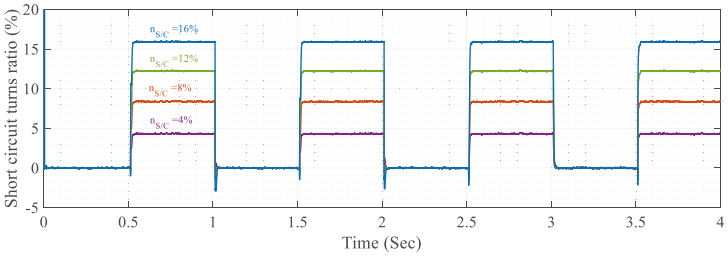

Figure 14. Estimation response in phase A at a frequency of 50 Hz with load variation from 0.75 to 3 A and 7.5 A step.

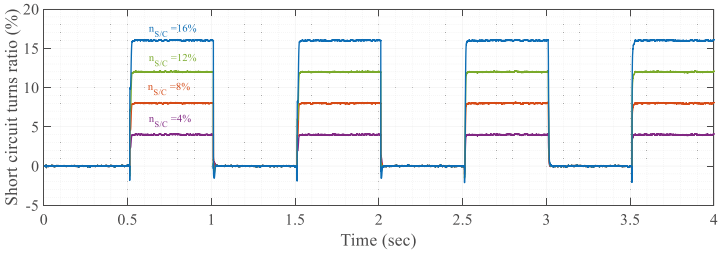

Figure 15. Estimation response in phase A at a frequency of 50 Hz with load variation from 0.75 to 3 A and 7.5 A step.

4.4. Frequency Variation Test

Figure 16 shows the estimated internal instantaneous currents in the case of faults in various frequencies, ranging from 20 Hz to 50 Hz with 10Hz step frequency and rate of change of 1 Hz. Figures 17 and 18 show the EKF the UKF estimation response in the presence of 4%, 8%, 12%, and 16% stator inter-turn short circuit in phase A at constant I_{Load} = 0.75 A and frequencies of 20 Hz, 30 Hz, 40 Hz and 50 Hz. The results show a constant response for both techniques with the frequency variation condition.

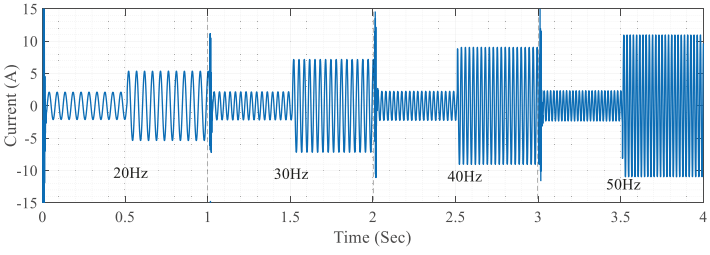

Figure 16. The instantaneous currents of phase A in case of fault at 0.75 A load and 50 Hz frequency.

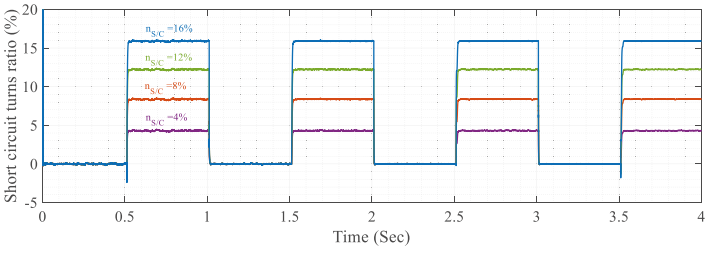

Figure 17. Estimation response in phase A at a load of 0.75 A with frequency variation from 20 to 50 Hz and 10 Hz step.

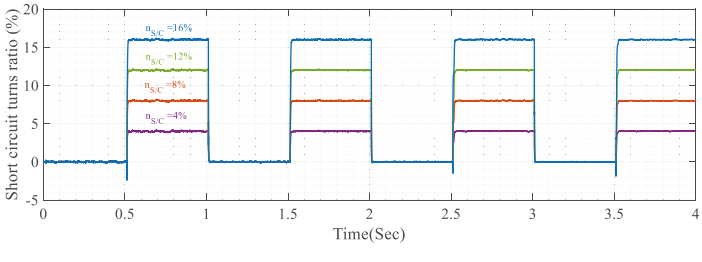

Figure 18. Estimation response in phase A at a load of 0.75 A with frequency variation from 20 to 50 Hz and 10 Hz step.

5. Experimental Results

5.1. Test Bench

For safety conditions, to prevent the used PMSG from being damaged, it is not possible to make an actual stator inter-turn fault. However, it is possible to validate this detection method by adding a shunt resistance $R_{S/C}$ between the needed phase and the neutral, to increase the current in this phase and make the machine unbalanced by a percentage equal to that of an inter-turn fault.

The generator used rotates by means of a separately excited DC motor as a prime mover; the shaft of the motor is coupled directly to the shaft of the PMSG. The power pack supplies the DC motor field with a constant DC supply, and the armature is supplied with a variable DC supply to control the speed of the generator. The load used is a three-phase variable load with a maximum RMS value of 5 A; the shunt resistance $R_{S/C}$ is variable resistance, which will be added to any phase of the three phases using a circuit breaker. Figure 19 shows all the power components of the test bench.

The three-phase voltages were measured by three voltage transformers. The transformers used were typical 220 v/12 v single-phase transformers. Hence, the voltages measured were connected to

analog signal conditioning boards to manipulate the voltage to be level with the digital signal processor (DSP) voltage (from 0 to 3.3 v).

On the other hand, the currents were measured using three CTs at a ratio of 10000:5. The current signals measured were connected to the signal conditioning circuit board to convert the current into a manipulated voltage which was compatible with a DSP analog to digital (A/D) input. The DSP used (Texas Instrument TMS320F280) had all measured signals connected to the A/D port in the DSP. The EKF algorithm was implemented online with a sampling period of T_s = 200 µs. The relay board was used to take the action of disconnection of the faulty phase to prevent fault propagation leading to severe failure. Figure 20 shows the connection diagram for the whole circuit.

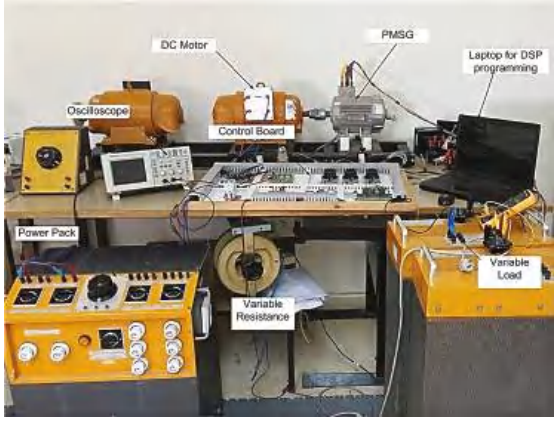

Figure 19. Test bench.

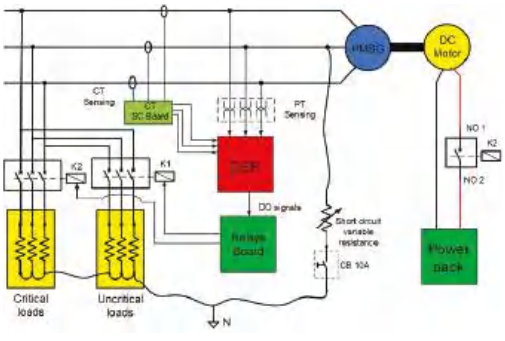

Figure 20. Connection diagram.

5.2. PMSG Test Output

The next step was to compare the measured output voltages and currents of the PMSG used in a simulation of a healthy state. The value of the measured currents and voltages was found to be approximately the same as that in simulation, but with more measurement noise around a mean of 0.4; this will affect the dynamic response of EKF estimation in case of a fault. The output was measured in different load and frequency operating conditions and showed the same output as the simulation. Figure 21a,b show the instantaneous three-phase currents and voltages in the case of a healthy state of PMSG with a load current 0.72 A and frequency of 30 Hz.

Figure 22 shows the difference between the three-phase instantaneous currents and voltages in simulation and practical implementations. It can be seen that the experimental results appear noisier

than that of the simulation. Accordingly, the parameter estimation responses will require more filtering action, which will cause a delay in the dynamic response.

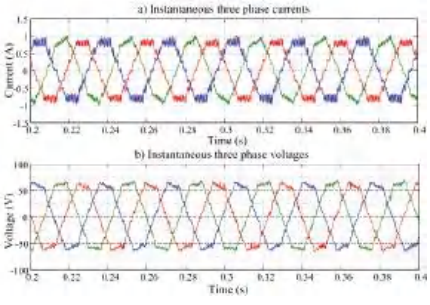

Figure 21. Instantaneous 3phase currents and voltages.

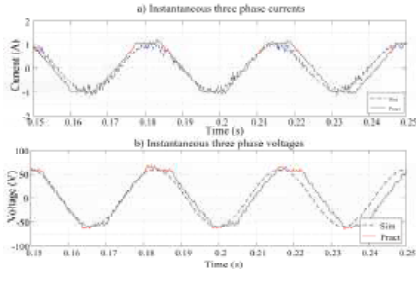

Figure 22. Simulation vs. Practical implementation 3phase currents and voltages.

5.3. EKF Response

The model of a faulty machine and the EKF model were implemented in the DSP, the input to the machine state-space model are the measured stator voltages in the dq-frame. The short circuit current was calculated from the measured dq stator load currents and is presented in the model as the feed-forward matrix D_m. Therefore, the measured three-phase voltages and currents must be converted in dq-frame to make the EKF estimator work probably.

Indeed, the detection of electrical angular position θ is essential to use it in the abc to dq0 transformation. There are two suitable solutions for the detection of electrical angular position θ; the first is to use an encoder sensor coupled directly to the machine shaft and uses its counts to calculate the mechanical angular position, and then calculates the electrical angular position. Nevertheless, this solution requires the addition of new hardware to the system. The second solution is to generate the electrical angular position θ from voltage signals through the three phases of the phased locked loop (PLL), this solution is more economical as extra sensing devices are not needed. Nevertheless, the angular position generated will be dependent on the nature of the measured voltage.

The machine works at a load current of 0.72 and a frequency of 30 Hz in a healthy state. The practical experiments tested the EKF estimation responses in different values of short circuit inter-turn to turn the ratio in all phases ($n_{A\,s/c}$, $n_{B\,s/c}$ & $n_{C\,s/c}$) and in different operating points. The Q and R were tuned at τ = 20 ms to achieve the required fast response with a good filtering action.

Figure 23 display the response of EKF to estimate $n_{A\,s/c}$ = 4% using these conditions. The parameter estimation showed an excellent response to this case when compared to the results of the simulation. Figure 24 display the estimated internal instantaneous currents in the presence of 4%, stator inter-turn short circuit in phase A at t = 0.5 s, respectively. The same response was noticed on the estimation of $n_{A\,s/c}$ = 8% in Figure 25 followed by the estimated internal instantaneous

currents in phase A in Figure 26, respectively. Also, The same response was noticed on the estimation of $n_{A\ s/c} = 12\%$ in Figure 27 followed by the estimated internal instantaneous currents in phase A in Figure 28, respectively. In addition, the estimation of the fault in $n_{A\ s/c} = 16\%$ casein Figure 29 and it's etimated internal current in Figure 30. It was noted that the current reached higher values when compared to the rated current of 0.72 A.

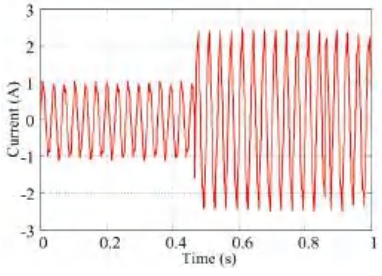

Figure 23. Current in phase A at $n_{A\ s/c} = 4\%$.

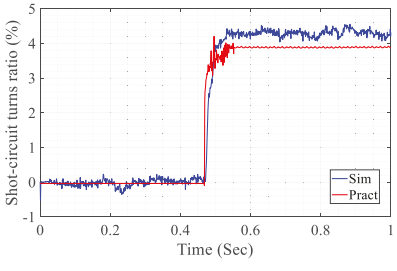

Figure 24. Estimation of 4% short circuit turns ratio in phase A.

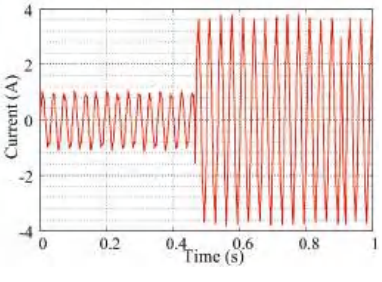

Figure 25. Current in phase A at $n_{A\ s/c} = 8\%$.

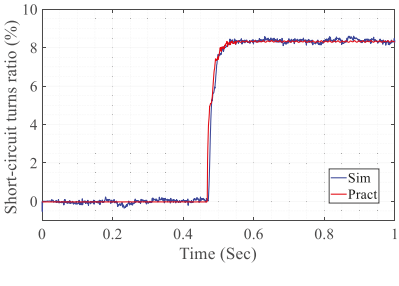

Figure 26. Estimation of 8% short circuit turns ratio in phase A.

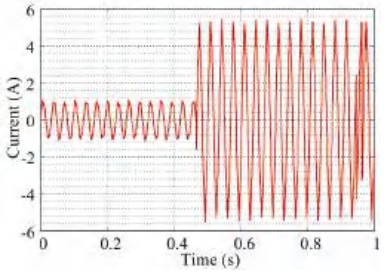

Figure 27. Current in phase A at $n_{A\,s/c}$ = 12%.

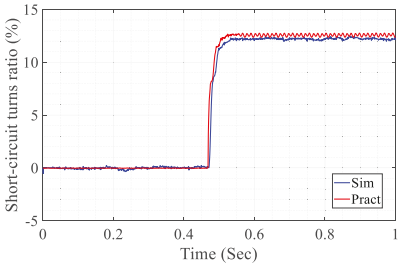

Figure 28. Estimation of 12% short circuit turns ratio in phase A.

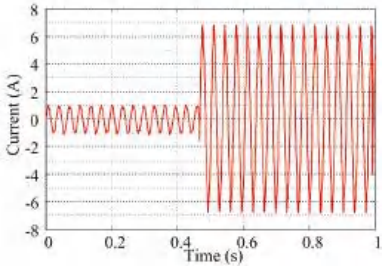

Figure 29. Current in phase A at $n_{A\,s/c}$ = 16%.

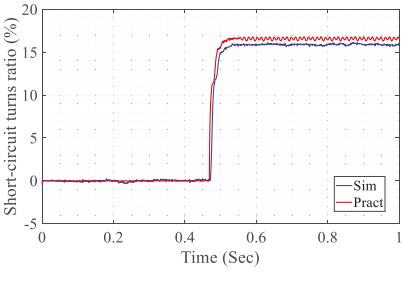

Figure 30. Estimation of 16% short circuit turns ratio in phase A.

5.4. Tuning of Covariance Matrices

Figure 31 shows the dynamic estimation response with different values of evolution time constant of the estimated parameter (τ) in the presence of a 16% fault in phase A. The weighting matrices (Q and R) were chosen based on measuring the variance of input noise and the variance of output

noise to achieve the required fast dynamic response for the estimation of the parameters at different operating conditions. However, the change in the weighting matrices caused changes in the nature of the estimation response.

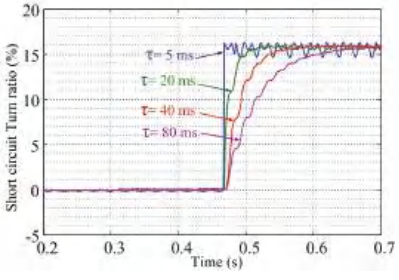

Figure 31. Estimation response with different τ at a constant frequency of 30 Hz.

5.5. Robustness Test

As in the simulation, the machine was tested using different load conditions; this approach tested the parameter estimation response to various load conditions. The tests are listed as following:

Test 1: Variation of frequency from 20 Hz to 50 Hz with a 10 Hz step.

Test 2: Variation of load Current variation from 0.72 A to 2.25 A by 0.75 A step at a constant frequency of 30 Hz.

The EKF showed a constant response in assays with different frequencies (20 Hz, 30 Hz, 40 Hz and 50 Hz) in the presence of 4%, 8%, 12%, and 16% stator inter-turn fault in phase A, and a load current of 0.72 A in a healthy state (Table 2). This emphasized the robustness of this technique when there was a variation in frequency. Moreover, the results confirmed the simulation results for the same machine during the same operating and fault conditions.

Table 2. EKF estimation response with different frequencies at constant load current in phase A.

Case	Freq (Hz)	Exact	Simulation	Practical
		$n_{A\ s/c}$ (%)	$n_{A\ s/c}$ (%)	$n_{A\ s/c}$ (%)
1	20	2%	2.15	1.94
2	20	4%	4.3	3.62
3	20	8%	8.3	7.52
4	20	10%	10.3	9.77
5	20	12%	12.22	12.1
6	20	16%	15.9	16.5
7	30	2%	2.15	1.97
8	30	4%	4.3	3.8
9	30	8%	8.3	7.85
10	30	10%	10.3	9.81
11	30	12%	12.22	11.8
12	30	16%	15.9	16.1
13	40	2%	2.2	1.97
14	40	4%	4.3	3.7
15	40	8%	8.5	7.53
16	40	10%	10.2	9.9
17	40	12%	12.3	12.3
18	50	2%	2.2	2.1
19	50	4%	4.1	4.1
20	50	8%	8.4	7.94
21	50	10%	10.2	10
22	50	12%	12.2	11.8

Besides, the estimation response was tested when exposed to variations in the current (1.5 A and 2.25 A) and at a constant frequency of 30 Hz. Again, the response of the EKF technique showed a robust estimation in load current variation at a constant frequency, (Table 3). For safety conditions, it was not able to emulate short circuit inter turns fault more than 12% as the current in the faulty state went over 5 A; 5 A being the maximum load current for this machine.

Table 3. EKF estimation response with different load currents in phase A at a constant frequency.

Case	Load Current (A)	Exact	Simulation	Practical
		$n_{A\ s/c}$ (%)	$n_{A\ s/c}$ (%)	$n_{A\ s/c}$ (%)
1	0.72	2%	2.15	1.97
2	0.72	4%	4.3	3.8
3	0.72	8%	8.3	7.85
4	0.72	10%	10.3	9.81
5	0.72	12%	12.22	11.8
6	0.72	16%	15.9	16.1
7	1.5	2%	2.15	2
8	1.5	4%	4.3	3.9
9	1.5	8%	8.3	8.2
10	1.5	10%	10.3	9.9
11	1.5	12%	12.22	12.1
12	2.25	2%	2.2	1.97
13	2.25	4%	4.3	3.85
14	2.25	8%	8.5	7.9
15	2.25	10%	10.2	9.5
16	2.25	12%	12.3	12

5.6. Decision-Making Process

The decision was taken based on the estimated total internal current in all three phases of the machine. The loads were divided into two groups: critical loads and uncritical loads were connected through contactors K2 and K1, respectively. To prevent the propagation of internal inter-turn faults inside the machine, there are two proposed scenarios:

- the disconnection of the machine;
- load shedding.

Figure 32 shows the flowchart presenting the FDS EKF technique and the proposed scenarios based on the operator's choice.

5.6.1. Scenario 1: The Disconnection of the Machine

This solution provides for the safety of the machine and prevents the propagation of the fault to other turns and phases. However, this solution affects the reliability of the operation, and it requires a backup for the disconnected generator.

This scenario is presented in the experimental work at RMS load current of 1.5 and 30 Hz frequency, in a healthy state the machine gives $n_{A\ s/c} = 0$, $n_{B\ s/c} = 0$ and $n_{C\ s/c} = 0$. At $t = 0.5$ s. A 4% inter-turn fault exists in phase A, the estimated parameter $n_{A\ s/c} = 4.1\%$ and the total estimated internal current reached an RMS value of 2.8 A. As the FDS works in parallel with the protection system of the machine, the disconnection of the machine will be based on the extremely inverse time (EIT) thermal characteristics curve of overcurrent relay based on IEEE standard [46], the expected time to disconnect the machine is 17 s, at TDS = 0.1 s. Figure 33b,c show the detection time and disconnection time of contactor K1 and contactor K2 after detecting the presence of a fault. An LCD was used to monitor the situation of the machine in both the healthy and faulty states; it also shows the expected disconnection time of both contactors and the position of the loads' contactor to inform the operator about the situation.

5.6.2. Scenario 2: Load Shedding

The second scenario is the disconnecting of some uncritical loads (contactor K1) to decrease the total current of the machine allowing it to run under the fault condition. This solution offers the reliability for the process; the machine can continue running in the presence of a fault but with partial loading. This solution does not solve the main problem of internal fault, but it gives the operator a suitable time to take corrective action; the fault may propagate for other turns or phases, respectively, increasing the internal short circuit current, causing a severe fault.

This scenario was implemented at RMS load current of 1.5 A and 30 Hz frequency; at t = 0.5 s, 2% inter-turn fault was emulated in phase C, which caused an increase in the total estimated internal current to 2 A. The fault was indicated, and the first group of loads (the uncritical loads) connected through contactor K1 was disconnected (Figure 34a). The disconnection of K1 decreased the current in the machine, and the total current became 1.25 A, allowing the machine to return to its normal state for a definite time and consequently canceling the alarm indication. After a time, the fault percentage increased to 8%, causing an increase in the internal current. In this case, the right decision was to disconnect the machine to solve the internal fault problem. The machine was disconnected after the estimated time based on the EIT characteristics of the overcurrent relay.

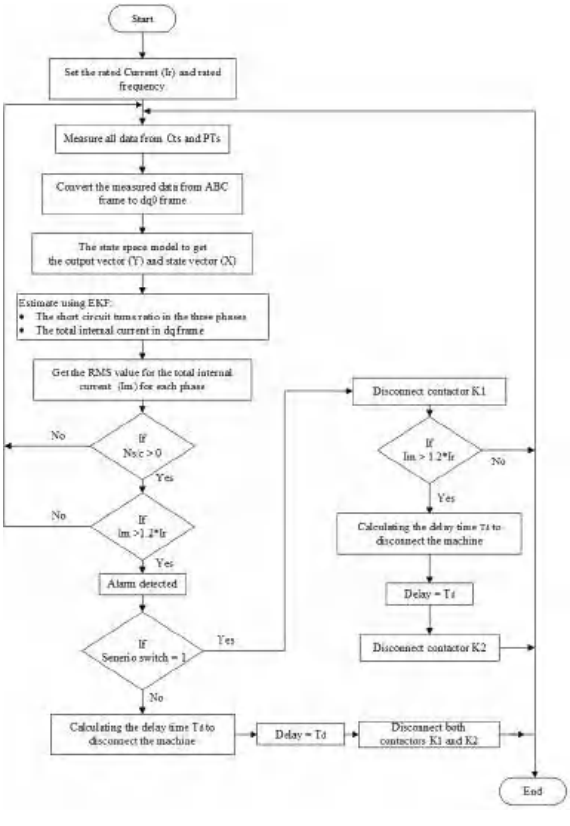

Figure 32. Decision-making process scenarios flowchart.

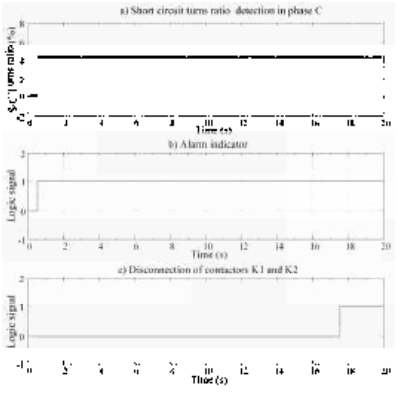

Figure 33. Scenario 1 Alarm indication and machine disconnection.

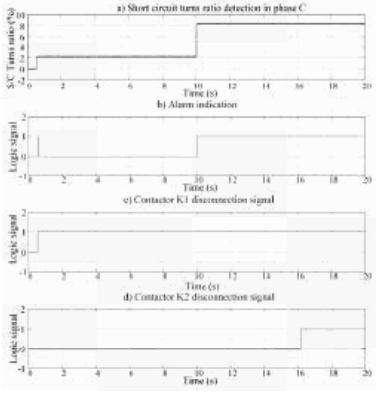

Figure 34. Scenario 2 Alarm indication and contactors disconnection.

6. Conclusions

The paper presents the detection and isolation of PMSG stator windings faults using the EKF and the UKF, which are model-based techniques. The model of the faulty machine was implemented in the state-space model using the machine equations in the dq-frame. The estimated states of the EKF and the UKF techniques were the short circuit turns ratio in each phase. It was noted that the proposed techniques have the following advantages:

- a fast and accurate response in relation to the time needed to take action in real time;
- a robust estimation, in the presence of process and measurement noises, in addition to load and frequency variations.

On the other hand, the UKF technique overcomes the EKF technique drawback of the inaccuracy of the technique in case of severe faults, as it is a nonlinear system and it was linearized around a definite operating point, and so the error of estimation increased as the value of the short circuit turn ratio increased.

Also, the tuning of the weighting matrices (Q and R) has a great impact on the estimated parameters. As indicated in the result, an increase in Q implies an acceleration of the dynamic response of the fault indicator with an increase in noise sensitivity, however, decreasing Q implies better filtering with a decrease in the dynamic response.

The results of this paper point to several exciting directions for future research work. The proposed technique can be used on FD of different types of faults such as bearing, eccentricity, and demagnetizations faults in machines. Moreover, other types of FD techniques may be used, such as artificial intelligence-based techniques and signal-based techniques, and comparing their results with the results of the EKF Technique. This result raises the ability to implement the fault tolerant control (FTC) technique in case of faults such as using the model predictive control (MPC) [47], which would increase the reliability of the machine safety-critical applications.

Author Contributions: Conceptualization, W.E.S., M.A.E.G. and A.L.; methodology, W.E.S. and M.A.E.G.; software, W.E.S.; validation, W.E.S., M.A.E.G. and A.L.; formal analysis, W.E.S., M.A.E.G. and A.L.; investigation, W.E.S., M.A.E.G. and A.L.; resources, W.E.S. and M.A.E.G.; data curation, W.E.S. and M.A.E.G.; writing—original draft preparation, W.E.S. and M.A.E.G.; writing—review and editing, W.E.S. and M.A.E.G.; visualization, W.E.S.; supervision, M.A.E.G. and A.L.; All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

L_d	Direct stator synchronous inductance.	mH	$y_m(t)$	Output vector.	
L_q	Quadrature stator synchronous inductance.	mH	T_s	Sampling period.	Sec
$[V_s]_{dq}$	Direct and quadrature stator voltages.	Volts	$I_{S/C}$	Short-circuit current.	Ampere
$P(\theta)$	dq transformation matrix.		$R_{S/C}$	Short-circuit resistance.	Ω
θ	Electrical angular position.	rad	$n_{S/C}$	Short-circuited turns ratio.	%
ω_e	Electrical angular velocity	rad/s	$\widetilde{F}_k$	State equation of the discrete model.	
[E]	Electromotive forces vector.	Volt	A_m	State matrix.	
$[Z_{s/c}]$	Equivalent fault impedance.	Ω	Q	State noises covariance matrix.	
$\widetilde{X}_{e_k}$	Extended state vector.		$W_m(t)$	State noises vector.	
$\hat{X}_{k\|k}$	Extended state vector.		$x_m(t)$	State vector.	
$\theta_{\frac{s}{c}}$	Fault localization angle.		$[I_s]_{dq}$	Stator currents vector after variable change in dq-frame.	Ampere
$Q\left(\theta_{\frac{s}{c}}\, k\right)$	Fault localization matrix.		$[I'_s]_{dq}$	Stator currents vector in dq-frame.	Ampere
D_m	Feed forward matrix.		R_S	Stator resistance.	Ω
J	Inertia	Kg.m^2	L_S	Stator synchronous inductance.	mH
B_m	Input matrix.		P	The electromechanical power	Watts
$u_m(t)$	Input vector.	-	$P_{k\|k}$	The error covariance matrix at time k	
K_k	Kalman gain		$\widetilde{H}_k$	The output equations of the discrete linearized model.	
T_m	Load torque	Nm	$P_{k\|k-1}$	The prior estimate of P_k	
R	Measurement noises covariance matrix		$\widetilde{F}_K$	The state equations of the discrete linearized model.	
$V_m(t)$	Measurement noises vector.		τ	The time constant of the estimated parameters.	Sec
H_k	Output equation of the discrete model.		σ_u	The variance of input signals noises.	
C_m	Output matrix.		σ_y	The variance of output signals noises.	

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GaN-Based DC-DC Resonant Boost Converter with Very High Efficiency and Voltage Gain Control

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Received: 29 October 2020; Accepted: 30 November 2020; Published: 3 December 2020

Abstract: This paper presents a concept for the operation of a resonant DC–DC switched-capacitor converter with very high efficiency and output voltage regulation. In its basic concept, such a converter operates as a switched-capacitor voltage doubler (SCVD) in the Zero Current Switching (ZCS) mode with a constant output voltage. The proposed methods of switching allow for the switched-capacitor (SC) converter output voltage regulation, and improve its efficiency by the operation with Zero Voltage Switching (ZVS). In this paper, various switching patterns are proposed to achieve high efficiency and the output voltage control by frequency or duty cycle regulation. Some examples of the application of the proposed switching patterns are presented: in current control at the start-up of the converter, in a bi-directional converter, and in a modular cascaded system. The paper also presents an analytical model as well as the relationships between the switching frequency, voltage ratio and efficiency. Further, it demonstrates the experimental verification of the waveforms, voltage ratios, as well as efficiency. The proposed experimental setup achieved a maximum efficiency of 99.228%. The implementation of the proposed switching patterns with the ZVS operation along with the GaN-based (Gallium Nitride) design, with a planar choke, leads to a high-efficiency and low-volume solution for the SCVD converter and is competitive with the switch-mode step-up converters.

Keywords: boost converters; DC–DC power converters; GaN switch; resonant power conversion; zero-current switching (ZCS); zero-voltage switching (ZVS)

1. Introduction

The switched-capacitor (SC) conversion principle applied in power electronic converters is a promising technology [1]. Switched-capacitor topologies are often proposed for the DC–DC conversion, which can achieve favorable features such as a high voltage ratio or light weight [1–27]. In some concepts, the SC converters can achieve continuous voltage regulation, as in references [2–4]. The SC converters, such as multipliers, can operate with a fixed voltage gain [5,6] or a discrete voltage ratio variation [7]. A switched-capacitor power converter can operate as a zero-current-switching (ZCS) circuit with limited current stress of its components by the application of oscillatory circuits for the recharging of the capacitors. Zero current switching (ZCS) converters can achieve high efficiency, which is demonstrated in [5–7]. A substantial part of losses in the SC converters results from conduction losses. This is reported in [4] for a resonant converter, discussed in detail in [5] for a voltage multiplier, and analyzed in [8] in a generic losses model of losses in the SC converters. However, the switching loss is still an important subject of an investigation into SC converters. Previous works related to the efficiency of the SC multipliers (SCVMs) [5–7] show that the losses associated with the discharging of the transistor output capacitance (C_{OSS} loss) can be significant. The reason for this is that the transistors of an SC converter operating in the ZCS mode are turned-on with the output capacitance

charged. However, in the SC resonant doubler (SCVD—such as that presented in Figure 1), their output charge can be reduced by the reverse current flow in the transistor before its turn-on. Therefore, this paper introduces a method of switching off the SCVD (Figure 1), where the switching pulse is shorter than half the period of the oscillations in the resonant circuit. The method of efficiency improvement, by phase-shift control in a resonant switched capacitor converter (RSCC), has been demonstrated in [2] and developed in [3] with the use of the (Gallium Nitride) GaN switches. In the classic switched-capacitor voltage multiplier [5], the Zero Voltage Switching (ZVS) operation (with hard turn-off of the switches) is not applicable, as the topology does not allow for the current termination in the resonant circuits.

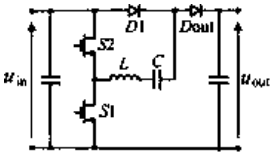


Figure 1. GaN-based resonant switched-capacitor voltage doubler (SCVD) with output voltage range from U_{in} to $2U_{in}$.

For the highest-efficiency operation, the switch needs to be turned off shortly before the zero-crossing of the oscillating current, and the other switch is turned on during its reverse conduction. In this mode, the ZVS and the low-current switching (LCS) is achieved when sufficiently fast switches are used. This can be accomplished by applying GaN switches. Other features of a GaN switch can also be favorable for the resonant SCVD. The linear function of the output capacitance C_{OSS} versus drain-source voltage V_{ds} is meant to improve the shape of the currents in the oscillatory circuits. The drain-source on resistance $R_{ds(on)}$ increase versus temperature is lower than in the case of silicon MOSFETs, which allows for operating at a higher temperature with high efficiency. A smaller area of GaN devices versus Si devices is beneficial for high power density design as well. Furthermore, a low gate charge of the GaN switch is important in this converter. Other features of GaN switches can be found in [28]. In [5], an impact of the dead-time between the input current pulses on the efficiency is demonstrated. The method of the reduction in Q_{oss} losses (the losses resulting from the output charge Q_{oss} discharge at transistor turn-ons) that is proposed in this paper improves the input current shape and allows for a decrease in both the root mean square (RMS) value of the currents in the SC converter, and its resistive losses. In [29], a comparison of power dissipation under the soft switching operation is presented between Si MOSFET 650 V, SiC MOSFET 900 V, GaN E-HEMT 600 V and GaN GIT 600 V. The lowest losses are reported there for the GaN GIT transistors (such type of switches is used in the experimental tests presented in this paper). In an SCVD design, this requires the application of switches with blocking voltage above 650 V (voltage limit of majority superjunction MOSFETs and GaN commercial devices); therefore, a SiC switch can be the most favorable option. In [29], the SiC power dissipation is located between those of GaN and Si superjunction MOSFET, and in [30], it has been concluded that 1200 V SiC devices have a better switching performance than those of 600 V. The application of SiC switches in a bidirectional MRSCC (multilevel resonant switched capacitor converter) converter with voltage ratio 0.5/2 kV is demonstrated in [31], where efficiency of 98.5% was achieved.

The amount of the dissipated energy associated with C_{OSS} losses may be difficult to predict on the basis of C_{OSS} datasheet parameter. In [32], a problem of underestimation of the energy stored in the output capacitance for a large signal operation of superjunction Si MOSFETs is presented. Therefore, the experimental results presented in this paper allow a credible characterization of the parameters of the switches associated with C_{OSS} losses: they present a comparison of efficiencies obtained in the ZCS and ZVS operation. This is one of the important contributions of the paper.

The major disadvantage of SC converters is that they have a limited regulation capability. In the vast majority of cases, the SC converter is a constant-voltage-ratio converter. However, the output voltage regulation is achievable by the use of a suitable topology and control. In this paper, an output voltage regulation capability of the SC doubler is investigated using suitable switching patterns. The method is based on the control of the switching frequency f_S in the range above the frequency of the oscillations in the resonant circuit of the converter and/or the turn-on time of the transistors. This method introduces a hard termination of the current in a transistor, which involves the reverse conduction of the second transistor and its turn-on at zero voltage.

A number of methods for the output voltage regulation in SC converters are analyzed in [2–4,7,9–24]. The phase-shift control in the RSCC presented in [2,3], aside from the improvement of efficiency, introduces the output voltage regulation. However, the methods proposed in this paper use the phase-shift concept as well, but introduce a number of switching patterns, present selected applications of the switching patterns and the analysis of voltage gain and efficiency. The proposed research brings an important contribution to the area of voltage regulation when compared to that presented in [2,3]. Further improvement in the SC resonant converter control by the use of phase shift method, switching frequency and dead-time control depending on the load conditions can be found in [23]. The reference [24] proposes modified Dickson RSCC step-down converters with ZVS operation and full-range regulation via modulation.

In [4], the voltage gain is controlled by the time delay introduced between the switching cycles. In [7], a method of regulation by reducing the number of active switching cells in the multiplier is proposed. This method enables the operation of the converter with various output voltage values in a steady state. The composition of the converter with switched capacitors and switched inductors [9–14] allows for the output voltage regulation by the duty cycle control. However, it requires additional passive magnetic components of significant values when compared with those used in the SCVD analyzed in this paper. A decrease in the volume and weight of converters by reducing the values of their inductive components is an important contemporary trend. Similarly, the elimination of ferrite components in the converter allows for an operation at higher temperatures, which is also favorable in many applications. This is achieved in the proposed SCVD. In [9], a 95 μH choke is used in the system combining SC circuits and a switch-inductor circuit that transfers the energy to the output. In [10], a converter integrating an SC converter and a cell that stores energy in an inductor (430 μH) to achieve high voltage gain with the output voltage regulation is presented. In [11], a converter utilizing a series/parallel connection of inductors (200 μH) and capacitors is proposed for high voltage gain with regulation. A converter operating on the principle of integration of a switch-mode DC–DC regulated converter (with the input inductance of 1.33 mH) with a simple SC circuit composed of diodes and capacitors is presented in [12]. In comparison to the inductors used in [9–12], with values that could be also typical for a DC–DC boost converter, the proposed resonant DC–DC converter uses an inductance of 10.4 μH in the experimental setup.

Some voltage gain control methods utilize the switching frequency variation. Such concepts can be found in [13] for a ladder resonant SC converter (RSC), and in [14,15] for two-switch SC converters.

A method for a variable number of voltage gains is presented in [7], and in [16–20]. In [16], a multilevel output voltage is generated by the appropriate connection of SC components, which gives the input voltage of a half-bridge inverter in the multilevel inverter. In [17], a multilevel DC–DC converter utilizes multiple DC sources. The methods and topologies presented in [18–20] demonstrate the ability for fractional voltage gain control. However, the method analyzed in this paper allows for continuous voltage regulation. Aside from the output voltage control, the proposed switching methods allow for controlling overload states or the start-up of the converter that may lead to an overcurrent.

Another issue, which is novel and presented in this paper, is associated with the bi-directional operation of the SCVD. This example is presented in Section 5, where the reverse conduction of the switch is used. The application of a GaN switch, in this case, makes it possible to avoid the losses connected with a reverse recovery charge (Qrr losses).

All in all, the major contributions of this paper related to efficiency improvement include: the proposition of various switching concepts for power loss reduction, analysis and the development of a model of efficiency, an implementation of the ZVS operation in an SCVD converter, experimental research with a GaN-based SCVD setup, and the demonstration of results related to operation and efficiency of the converter. Some issues such as analysis of various methods of switching and power losses modeling in the SCVD are novel in relation to previous works. This research is a follow-up to the contemporary trends of efficiency improvement and the analyses of prospective topologies for GaN switches favorable implementations.

The major contributions of this paper related to the output voltage regulation in the SCVD converter include the proposition and analysis of various switching methods with a model of voltage gain, and the presentation of examples of their capabilities. Some experimental results of steady-state voltage gain of the converter as well as the dynamical states of the output voltage control are also presented. The application of GaN switches [33,34] makes it possible to implement the proposed switching concepts in high-frequency converters.

The SC converters can be attractive in photovoltaic or fuel-cell low-power systems, where the ability for a high voltage gain is required. The demonstration, in this paper, of bi-directional DC–DC conversion suggests the possibility of implementing it in battery-powered systems. Low weight and volume, achieved in an inductiveless design, can be very favorable in such applications as well. When ferrites are not used in an SC-based converter, it can operate at a higher temperature, which allows the optimization of the converter towards a low volume of heat sink or operation in a higher temperature environment.

The paper is organized in the following way. Section 2 introduces the principle of operation of the SCVD and various switching patterns. The most advantageous patterns are selected and their operation, efficiency, voltage ratio and rated power are presented. Section 3 contains an analysis of the voltage gain control in the SCVD and demonstrates models of output voltage versus switching frequency and power for two switching patterns. Section 4 shows the model of efficiency of the SCVD. In Section 5, we present selected examples of the use of mixed switching patterns for the start-p control of an SCVD, in a bi-directional SCVD, and in a modular SC system. Section 6 presents the laboratory model of the SCVD converter as well as the experimental results which confirm the proper operation, regulation ability and high efficiency of the converter.

2. Operation Principle of the Resonant Power SCVD

According to the basic principle of the operation of a Switch-Capacitor Voltage Multiplier (SCVM) or an SCVD described in [5,6], the converter operates in the ZCS mode. The topology presented in Figure 1 is explained in [6] and in [2,3] (in the case of a converter equipped with four transistors). Both in the charging and discharging cycle of the switched capacitor, the current oscillates and reaches zero value (Table 1, pattern P1). In such a switching method, the theoretical voltage gain of the SCVD equals

$$G_U = U_{\text{out}}/U_{\text{in}} = 2 \tag{1}$$

In the ZCS mode, conduction losses and switching losses of the SCVD are caused by the discharging of the transistor output capacitance during the turn-on transitions (C_{OSS} loss). Using that soft-switching mode, the efficiency of the SCVD has the following analytical model (based on [5]):

$$\eta = 1 - \frac{\pi^2}{16}\frac{P_{\text{in}} r}{U_{\text{in}}^2}\frac{T_{\text{S}}}{T_1} - \frac{\Delta U_D}{U_{\text{in}}} - \frac{\Delta W_{\text{Sn}} f_{\text{S}}}{P_{\text{in}}} \tag{2}$$

where U_{in} is the input voltage, P_{in} is the input power, r denotes the total resistance, both of the circuit of charging and discharging the switched capacitor, including the resistance of the switch, and ΔU_D is the voltage drop across each diode, assumed to remain constant in the forward-conducting state. T_1 is the

conduction time of the transistors, T_S is the switching period, f_S is the switching frequency, and ΔW_{Sn} is the energy lost at turn-ons in the resistances of both the switches in a single switching period.

Table 1. Switching patterns of SCVD and their basic features.

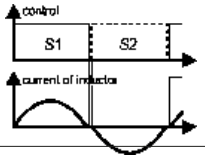
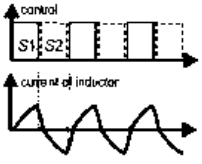
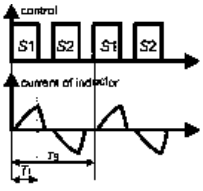
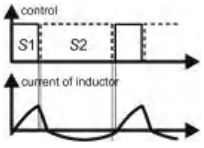
Pattern		
P1		Operation without voltage regulation. Basic ZCS switching [5–7] Features: • problem with C_{OSS} losses.
P2		Regulation by switching frequency variation Operation above the resonant frequency with continuous inductor current. Features: • ZVS-low conduction losses (no blanking times between pulses, low RMS currents) [5], • output voltage regulation is possible by switching frequency regulation, • the output voltage range is limited by the maximal applicable switching frequency. Therefore, $U_{outmin} > U_{in}$.
P3		Regulation by duty cycle control Operation with short pulses and discontinuous inductor current. Features: • output voltage regulation is possible with the constant switching frequency, • the minimum output voltage is not limited: $U_{outmin} = U_{in}$, • hard turn-on.
P4		Regulation by duty cycle control Features: • ZVS, • output voltage regulation is possible with variable switching frequency, • the minimum output voltage is not limited: $U_{outmin} = U_{in}$, • control design similar to typical procedures for switch-mode DC–DC converters with a regulated duty cycle (switching frequency regulation required).

Figure 1 shows that the voltage on the switches of an SCVD equals the input voltage. However, in an SCVM, the voltages on the switches exceed the input voltage, and they increase in the switching cells nearer to the output [5].

In the case of the application of GaN switches, it is assumed that the converter can operate with very high efficiency under modes when the switches are turned-off while conducting. Therefore, each switching period can consist of four states that are presented in Figure 2.

- State 1: transistor *S*2 is switched-off and transistor *S*1 conducts the source current that charges the switched capacitor (SC);
- State 2: transistor *S*1 is switched-off and transistor *S*2 conducts reversely until the inductance current reaches zero; the charging of the SC is continued in this state;

- State 3: transistor *S*1 is switched-off and transistor *S*2 conducts the current that is forced by the source and the switched capacitor to flow to the output;
- State 4: transistor *S*2 is switched-off and transistor *S*1 conducts reversely until the inductance current reaches zero; the charging of the output capacitor is continued.

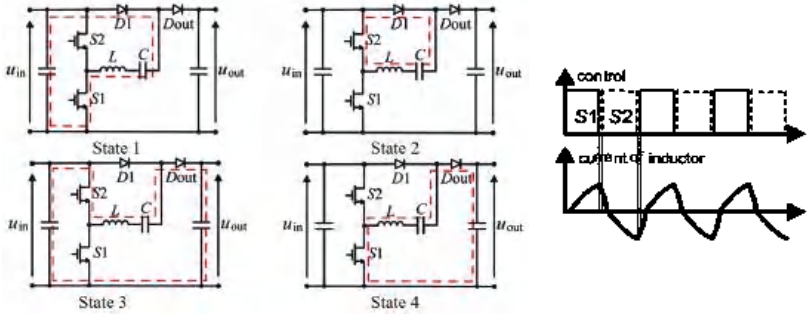


Figure 2. (**a**) Operating states of SCVD in charging and discharging cycles of the switched capacitor. (**b**) Idealized control signals and inductor current waveforms. Pattern P2.

Assuming a hard termination of the transistor current, various switching patterns can be proposed (Table 1). Pattern P1 with the ZCS switching is also shown for comparison.

Under the ZVS operation, the inductor current can discharge the capacitance of a switch before it starts flowing in the reverse direction (Figure 3). This can occur when the switch output capacitance is low, because a high-frequency SC converter is designed with a very low parasitic inductance. Therefore, a GaN or a superjunction MOSFET switch is very favorable in such an operating mode, due to short transition times. As the ZVS operation is more efficient than the ZCS switching, pattern P2 appears to be the most attractive. Furthermore, using pattern P2, switching can be achieved in the ZVS and nearly ZCS mode (LCS–low current switching), which is discussed in more detail in Section 4.

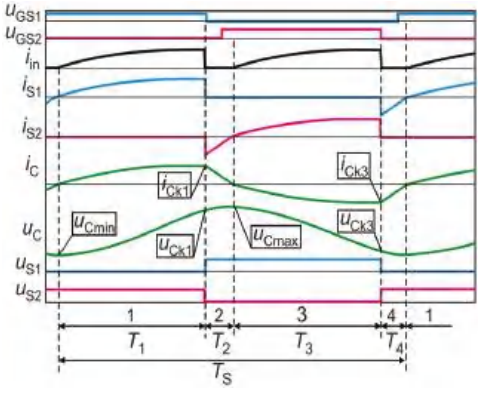


Figure 3. Theoretical time waveforms of currents and voltages in SCVD useful for the analysis–switching pattern P2.

3. Output Voltage Control of SCVD

An idea of the output voltage regulation of the SCVD assumes the shortening of the charging and/or discharging process of the switched capacitor. Thus, a lower amount of energy is transferred

through this component. At the same time, high efficiency of operation can be achieved by reducing the RMS current and eliminating turn-on losses. Thus, when a wide range of switching frequency is assumed on the stage of the design, pattern P2 (Table 1) seems to be the most favorable, and the operation under this pattern will be further analyzed in more detail.

The analysis below refers both to the switching patterns P2 ($T_1 + T_2 + T_3 + T_4 = T_S$, Figure 3) and P3 ($T_1 + T_2 + T_3 + T_4 < T_S$) (Table 1). It assumes ideal power electronic switches, fixed values of input voltage U_{in} and power P_{in}, equal values of resonant frequency f_0 and characteristic impedance ρ of each current path in Figure 2, as well as neglecting parasitic resistances and voltage drops across the power electronic devices, where

$$\omega_0 = 2\pi f_0 = 1 / \sqrt{(LC)},\ \rho = \omega_0 L = \sqrt{L/C} \tag{3}$$

The capacitor is being charged in states 1 and 2 (Figures 2 and 3). The capacitor current and voltage are described by Equations (4)–(11) (time is counted from zero from the beginning of each state)). They present the current of a typical series *LC* circuit supplied from a voltage source, and the voltage across its capacitor, taking into account the initial values of the currents and voltages (Figure 3). The capacitor current and the voltage across it are given by

$$i_C(t) = \frac{U_{in} - U_{Cmin}}{\rho} \sin\omega_0 t = I_m \sin\omega_0 t \tag{4}$$

$$u_C(t) = U_{in} - (U_{in} - U_{Cmin}) \cos\ \omega_0 t \tag{5}$$

in cycle 1, with $i_C\ (T_1) = I_{Ck1}$, $u_C(T_1) = U_{Ck1}$, and by (6) and (7)

$$i_C(t) = I_{Ck1} \cos\ \omega_0 t - \frac{U_{Ck1}}{\rho} \sin\omega_0 t \tag{6}$$

$$u_C(t) = U_{Ck1} \cos\ \omega_0 t + \rho\, I_{Ck1} \sin\omega_0 t \tag{7}$$

in cycle 2, with $i_C\ (T_2) = 0$, $u_C(T_2) = U_{Cmax}$.

The capacitor is being discharged in states 3 and 4 (Figures 2 and 3). The capacitor current and voltage are as follows:

$$i_C(t) = -(U_{in} - U_{out} + U_{Cmax})\ /\rho\ \sin\omega_0 t \tag{8}$$

$$u_C(t) = U_{out} - U_{in} + (U_{in} - U_{out} + U_{Cmax})\ \cos\ \omega_0 t \tag{9}$$

in cycle T_3, with $i_C\ (T_3) = I_{Ck3}$, $u_C(T_3) = U_{Ck3}$, and

$$i_C(t) = I_{Ck3} \cos\omega_0 t + (U_{out} - U_{Ck3})/\rho\ \sin\omega_0 t \tag{10}$$

$$u_C(t) = U_{out} - (U_{out} - U_{Ck3})\ \cos\ \omega_0 t + \rho\, I_{Ck3} \sin\omega_0 t \tag{11}$$

in cycle 4, with $i_C\ (T_4) = 0$, $u_C(T_4) = U_{Cmin}$.

For further analysis, it is assumed that

$$T_1 = T_3, \qquad T_2 = T_4 \tag{12}$$

$$I_{Ck3} = -I_{Ck1} \tag{13}$$

I_m (4) is the amplitude of the input current and the switched capacitor current, and can be calculated based on the expression

$$I_{inav} = \frac{P_{in}}{U_{in}} = \frac{2}{T_S}\int_0^{T_1} I_m \sin\omega_0 t dt = \frac{1}{\pi}\frac{f_S}{f_0} I_m \left[1 - \cos\left(2\pi\frac{T_1}{T_0}\right)\right] \tag{14}$$

All the currents and voltages in the SCVD can be computed based on (4)–(14).

Introducing normalized quantities

$$\begin{gathered} \underline{I}_{\mathrm{mn}} = \frac{I_{\mathrm{m}}}{U_{\mathrm{in}}/\rho},\ \underline{I}_{\mathrm{Ck1n}} = \frac{I_{\mathrm{Ck1}}}{U_{\mathrm{in}}/\rho},\ \underline{P}_{\mathrm{in\_n}} = \frac{P_{\mathrm{in}}}{U_{\mathrm{in}}^2/\rho} \\ \underline{U}_{\mathrm{Ck1n}} = U_{\mathrm{Ck1}}/U_{\mathrm{in}},\ \underline{U}_{\mathrm{Cmin-n}} = U_{\mathrm{Cmin}}/U_{\mathrm{in}},\ \underline{U}_{\mathrm{Cmax-n}} = U_{\mathrm{Cmax}}/U_{\mathrm{in}},\ \underline{U}_{\mathrm{outn}} = U_{\mathrm{out}}/U_{\mathrm{in}} \\ \underline{U}_{\mathrm{outn}} = U_{\mathrm{out}}/U_{\mathrm{in}} \\ \underline{f}_{\mathrm{Sn}} = f_{\mathrm{S}}/f_0,\quad \underline{T}_{1\mathrm{n}} = T_1/T_{\mathrm{S}},\quad \underline{T}_{2\mathrm{n}} = T_2/T_{\mathrm{S}} \end{gathered} \tag{15}$$

we obtain

$$\underline{I}_{\mathrm{mn}} = \frac{\pi \underline{P}_{\mathrm{in-n}}/\underline{f}_{\mathrm{Sn}}}{1 - \cos\left(2\pi \underline{T}_{1\mathrm{n}}/\underline{f}_{\mathrm{Sn}}\right)},\ \underline{I}_{\mathrm{Ck1n}} = \underline{I}_{\mathrm{mn}} \sin\left(2\pi \underline{T}_{1\mathrm{n}}/\underline{f}_{\mathrm{Sn}}\right) \tag{16}$$

$$\underline{U}_{\mathrm{Cmin-n}} = 1 - \underline{I}_{\mathrm{mn}},\quad \underline{U}_{\mathrm{Ck1}n} = 1 - \underline{I}_{\mathrm{mn}} \cos\left(2\pi \underline{T}_{1\mathrm{n}}/\underline{f}_{\mathrm{Sn}}\right) \tag{17}$$

$$\underline{T}_{2\mathrm{n}} = \underline{f}_{\mathrm{Sn}} \operatorname{arctg}\left(\underline{I}_{\mathrm{Ck1n}}/\underline{U}_{\mathrm{Ck1n}}\right)/(2\pi) \tag{18}$$

$$\underline{U}_{\mathrm{Cmax-n}} = \underline{U}_{\mathrm{Ck1n}} \cos\left(2\pi \underline{T}_{2\mathrm{n}}/\underline{f}_{\mathrm{Sn}}\right) + \underline{I}_{\mathrm{Ck1n}} \sin\left(2\pi \underline{T}_{2\mathrm{n}}/\underline{f}_{\mathrm{Sn}}\right) \tag{19}$$

$$\underline{U}_{\mathrm{outn}} = \underline{U}_{\mathrm{Cmin-n}} + \underline{U}_{\mathrm{Cmax-n}},\qquad \underline{U}_{\mathrm{Ck3}n} = \underline{U}_{\mathrm{outn}} - \underline{U}_{\mathrm{Ck1}n} \tag{20}$$

3.1. Pattern P2—Continuous Capacitor Current Mode

The capacitor current is continuous if $T_1 + T_2 + T_3 + T_4 = T_{\mathrm{S}}$ (pattern P2—Table 1 and Figure 3), which corresponds to (12)

$$T_{\mathrm{S}} = 2(T_1 + T_2) \tag{21}$$

This switching pattern can be easily obtained by varying T_S and using long gate pulses, as shown in Table 1 for pattern P2–times T_1 and T_2 (Figure 3) will be set automatically.

Using (16)–(20) and taking into account that (21) $\underline{T}_{2\mathrm{n}} = 1/2 - \underline{T}_{1\mathrm{n}}$ yields

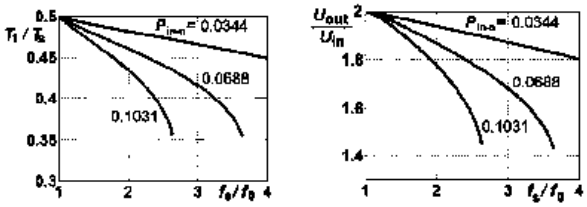
$$\pi\left(1 - 2\underline{T}_{1\mathrm{n}}\right) = \underline{f}_{\mathrm{Sn}} \operatorname{arctg}\left[\frac{\pi \underline{P}_{\mathrm{in-n}}/\underline{f}_{\mathrm{Sn}} \sin\left(2\pi \underline{T}_{1\mathrm{n}}/\underline{f}_{\mathrm{Sn}}\right)}{1 - \left(1 + \pi \underline{P}_{\mathrm{in-n}}/\underline{f}_{\mathrm{Sn}}\right) \cos\left(2\pi \underline{T}_{1\mathrm{n}}/\underline{f}_{\mathrm{Sn}}\right)}\right] \tag{22}$$

From (22), normalized conduction time $\underline{T}_{1\mathrm{n}} = T_1/T_{\mathrm{S}}$ of the transistor can be computed numerically. Figure 4 presents $\underline{T}_{1\mathrm{n}}$ (a), and normalized output voltage $\underline{U}_{\mathrm{outn}}$ (b) as a function of $\underline{f}_{\mathrm{Sn}}$ for three values of $\underline{P}_{\mathrm{in\text{-}n}} = P_{\mathrm{in}}/(U_{\mathrm{in}}{}^2/\rho)$: 0.0344, 0.0688, and 0.1031. The value of $\underline{P}_{\mathrm{in\text{-}n}} = 0.0688$ corresponds to, e.g.,: $U_{\mathrm{in}} = 200$ V, $P_{\mathrm{in}} = 400$ W, and $\rho = 6.876$, which can be obtained for, e.g., $L = 10.4$ μH and $C = 0.22$ μF. These parameters correspond to those of the experimental setup presented in Section 6.

In switching pattern P2, the theoretical lower limit of the normalized switching frequency $\underline{f}_{\mathrm{Sn}}$ is 1, which corresponds to switching pattern P1 (Table 1) with zero dead-times. The upper limit of $\underline{f}_{\mathrm{Sn}}$ results from (21), and it depends on power, which can be seen in Figure 4.

The normalized conduction time T_1/T_{S} of the transistors decreases with increasing frequency, and the power is larger as the decrease rate is higher. Moreover, it is very important that varying f_{S} affects the output voltage. In switching pattern P2, it is possible to control the output voltage in the range of ca. 1.45 U_{in} to 2 U_{in}. An increase in f_{S} results in decreasing voltage gain [see Figure 4b]. As in the case of T_1/T_{S}, the larger the power, the higher the decrease rate.

In the discussed switching pattern P2, the capacitor is never discharged to zero volts.



(**a**) (**b**)

Figure 4. (**a**) Normalized conduction time $T_{1n} = T_1/T_S$ of transistors, (**b**) normalized output voltage $U_{outn} = U_{out}/U_{in}$: as a function of $f_{Sn} = f_S/f_0$ for three values of normalized power $P_{in\text{-}n} = P_{in}/(U_{in}^2/\rho)$: 0.0344, 0.0688, and 0.1031. Switching pattern P2.

3.2. Pattern P3—Discontinuous Capacitor Current Mode

The continuous current mode is advantageous in terms of optimizing the converter's efficiency. However, the converter can also be operated at a fixed frequency f_S by varying the conduction time T_1 of the transistors. If $\underline{T}_{1n} = T_1/T_S$ is lower than that in Figure 4a, the capacitor current becomes discontinuous–pattern P3 in Table 1. This operating mode offers a wider range of output voltage control.

The conduction time T_1 of the transistors is limited. Its maximum normalized value is equal to that shown in Figure 4a and its minimum value is limited by two factors. The first is the condition $U_{Cmin} \geq 0$, leading to

$$\underline{T}_{1min-n} = T_{1min}/T_S = \underline{f}_{Sn}/(2\pi)\arccos\left(1 - \pi\underline{P}_{in-n}/\underline{f}_{Sn}\right) \tag{23}$$

The second factor is the requirement for $\underline{U}_{outn} \geq 1$, which results from the topology (Figure 1).

The output voltage regulation can be done by varying transistor conduction time T_1 at a given frequency f_S, where a decrease in T_1 leads to a decrease in the voltage gain ratio (Figure 5). This ratio falls with the rise of frequency f_S. Moreover, U_{out} is lower at higher powers.

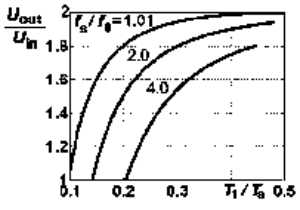


Figure 5. Normalized output voltage U_{out}/U_{in} of the converter as a function of $T_{1n} = T_1/T_S$ for three values of $f_{Sn} = f_S/f_0$: 1.01, 2.0, and 4.0. $P_{in\text{-}n} = P_{in}/(U_{in}^2/\rho) = 0.0344$. Switching pattern P3.

4. Efficiency of the SCVD

4.1. Model of Efficiency of the SCVD–Maximum Efficiency of the Converter without Switching Losses

The efficiency of the SCVD is determined by the resistance of its components, voltage drops on the diodes, input voltage, power, operating frequency, and the switching pattern. The following calculations have been performed for the SCVD with GaN switches using pattern P2 (Table 1). The assumptions for the analysis given in Section 3 remain valid, except for taking into account the circuit parasitic resistances, which are now added to the transistor resistances, and voltage drops on the diodes. Moreover, the conduction losses in the GaN transistors are computed taking into account its $R_{DS(on)}$, both for forward and reverse conduction. This can be done as the gate signals are applied during nearly the half-period $T_S/2$, except for dead-time, which is very short.

The current $i_{S1}(t)$ in transistor $S1$ is equal to the capacitor current $i_C(t)$ in state 4 (reverse conduction) and state 1 (forward conduction), and equal to zero in states 2 and 3 (Figures 2 and 3). The current $i_{S2}(t)$ in transistor $S2$ is phase-shifted, having the same shape and values. The RMS value of both currents is the same. It can be calculated from

$$I_S = \sqrt{\frac{1}{T_S}\int_0^{T_S} i_{S1}^2(t)\mathrm{d}t} = \sqrt{\frac{1}{T_S}\left[\int_0^{T_1} i_{S1(1)}^2(t)\mathrm{d}t + \int_0^{T_4} i_{S1(4)}^2(t)\mathrm{d}t\right]} \tag{24}$$

where $i_{S1(1)}(t) = i_C(t)$ in state 1 (4), $i_{S1(4)}(t) = i_C(t)$ in state 4 (10), and $T_4 = T_2$ (12). After calculating the integrals using the equations mentioned above, and taking into account relationship (13), current I_S can be presented in the form

$$I_S = \sqrt{I_{SA}^2 + I_{SB}^2 + I_{SC}^2 + I_{SD}^2}. \tag{25}$$

where

$$\begin{aligned} I_{SA}^2 &= \tfrac{I_{Ck1}^2}{2}\left[\underline{T}_{2n} + \tfrac{\underline{f}_{Sn}}{4\pi}\sin\left(4\pi\underline{T}_{2n}/\underline{f}_{Sn}\right)\right] \\ I_{SB}^2 &= \tfrac{\underline{f}_{Sn}}{4\pi} I_{Ck1}\tfrac{U_{Ck3} - U_{out}}{\rho}\left[1 - \cos\left(4\pi\underline{T}_{2n}/\underline{f}_{Sn}\right)\right] \\ I_{SC}^2 &= \tfrac{(U_{Ck3} - U_{out})^2}{2\rho^2}\left[\underline{T}_{2n} - \tfrac{\underline{f}_{Sn}}{4\pi}\sin\left(4\pi\underline{T}_{2n}/\underline{f}_{Sn}\right)\right] \\ I_{SD}^2 &= \tfrac{(U_{in} - U_{Cmin})^2}{2\rho^2}\left[\underline{T}_{1n} - \tfrac{\underline{f}_{Sn}}{4\pi}\sin\left(4\pi\underline{T}_{1n}/\underline{f}_{Sn}\right)\right]. \end{aligned} \tag{26}$$

The current $i_{D1}(t)$ in diode $D1$ is equal to the capacitor current $i_C(t)$ in states 1 and 2, and equal to zero in states 3 and 4 (Figures 2 and 3). The current $i_{Dout}(t)$ in diode Dout is phase-shifted, having the same shape and values as $i_{D1}(t)$. The average value of both currents is the same and equal to

$$I_{Dav} = \frac{1}{T_S}\int_0^{T_S} i_{D1}(t)\mathrm{d}t = \frac{1}{T_S}\left[\int_0^{T_1} i_{D(1)}(t)\mathrm{d}t + \int_0^{T_2} i_{D(2)}(t)\mathrm{d}t\right] \tag{27}$$

where $i_{D1(1)} = i_C(t)$ in state 1 (4) and $i_{D1(2)} = i_C(t)$ in state 2 (6).

$$I_{Dav} = \frac{\underline{f}_{Sn}}{2\pi}\left\{I_m\left[1 - \cos\left(2\pi\underline{T}_{1n}/\underline{f}_{Sn}\right)\right] + I_{Ck1}\sin\left(2\pi\underline{T}_{2n}/\underline{f}_{Sn}\right) - \frac{U_{Ck1}}{\rho}\left[1 - \cos\left(2\pi\underline{T}_{2n}/\underline{f}_{Sn}\right)\right]\right\} \tag{28}$$

Conduction losses ΔP_C are the sum of losses in the transistors and the diodes

$$\Delta P_C = (r_1 + r_2)\, I_S^2 + (\Delta U_{D1} + \Delta U_{Dout})\, I_{Dav} \tag{29}$$

where r_1 and r_2 denote the total resistance, including the resistance of the transistor, in the circuits with $S1$ and $S2$, respectively; ΔU_{D1} is the voltage drop across diode $D1$, and ΔU_{Dout} is the voltage drop across diode Dout (Figure 1). It is assumed that the voltage drops across the diodes remain constant in the conducting state. Therefore, the efficiency is

$$\eta = 1 - \frac{\Delta P_C}{P_{in}} = 1 - \frac{(r_1 + r_2) I_S^2}{P_{in}} - \frac{(\Delta U_{D1} + \Delta U_{Dout}) I_{Dav}}{P_{in}} \tag{30}$$

If the resistances and diode voltage drops are the same, i.e.;

$$r_1 = r_2 = r,\ \Delta U_{D1} = \Delta U_{Dout} = \Delta U_D \tag{31}$$

we can rewrite the efficiency formula in the form

$$\eta = 1 - 2\left(\underline{r}_n \underline{I}_{Sn}^2 + \underline{\Delta U}_{Dn} \underline{I}_{Davn}\right) / \underline{P}_{in-n} \tag{32}$$

where

$$\underline{I}_{Sn} = \frac{I_S}{U_{in}/\rho}, \quad \underline{I}_{Davn} = \frac{I_{Dav}}{U_{in}/\rho}, \quad \underline{r}_n = r/\rho, \quad \underline{\Delta U}_{Dn} = \Delta U_D/U_{in} \tag{33}$$

Figure 6 presents the model of efficiency created on the basis of (32). The peak efficiency achieves a maximum above the resonant frequency. It is assumed that the switching losses are reduced in this area as well.

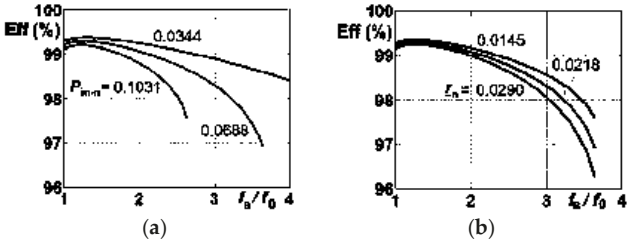


Figure 6. Efficiency of SCVD as a function of $f_{Sn} = f_S/f_0$: (**a**) for three values of $P_{in\text{-}n} = P_{in}/(U^2_{in}/\rho)$: 0.0344, 0.0688, and 0.1031 at $r_n = r/\rho = 0.0218$, (**b**) for three values of $r_n = 0.0145$, 0.0218, and 0.0290 at $P_{in\text{-}n} = 0.0688$. $\Delta U_{Dn} = 0.006$. Switching pattern P2.

4.2. The Switching Concept for Maximum Efficiency

The advantages of the application of the GaN switches in the proposed high-frequency SCVD results from the possibility of using the ZVS mode with low switching losses under the operation above the resonant frequency (low C_{OSS} of the switch and short transition time). It can be assumed that the most favorable case of operation (ZVS), from the efficiency point of view, is achieved by turning-off the transistors just before their current reaches zero. The reverse conduction of the transistors should be as short as possible (Figure 7). When the transistors turn off near the zero crossings of the current, the turn-off loss can be neglected. In an SC converter such as the SCVD, with very small inductors, the application of a GaN switch will make it possible to achieve a highly improved efficiency in the ZVS mode keeping both the dead-dime and reverse-time very short.

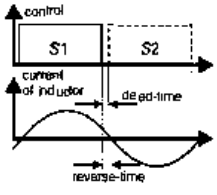


Figure 7. A method for operation with maximum efficiency (Zero Voltage Switching (ZVS), nearly Zero Current Switching (ZCS) (Low-Current Switching—LCS) turn-off and decreased RMS current in comparison to full ZCS case): the use of pattern P2 for high efficiency (pattern P2HE).

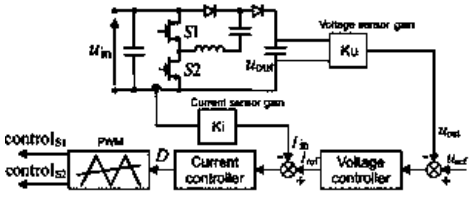
5. Mixed Switching Patterns in Applications

To obtain a functional converter with efficient and effective voltage regulation, various switching patterns can be utilized depending on the operational conditions. Furthermore, the proposed switching patterns can be effectively used in more complex systems created on the basis of the SCVD.

5.1. Start-Up of the Converter

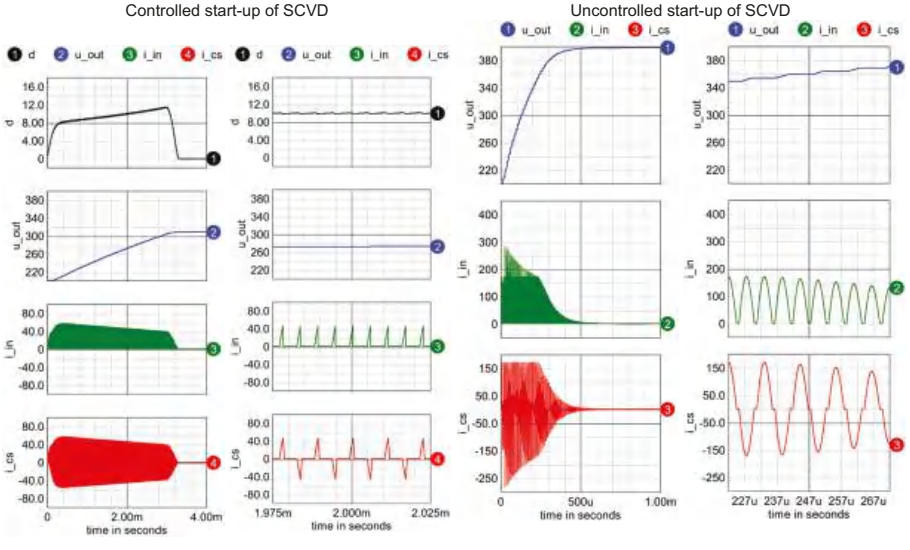
During the start-up of the converter, the SCVD is usually overloaded when pattern P1 is used. The maximum power (P_{max}) of this type of voltage multiplier is proportional to the switching frequency and the switched capacitance C [5]. Under pattern P1, the converter can increase the power as far as the

switched capacitor is not fully discharged in a switching period. The operation of an SCVD with partial discharge and low voltage ripples under the rated power requires the use of a large-enough switched capacitor (C). In this case, the converter's power is $P_{nom} << P_{max}$. When the switches, diodes and the PCB are designed for nominal power P_{nom}, the converter can easily be overloaded. To overcome this issue in conditions of overloading, such as the start-up of the converter, other switching patterns can be used. Figure 8 presents a comparison of waveforms during the start-up with pattern P3 and pattern P1. From these results, it is seen that the overloading of the converter is significantly limited by the appropriate use of the proposed switching pattern P3.



K_u	0.001
K_i	0.01
u_{ref}	0.3
Voltage controller	PI type: K_P=10, K_i = 5× 10^4
Current controller	Integral type: K_i = 5×10^2

(**a**)



(**b**) (**c**) (**d**) (**e**)

Figure 8. (**a**) Closed-loop voltage control system with overcurrent protection and its parameters (pattern P3 with the duty ratio control $D = T_1/T_S$–Table 1). (**b**,**c**) Controlled start-up of SCVD under pattern P3 in the closed-loop system and uncontrolled start-up of SCVD under pattern P1. Waveforms of duty cycle (symbol d (%)), output voltage u_{out} (V), input current i_{in} (A), current i_{Cs} (A) of capacitor C in the cases: (**b**,**d**) full range, (**c**,**e**) zoom. ICAP/4 simulation results. Circuit parameters as in Table 3.

Pattern P3 can be easily achieved in a classic PWM generator (it requires a constant switching frequency and a variable duty ratio). The implementation of this pattern can be achieved by the use of VCO (Voltage Controlled Oscillator), and pattern P4 could require a special hardware design (e.g., in FPGA technology).

5.2. Bi-Directional Converter

A synchronous SCVD makes it possible to convert energy in both directions, which is required in systems with batteries. When the voltages on both sides are constant, the converter should be able to regulate the voltage gain in both directions. Figure 9 presents the concept of such a synchronous SCVD, the most suitable switching pattern (P4), and its operating states. The operation occurs in the following three states (Figure 9b):

(1) In the first state, the SC is being charged from the output voltage source. This state is terminated by turning off the switches *S*1 and *S*4;
(2) State 2—the inductor current goes to zero via *S*2 and *S*3 (reverse conduction);
(3) In state 3—turning on *S*3 starts an oscillation in a new circuit, and the energy is transferred to the input source. This is advantageous since the oscillation continues until the inductor current reaches zero. Breaking this oscillation by switching off *S*3 would start the current flow to the output and charging the output, which would not be favorable to the efficiency of the conversion.

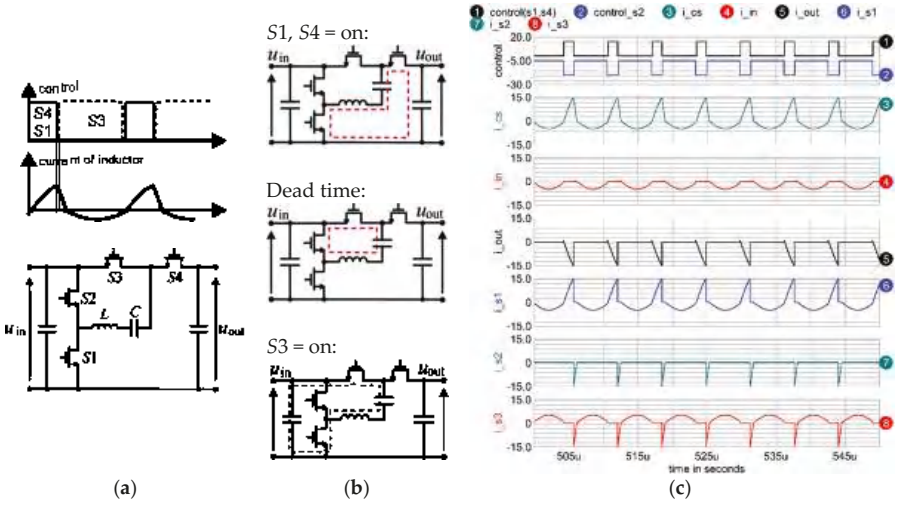


Figure 9. (**a**) Synchronous SCVD and switching pattern P4 with corresponding symbols, (**b**) states in a switching cycle during charging the source by the converter, (**c**) steady-state waveforms during the reverse energy transfer with the use of switching pattern P4 (ICAP/4 simulation results): waveforms of currents (A) and control signals for *S*1, *S*3 and *S*4 (control signal of *S*2 = 1). P_{in} = 500 W. Circuit parameters as in Table 3.

Pattern P4 guarantees a proper operation of the synchronous SCVD, which is confirmed by the steady-state waveforms presented in Figure 9. It assures ZVS of switch *S*3, ZCS turn-on of *S*1 and *S*4, voltage regulation and unidirectional currents of the sources. Other switching patterns enable a bi-directional energy transfer with voltage regulation, but with an unrequired current recirculation between SC and the sources.

5.3. A Series-Connected High-Voltage-Gain System

A section containing capacitors allows for designing modular [23] and cascaded [26,27] converters, where such parameters as the output voltage regulation can be improved. In [27], modular converters composed of series-parallel sections are analyzed. It has been proven there that the series-connected voltage doublers (Figure 10) are the most effective voltage multiplier topology taking into consideration the relation of the number of switches to the voltage gain.

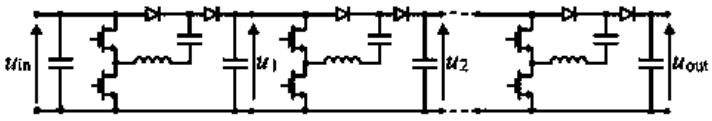


Figure 10. SCVD series in a high-voltage-gain converter.

The SCVD series achieves the voltage gain $G_U = 2^n$, where n is the number of the SCVD converters. In an SCVD series (Figure 10), each internal converter operates in different conditions (voltage and current stress). By suitable use of the proposed switching patterns, the SCVD series can achieve novel unique features such as output voltage regulation and very high efficiency. The most effective mixed switching pattern can depend on such parameters as switching frequency or load. Table 2 presents examples of scenarios for a decision on implementing optimal switching patterns.

Table 2. Examples of scenarios for series SCVD optimal switching.

Scenario	Mixed Switching Patterns
Light-load conditions (low predicted conduction losses, high switching losses)	• The first SCVD, connected directly to the source, regulates the voltage of the converter in the range U_{in}–$2U_{in}$. It operates at the lowest level of voltage with non-significant C_{OSS} losses. It can use pattern P2, and patterns P3 or P4 for a deep voltage decrease with high efficiency. • When the first cell decreases the voltage, the voltages on the switches in all other cells are also decreased, which reduces C_{OSS} losses. It is more beneficial than the voltage regulation by any other cell. • The other cells, except the first, operate with pattern P2HE (Figure 7), which decreases the switching losses significantly.
High-load (predicted conduction losses higher than switching losses in all the cells)	• All the cells should operate with the highest possible voltage to limit conduction losses (pattern P2HE–Figure 7). • The last SCVD, connected directly to the load, regulates the voltage of the converter in the range $(n-1)U_{in}$–nU_{in}, using pattern P2, and patterns P3 or P4. • If a deeper voltage decrease is required, an appropriate middle cell regulates the voltage, e.g., to achieve the range $(n-2)U_{in}$–nU_{in}.

6. Experimental Setup and Test Results

The experimental investigations have been performed in the setup with parameters presented in Table 3 using the equipment listed in Table 4. The efficiency of the GaN-Based DC–DC resonant boost converter was determined using Yokogawa WT1800 power analyzer [35] on the basis of the output to the input power ratio. The range of voltages and currents in the tested converter allows for the use of the internal current and voltage sensors (5 A and 600 V) and achieving an adequate precision of the measurements.

Table 3. Parameters of the laboratory SCVD converter.

Transistors	PGA26E07BA
Diodes	STPSC12065GY-TR
Switched capacitor	220 nF
Inductor	10.4 μH
Input capacitor	4 μF
Output capacitor	4 μF (and 100 μF external bank)
Input voltage	U_{in} = 200 V
Resonant frequency	f_0 = 105.2 kHz

Table 4. Parameters of the laboratory test setup.

Purpose	**Equipment**
PWM signal generator	FPGA-based: DE0-CV Cyclone V Control Board
Measurements	Scope: Tektronix DPO4054 Current probes TCP0030 Voltage probes THDP0200 Power Analyzer Yokogawa WT1800
Supply and load	DC power supply Delta SM300, Rigol DP832, Mixed passive and electronic load LDH400P
IR measurements	FLIR i60

The measurements were intended to verify the basic concepts presented in this paper: the switching strategies and efficiency of the SCVD converter shown in Figure 1. The obtained results confirm the proper operation of the converter under various switching strategies and its high efficiency.

6.1. Switching Pattern P2–Operation with Continuous Capacitor Current Mode

Figure 11 presents examples of selected time waveforms in switching pattern P2. A dead-time of 50 ns has been used; thus, after the turn-off of each transistor, the other transistor begins conducting (reverse conduction and, next, forward conduction) with nearly zero turn-on loss and low conduction loss.

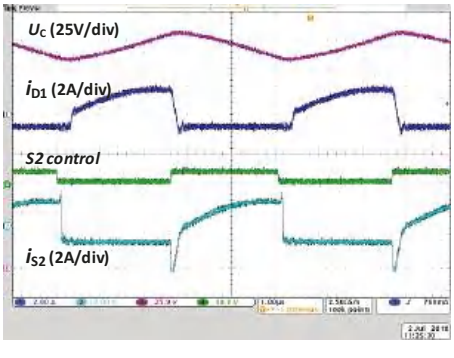


Figure 11. Steady-state operation of SCVD in Continuous Conduction Mode (CCM) and ZVS mode. Waveforms of voltage on switched capacitor C, current of $D1$, control signal of $S2$, and current of transistor $S2$. U_{in} = 200 V, f_S = 201.6 kHz, P_{out} = 400 W, t_M = 50 ns. Switching pattern P2.

6.2. Comparison of Operation in the ZCS Mode (Pattern P1) and ZVS Mode (Pattern P2)

A comparison of the operation below resonant frequency (ZCS) and above that frequency (ZVS) confirms the concept of operation with high efficiency and output voltage control.

Figure 12 presents the operation of the converter in the ZVS and nearly in the ZCS mode. In these conditions, maximum efficiency is achieved. The ZVS mode is maintained, although the negative current of *S*2 is not as clearly visible as in Figure 11. Before the switch *S*2 is turned on, it conducts a negative current and its voltage is zero. On the other hand, the full ZCS mode is visible in Figure 15a.

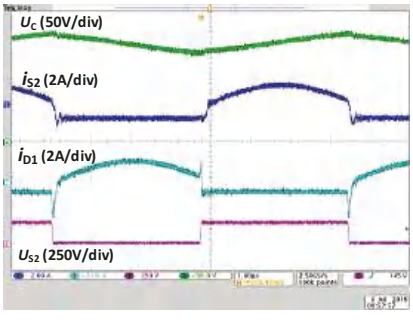
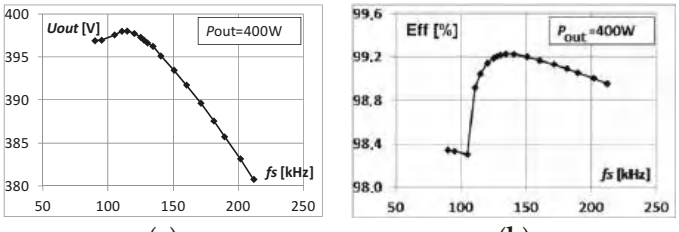


Figure 12. CCM operation of SCVD in steady-state in ZVS and nearly ZCS mode. Waveforms of voltage on switched capacitor *C*, current of transistor *S*2, current of diode *D*1, voltage on transistor *S*2. U_{in} = 200 V, f_S = 201.6 kHz, P_{out} = 400 W. Switching pattern P2.

Figure 13 presents graphs of voltage gain end efficiency versus switching frequency f_S. The efficiency chart (Figure 13b) clearly shows a substantial increase in efficiency when the operating mode changes from the switching pattern P1 to P2. The peak efficiency occurs slightly above f_0. A further increase in the switching frequency leads to a decrease in output voltage (voltage gain regulation) and results in a decrease in efficiency.

Figure 14a–d present the charts of efficiency of the SCVD versus output power for various values of the switching frequency under pattern P2. Figure 14e depicts the relation between the efficiency and the gain, obtained from the data in Figure 13. The highest achieved efficiency is 99.228% at f_S = 134.4 kHz and P_{out} = 396.23 W.



(**a**) (**b**)

Figure 13. (**a**) Output voltage U_{out} and (**b**) efficiency of SCVD as a function of switching frequency f_S. U_{in} = 200 V, P_{out} = 400 W, t_M = 50 ns. Switching pattern P1 (for $f_S < f_0$) and P2 (for $f_S > f_0$).

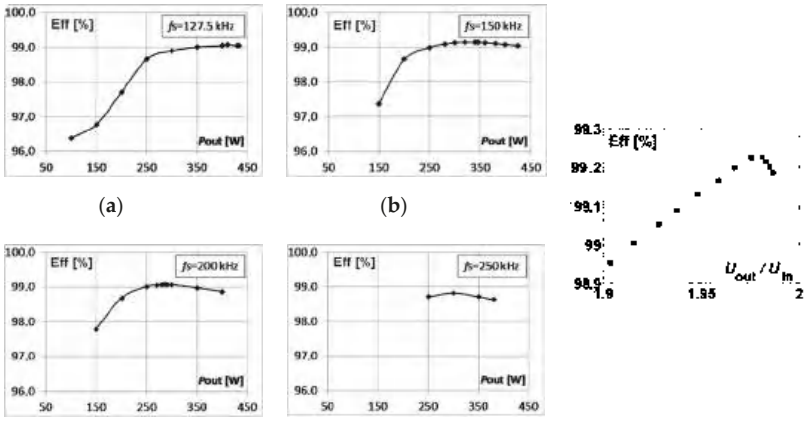


Figure 14. Efficiency of SCVD in CCM mode as a function of: (**a**–**d**) output power P_{out}, (**e**) U_{out}/U_{in} at P_{out} = 400 W. U_{in} = 200 V, t_M = 50 ns. Switching pattern P2.

Further analysis of the ZVS concept in the SCVD, achieved by the introduction of pattern P2, is presented by comparing the waveforms and thermograms of the converter operating in accordance with patterns P2 and P1. The comparison is presented in Figure 15 for P_{out} = 400 W. The IR photos confirm considerably lower losses and heat generation in the transistors when the converter operates using pattern P2 [see Figure 15b,d] versus the case of the ZCS switching with pattern P1 [see Figure 15a,c].

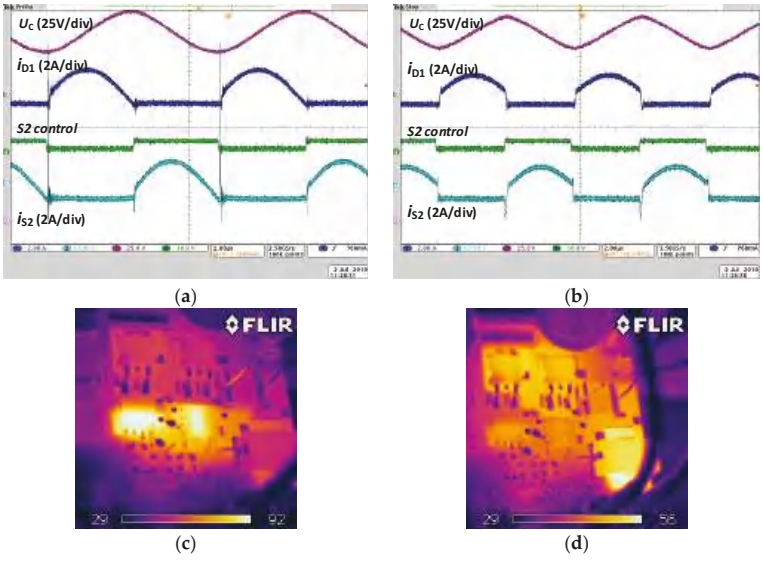


Figure 15. Operation of SCVD in ZCS mode (pattern P1) at f_S = 105 kHz with η = 98.30%, and in ZVS mode (pattern P2) at f_S = 134.4 kHz with η = 99.228%. Steady-state waveforms of voltage on switched capacitor *C*, current of diode *D*1, control signal of transistor *S*2, current of *S*2; IR photos of converter. U_{in} = 200 V, P_{out} = 400 W, t_M = 50 ns. Results (**a**,**c**)—switching pattern P1, results (**b**,**d**)—switching pattern P2.

Figure 16 confirms the proper operation of the converter in switching pattern P3. The inverter operates in discontinuous conduction mode (DCM). Output voltage regulation is possible at a constant switching frequency (Table 1).

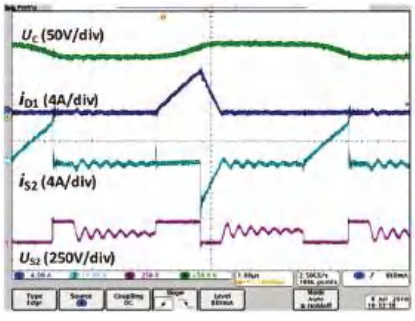


Figure 16. Steady-state operation of SCVD in DCM. Waveforms of voltage on switched capacitor C, current of $D1$, current of transistor $S2$, voltage on transistor $S2$. U_{in} = 200 V, f_S = 134.4 kHz, $D = T_1/T_S$ = 15.6%, t_M = 50 ns. Switching pattern P3.

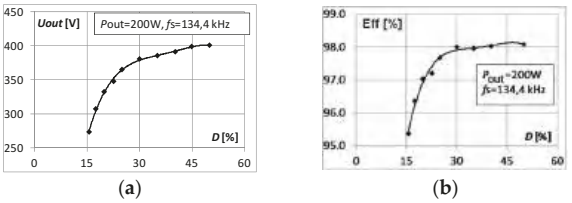
Table 5 shows a comparison of the maximum efficiencies of selected converters presented in recently published papers. The power at that the maximum efficiency was registered, and the type of switches that were used are also listed. (RSCC–resonant switched-capacitor converter, RTBSCC–resonant two-switch boosting switched-capacitor converter, IBC–intermediate bus converter, MRSCC–multilevel resonant switched-capacitor converter). The efficiency of the converter presented in this paper is one of the highest that are reported in the recent bibliography.

Table 5. Comparison of the maximum efficiencies of selected converters presented in recently published papers.

Proposed Solution	Doubler RSCC [3]	RSCC [4]	RTBSCC [14]	High Freq. IBC [33]	MRSCC [31]	Ref. [23]	Ref. [24]
η = 99.228%	η = 99.82%	η = 96%	η = 98.3%	η = 96.7%	η = 98.5%	η = 99.5%	η = 94.6%
P = 400 W	P = 1500 W	P =10 W	P = 23 W	P = 240 W	P = 5 kW	P = 3 kW	P = 140 W
GaN	GaN	MOSFET	MOSFET	GaN	SiC MOSFET	MOSFET	MOSFET

6.3. Output Voltage Regulation by the Switching Pattern P3

The most suitable method for the output voltage regulation in an SCVD is pattern P3, where the capacitor current is discontinuous (Figure 16). Very good effectiveness of the regulation is confirmed in Figure 17 which shows the output voltage versus duty cycle D defined as the ratio of the turn-on time T_1 of a transistor to the switching period T_S. A wide range of the output voltage is achievable with an acceptable efficiency deterioration at low values of the duty cycle.



(**a**) (**b**)

Figure 17. (**a**) Output voltage U_{out} of SCVD and (**b**) its efficiency in DCM mode as a function of duty cycle $D = T_1/T_S$. U_{in} = 200 V, f_s = 134.4 kHz, P_{out} = 200 W, t_M = 50 ns. Switching pattern P3.

7. Conclusions

In this paper, the concepts of control for a resonant switched-capacitor voltage doubler are presented. They allow the use of the SCVD converter as a fully functional DC–DC converter with output voltage regulation and very high efficiency.

A classic SCVM operates in the ZCS mode, in which switching power losses associated with C_{OSS} of the transistors are significant. The application of GaN switches makes it possible to operate with a high frequency while maintaining high efficiency. However, the efficiency can be significantly improved by the proposed switching patterns of the converter, where the reverse conduction occurs to achieve zero-voltage turn-on of the transistors. The maximum efficiency that was measured in the demonstrated setup exceeds 99.2%. The heat generation in the transistors is reduced significantly as well. In the switching pattern dedicated to maximum efficiency, an output voltage adjustment is possible. In another switching pattern (P3) proposed in this paper, the SCVD converter achieves a very high output voltage regulation range. The developed model of losses matches the experimental results and can be used in the design process. In addition, the results can be applied in other topologies of the SC converters.

The switching pattern P2 allows for a significant improvement in the efficiency of the SCVD by C_{OSS} loss reduction. To accomplish that, very fast switching is required because the cycle sequence: turn-off/dead-time/turn-on should occur on the falling slope of the resonant current, taking only a small part of the oscillation time. The SCVD is a switched-capacitor converter with low resonant inductance, therefore the oscillation time is very short. Three types of switches (superjunction MOSFET, GaN, and SiC) as a prospective adequate solution for high-efficiency operation of the SCVD. Taking into consideration the features of GaN switches, the experimental tests have been performed with the use of GaN GIT switches. The switching pattern P3 allows for easy implementation for overcurrent limitation of the start-up of the converter, and pattern P4 can be used in the bi-directional operation of the synchronous SCVD. Various patterns can be also combined in the cascaded high-voltage-gain system composed of several SCVDs.

Author Contributions: Conceptualization, R.S.; methodology, R.S., Z.W., A.M., A.S. and A.P.; software, R.S., Z.W., A.P., and A.S.; validation, R.S., and Z.W.; formal analysis, R.S., Z.W.; investigation, R.S., Z.W., A.M., A.S. and A.P.; resources, R.S.; data curation, R.S., Z.W., A.M., and A.S.; writing—original draft preparation, R.S., and Z.W.; writing—review and editing; visualization, R.S. and Z.W.; supervision, R.S. and Z.W.; project administration, R.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

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SiC-Based Bidirectional Multilevel High-Voltage Gain Switched-Capacitor Resonant Converter with Improved Efficiency

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Received: 2 April 2020; Accepted: 9 May 2020; Published: 13 May 2020

Abstract: This paper presents the research results of the bidirectional multilevel resonant switched capacitor converter (MRSCC). The converter can achieve a high voltage ratio in multilevel topology, which limits the voltage stress on switches and is able to operate with high power efficiency. The converter can be applied as an interconnector between DC voltage systems used for various applications. This paper presents a method that significantly improves the efficiency of the MSRCC through topology modification. Furthermore, the feasibility of the converter was demonstrated with the use of SiC and Si MOSFET switches, together with suitable passive components. It was demonstrated that the proposed modification of the topology makes the converter very efficient in SiC-based ones and can significantly improve the efficiency of Si MOSFET converters. The series of test results of the SiC-based converter is a novel aspect presented in this paper and shows promising achievements of efficiency. The results were obtained from the laboratory setup of 5 kW and 0.5/2 kV MRSCC. To demonstrate the bidirectional operation of the converter, a back-to-back setup (0.5/2/0.5 kV) was used. It also demonstrates that such a high-voltage gain converter can be accurately tested with the use of laboratory equipment with a typical voltage range.

Keywords: bidirectional converter; multilevel converter; resonant converter; SiC MOSFET; high-voltage converter; switched capacitor converter

1. Introduction

The multilevel topology of the converter is favorable for high-voltage circuits due to the reduction of voltage stress on switches. Aside from typical multilevel converters, such as the flying capacitor, neutral point clamped, and cascade bridges, various concepts of switched capacitor-based converters have been proposed recently. The switched capacitor (SC) technique is suitable for high-voltage gain converters and can be effectively used in power converters, which was proven in [1,2]. On the basis of the SC technique, such multilevel topologies include MRSCC (multilevel mesonant switched capacitor converter) [3–5], modular capacitor clamped [6,7], resonant Ladder [8], MMCCC (multilevel modular capacitor clamped converter), 6X [9], converter with coupled inductors in various levels [10], and converters presented in [11–16], where the topologies include a similar concept to MRSCC.

Another important quality of a power electronic converter is its bidirectional operation capability. It is required in a vast range of applications, which incorporates battery management. The analyzed MRSCC is made up of a basic SC structure, which makes it possible to transfer energy in both directions, similar to the converters presented in [3–5,13–17].

The four-level MRSCC converter analyzed in this study (Figure 1a) is a very favorable solution when compared to well-established topologies. It comprises features of a bidirectional and multilevel

topology. In MRSCC, voltage stress on the switches is equal to the voltage of a single cell; therefore, the benefit of switch voltage stress reduction is achieved. In comparison to the other concepts of SC converters, such as SCVMs (switched capacitor voltage multipliers) presented in [18,19], MRSCC is a multilevel concept that can be more favorable for high-voltage applications. Voltage stresses on some switches of SCVMs can reach the output voltage (the highest value). Due to the high voltage gain, low stress on switches, and bidirectional conversion ability, MRSCC can be a beneficial solution for the interconnection between DC voltage systems. Depending on applications, numerous DC voltage systems are often used nowadays [20], and the required DC voltage reaches 1500 V [17]. The microgrid connection is another prospective application of such a converter as well. Furthermore, in MRSCC, the energy is transferred via capacitors, which makes it possible to reduce the weight of the converter in comparison to solutions based on inductive components. In some applications, a low weight can be an important feature due to the requirements related to the assembling system components.

The basic concepts of three-level and four-level MRSCCs are presented in [3], in which a detailed analysis of losses and selection of inductance can be found. In [4], the four-level SC converter with loads connected asymmetrically was analyzed. In [5], the first harmonic approximation analysis and basic experimental results of four-level 1.2 kV MRSCC based on SiC are presented. In [13], as well as [14], the basic structure of a multilevel SC converter is used in cascaded systems. However, the problems of topology modification and efficiency improvement in ZVS conditions were not investigated.

Recently, a lot of research has focused on the elimination or limitation of C_{oss} losses in different types of converters. However, very few of them present a solution for switched capacitor converters and especially multilevel ones. In [15,17], the C_{oss} losses were identified as an important factor in the power efficiency limitation of the voltage doubler based on the MRSCC concept. The solution for C_{oss} elimination is reported in [15] for a MOSFET converter as well as in [16] for GaN and in [17] for SiC. Therefore, the methods for achieving ZVS (zero-voltage switching) in such a converter are demonstrated in those papers, but all of them are similar and limited to two-level (voltage doubler) MRSCC. The methods rely on the application of the special control pattern to switches in higher and lower voltage levels, for additional energy delivery to the resonant inductor before dead time intervals. The energy stored in the resonant inductor is then utilized for the C_{oss} voltage transition in dead time intervals. As reported in [16], this technique is problematic in light load operations, due to significant switching frequency increases. Special control with cycle skipping is required for light load operation, which itself brings some power loss and is problematic due to parasitic oscillations [21]. To mitigate this challenge, the authors in [16,17,21] proposed to move the resonant inductor to the DC side of the converter. It eliminates most disadvantages; however, it still cannot be applied to converters with a number of levels higher than 2, since in higher levels of the converter, the resonant operation could not be achieved. In this paper, the solution with an additional small inductor further referenced as the commutation supporting inductor (L_{SC}) and small (commutation) capacitors connected across resonant branches is presented. This solution is free from the abovementioned limitations. It operates well at any load level, including an idle state, and can be applied for a converter with any number of voltage levels; however, it requires additional components.

C_{oss} losses have an important impact on the efficiency of a high-frequency converter. A model of this type of loss in an SiC-based converter is analyzed in detail in [22]. In the case of SC converters, which contain large numbers of switches, such as SCVM [18,19], and do not operate in ZVS mode, C_{oss} losses can become significant. The method for ZVS operation in SC converters with resonant inductors is an important research subject. It can be introduced to other SC topologies than MRSCC and the results of ZVS operation in an SiC-based converter presented in this paper can have even more general importance. In [23–28], SC converters with ZVS operation are presented. The presented approach for the ZVS problem solution is similar there and the converters use resonant inductors, which makes it possible to apply a phase shift switching or an operation above the resonant frequency for a charge reduction of the switch before it is turned on. The C_{oss} voltage transition method and ZVS operation is accomplished in this paper for four-level MRSCC and can be extended to a higher

number of voltage levels, which is the main difference from previously presented solutions. Therefore, this paper confirms the merit of the MRSCC topology with introduced improvements. Furthermore, numerous new experimental results of Si and SiC MOSFETs based on bidirectional four-level MRSCC, such as the efficiency, voltage ratio measurements, and resonant circuit operation, are presented and compared in this paper. In essence, the main goal of this paper was to verify the concept of the topology modification towards efficiency improvement of four-level SiC-based and Si-based MRSCC converters with the major contributions of this paper being as follows:

- A presentation of a modification of the MRSCC topology to achieve ZVS with no restrictions in terms of the number of voltage levels. A significant increase of the efficiency and significant decrease of idle power losses are achieved in comparison to the base topology by (almost) elimination of the C_{oss} losses.
- A comparison the SiC-based and Si-based MRSCC performance based on experimental results. It is demonstrated that the proposed method makes it possible to achieve a performance of the Si MOSFET design close to the outstanding SiC-based one.
- The demonstration of MRSCC operation in a boost mode as well as in buck mode. It is accomplished in a test setup with two cascaded converters with a common high-voltage DC link (2 kV in the tested case). However, the load and the output voltage sensors operate on a low voltage (<1 kV), which is appropriate for precise voltage registration and efficiency measurement, and MRSCC is a bi-directional converter and such concept of a test setup configuration is justified. A similar approach can be found in [15], which presents the regenerative test setup, composed of two resonant SC converters for efficiency. A single DC-DC converter with a high voltage ratio can be used in photovoltaic systems [17] with a common DC link or DC grid on the output. The application of such converters as an interconnector between DC grids is their prospective application as well, especially as SiC-based solutions.

The paper is organized as follows. In Section 2, the basics of operation of the MRSCC and simulation results are presented. In Section 3, the problem of C_{oss} loss is addressed and a modification of base topology is proposed. Section 4 includes a description of the back-to-back experimental setup and experimental results of MRSCC operation.

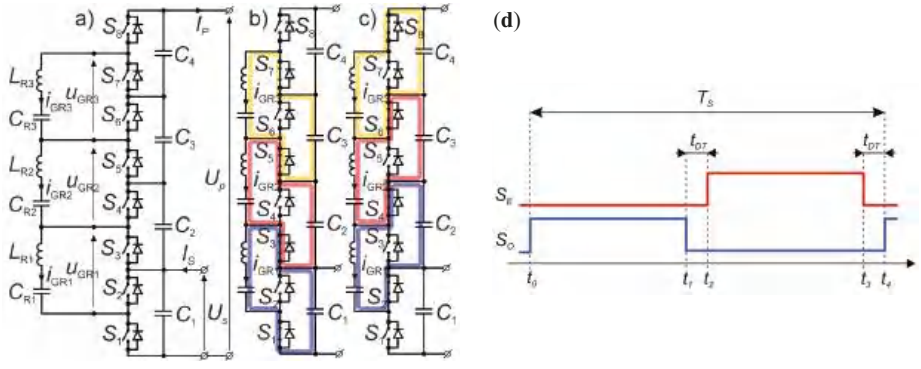


Figure 1. The bidirectional four-level switched capacitor resonant DC-DC converter (**a**) the concept, (**b**,**c**) the modes of operation, (**d**) the control signals of the switches; S_E—control signal of the even switches; S_O—control signal of the even switches.

2. Principle of Operation of the Multilevel Resonant Switched Capacitor Converter (MRSCC)

Figure 1 presents the topology of the MRSCC. The principle of operation assumes charging and discharging of switched capacitors (C_R) in resonant circuits and energy exchange between DC capacitors C_1–C_4. Each voltage level contains two transistors in HB (half bridge) configuration, with

appropriate driving circuits. All the resonant branches $C_{R1}L_{R1}$-$C_{R3}L_{R3}$ are tuned to the same resonant frequency. The control of the converter, in the general concept, requires alternating the switching of odd and even switches with a 50% duty ratio with the resonant frequency of the branches $C_{R1}L_{R1}$-$C_{R3}L_{R3}$. As a result, each resonant branch ($C_{Rk}L_{Rk}$) is switched between two adjacent voltage level capacitors C_k and $C_{(k+1)}$ (Figure 1b,c). The control signals are presented in Figure 1d.

Voltages of the capacitors C_1-C_4 of MRSCC are nearly equalized. As a result, the voltage gain of the idealized converter in the boost-type interpretation is as follows:

$$k_{UTE} = \frac{U_p}{U_s} = n, \tag{1}$$

where U_p-higher side voltage value, U_s-lower side voltage value, and n- number of levels.

During the t_0-t_1 and t_2–t_3 time intervals, the current oscillations occur in resonant branches. During the dead time intervals, the oscillations are stopped, and in the idealized and tuned circuit, the currents of resonant branches are zero during dead time. The current peak stresses of the resonant branches are given by the following relationship:

$$\begin{cases} I_{GR(k)DTmax} = \frac{\pi}{G_{DT}}(n-k)I_P \\ I_S = nI_P \end{cases} \tag{2}$$

where $k = 1,\ 2,\ 3,\ 4, \ldots, (n-1)$; $G_{DT} = 1 - \frac{2t_{DT}}{T_s} \leq 1$; and I_p, I_s-current value of lower and higher voltage side.

The current stresses of the switches are given by:

$$I_{S(2k)RMS}(t) = I_{S(2k-1)RMS}(t) = \frac{\pi}{2}\frac{1}{\sqrt{G_{DT}}}I_p, \tag{3}$$

$$I_{S2RMS}(t) = I_{S1RMS}(t) = \frac{\pi}{2}\frac{1}{\sqrt{G_{DT}}}(n-1)I_p, \tag{4}$$

where $k = 2, 3, 4, \ldots, n$, $\varphi = \varphi_{k-1} = \varphi_k$.

From Equations (3) and (4), it follows that the current stress of switches S1 and S2 is greater than others for $n > 2$. The higher the number of n, the bigger the difference between the current stresses of switches observed in the converter, which is an important conclusion from the switches' selection standpoint. The dead time increases the current stresses of the resonant branches and switches. It corresponds with the G_{DT} coefficient variation in Equations (2)–(4). The example simulation waveforms of the 5 kW and 500 V/2 kV MRSCC are presented in Figures 2 and 3. The results were carried out from two different models and software tools. In the waveforms presented in Figure 2, during the dead time intervals, the oscillations are halted and the current of the resonant branches equals zero. In this simulation, which was performed in MATLAB/SIMULINK software, all parasitic capacitances of the switches were omitted. In a real circuit (Figure 7a), or precise behavioral simulation model designed for PSpice (Figure 3), the distortions can be observed in the dead time intervals. The distortions are caused by an interaction of resonant branches and C_{oss} capacitances of the switches as can be anticipated by comparing the simulation results. Therefore, the distortions in dead time intervals are natural for this topology and are not caused by an improper design of the real converter. For PSpice simulation, the precise models of power transistors provided by the manufactures were used. The simulations parameters are consistent with the experimental setup (Tables 1 and 2) described in Section 4.

Table 1. Parameters for SiC and Si designs for the base configuration.

Number of Voltage Levels	***n***	**4**
Switching frequency	f_s	285 kHz
Lower side nominal voltage	V_S	500 V
Higher side nominal voltage	V_P	2000V
Design max power	P_N	5 kW
Capacitance of levels capacitors	$C_4 = C_3 = C_2 = C_1 = 4.7$ µF	
	$C_{1a} = C_{1b} = = 0.47$ µF	
Resonant branches	$L_{R3} = 3.0$ µH $L_{R2} = 2.0$ µH $L_{R1} = 0.9$ µH	
	$C_{R3} = 100$ nF $C_{R2} = 147$ nF $C_{R1} = 320$ nF	
Commutation branches	$C_{C3} = 22$ nF $C_{C2} = 22$ nF $C_{C1} = 47$ nF	
	$R_{C3} = 1\ \Omega$ $R_{C2} = 1\ \Omega$ $R_{C1} = 0.5\ \Omega$	
Switching supporting inductor	$L_{SC} = 54$ µH ETD29	

Table 2. The measured idle power of a single HB for different transistors used for the SiC and Si setup.

No	**Part**			**Measurement**		
	Type	V_{DS} **(V)**	R_{DSon} **(mΩ)**	U_{DS} **(V)**	f **(kHz)**	ΔP_{CO} **(W)**
1,2	SCT3030AL	650	30	500	285	42
3–8	C3M012090D	900	120			15
1,2	SiHG33N65EF	650	95			93
3–8	SiHG21N65EF	650	150			60

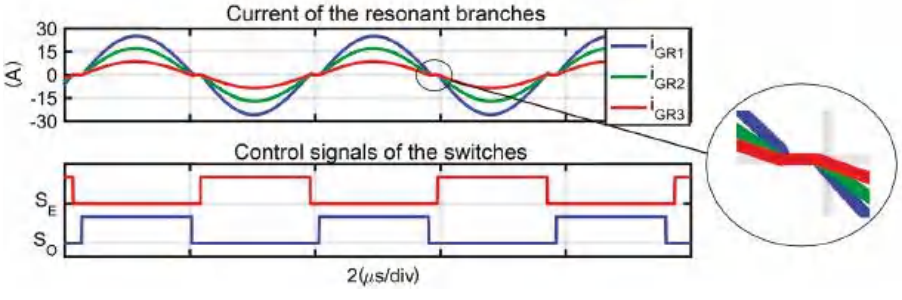


Figure 2. Simulation result of the 5 kW 500V/2 kV MRSCC (Multilevel Resonant Switched Capacitor Converter) in the base configuration in MATLAB/Simulink without C_{oss}.

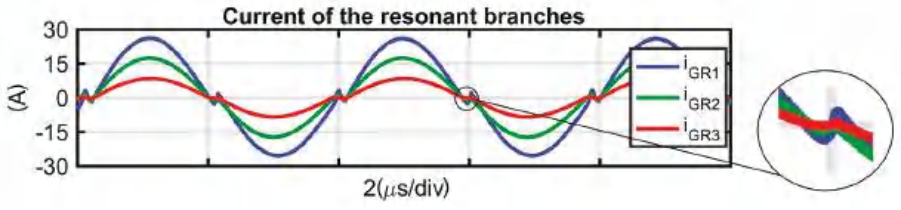


Figure 3. Simulation result of the 5 kW 500 V/2 kV MRSCC in the base configuration in PSpice (plotted in MATLAB) with C_{oss} and other parasitics.

The transition between the boost and buck mode of operation of MRSCC does not require any special control. It depends on the relationships between voltages U_p/U_S. The resonant legs should be tuned to achieve the best possible performance of the converter, and only this case is analyzed in the paper. In [5], the analysis for the general case can be found. For a cost reduction, selected switches can be replaced by diodes, but only unidirectional operation is possible in this case. For example, as presented in the literature [8], a diode-based ladder resonant switched capacitor converter operates in boost mode only.

3. C_{oss} Losses and Its Reduction by Application of the Commutation Supporting Inductor

The converter operates in ZCS (zero current switch) conditions, but switching losses still occur due to charging and discharging of the output capacitances of the switches. The converter consists of a relatively large number of switches; thus, the switching losses may seriously deteriorate its efficiency, especially under the light load operation. C_{oss} losses are also the subject of the research presented in [15,16], where it is eliminated by the special control of the switches. However, a solution for a converter composed of the number of voltage levels above 2 is not presented.

C_{oss} losses are associated with the energy dispersion from C_{oss} by the switch that is turned on as well as the power losses during C_{oss} charging caused by the current flow and commutation in the corresponding switch. In an MOSFET switch, the capacitance C_{oss} is strongly nonlinear and the charge transferred to C_{oss} is (from the DC source U_{HB}, during the lower switch turn on in a half-bridge operating with ZCS):

$$Q_{oss}(U_{HB}) = \int_0^{U_{HB}} C_{oss\_low}(u_{DS\_low})\, du_{DS\_low}. \tag{5}$$

Typically, both switches in HB are the same type and have the same parameters. Therefore, the high side switch will result in the same charge transfer from a DC source. As a result, the charge Q_{oss} is transferred twice in the switching period. Thus, the average value of the C_{oss} losses in a half-bridge of the converter is:

$$\Delta P_{HB\_loss} = 2f_s U_{HB} Q_{oss}(U_{HB}) = 2f_s U_{HB} \int_0^{U_{HB}} C_{oss\_low}(u_{DS\_low})\, du_{DS\_low}. \tag{6}$$

If C_{oss} capacitances are charged to the certain voltage value in the dead time by the external circuit, the start value in the integral in Equation (6) is a nonzero value. Therefore, the losses (Equation (6)) are lower in such a case, and can even be zero (in idealized analysis). The detailed analysis of C_{oss}-related energies and losses in HB can found in [29,30]. The MRSCC converter consists of n number of HBs composed with two various types of switches, resulting from their current stresses described by Equations (3) and (4). The total C_{oss} power loss of the converter is the sum of the C_{oss} losses of all HBs.

For the analysis and optimization of losses in MOSFET power transistors in MRSCC, the following FOM (figure of merit) [31] can be used:

$$F_M = r_{DSon} Q_{oss}, \tag{7}$$

where r_{DSon}-turn on resistance of MOSFET, Q_{oss}-charge calculated as in (5) with $U_{HB} = U_S$.

Based on Equations (3) and (4), the conduction loss in power transistors of the lower HB (S1, S2) and all the higher HBs (S3-S8) can be the following:

$$\Delta P_{Rds\_L} = I_P^2 \frac{\pi^2}{2} r_{DSon\_L}(n-1)^2, \tag{8}$$

$$\Delta P_{Rds\_H} = I_P^2 \frac{\pi^2}{2} r_{DSon\_H}(n-1), \tag{9}$$

where r_{DSon_L}-on-state resistance of the S1-S2 switches, r_{DSon_H}-on-state resistance of the S3–S8 switches.

Utilizing Equations (7) and (6), the C_{oss} loss in power transistors of the lower HB (S1, S2) ΔP_{Coss_L} and all the higher HBs (S3–S8) ΔP_{Coss_H} can be found:

$$\Delta P_{Coss\_L} = 2 f_s F_{ML} U_S \frac{1}{r_{DSon\_L}}, \tag{10}$$

$$\Delta P_{Coss\_H} = 2 f_s F_{MH} U_S (n-1) \frac{1}{r_{DSon\_H}}, \tag{11}$$

where r_{DSon_L}—on resistance of the S1–S2, r_{DSon_H}—on resistance of the S3–S8, f_s—switching frequency, F_{ML}—figure of merit (7) for S1 and S2, F_{MH}—figure of merit (7) for S3–S8.

The total power loss for a given group of switches is the sum of the conduction loss and C_{oss}-related loss. The selection of transistors with higher on-state resistance leads to a higher conduction loss. However, the C_{oss} loss is lower in such a case, if the figure of merit (Equation (7)) is considered constant. Using the above Equations (8)–(11), it is possible to find the optimal value of r_{DSon_L} and r_{DSon_L} for which the total power loss of a transistor is minimal for a given figure of merit. Obviously, the selection of transistors is a discrete problem since only several types of devices with specific parameters are manufactured. The presented solution is continuous, but in spite of this fact, it can be used for the selection of the transistors nearest to the calculated optimal parameters. The optimal on-state resistances of transistors are given by the following relationship:

$$r_{DSon\_L\_opt} = \frac{2nU_S\sqrt{U_N f_s F_{ML}}}{\pi P_S (n-1)}, \tag{12}$$

$$r_{DSon\_H\_opt} = \frac{2nU_S\sqrt{U_N f_s F_{MH}}}{\pi P_S}, \tag{13}$$

where $r_{DSon\_L\_opt}$—optimal on resistance of the S1–S2, $r_{DSon\_H\_opt}$—optimal on resistance of the S3–S8, f_s—switching frequency, F_{ML}—figure of merit (7) for S1–S2, F_{MH}—figure of merit (7) for S3–S8, P_S—power of lower voltage side, for which value the minimum losses should occur.

The above Equations (8)–(13) were evaluated for the real setup parameters, which are presented in Section 4, especially in Tables 1 and 2. The figure of merit was calculated based on Equations (5) and (7) and the C_{oss} curves from the data sheets for the two transistors selected in the initial design step: SCT3030AL as S1, S2; F_{ML} = 4 nVs and C3M012090D as S3–S8; F_{MH} = 5.9 nVs. The results are presented in Figure 4.

As can be observed in Figure 4, the initially selected transistors are not optimal. However, there is no significant improvement possible since it is about 20% of the total power loss in the switches. A significant improvement of efficiency may be achieved by the introduction of further modifications as described in Section 4, which nearly eliminates the total C_{oss} power loss. In case of the initially selected transistors, the C_{oss} loss accounts for nearly 87% of the total loss in the switches, and in the case of hypothetical optimal switches, 52%. After the introduced modification of the topology, only conduction losses are relevant. The conduction losses are lower for the initially selected transistors (SCT3030AL, C3M012090D) than in the case of any hypothetical optimal ones. Therefore, the initially

selected transistors were accepted as the final selection. After the modification, the optimization problem must be defined in another way since there is no longer a tradeoff needed between C_{oss} and the on-state resistance.

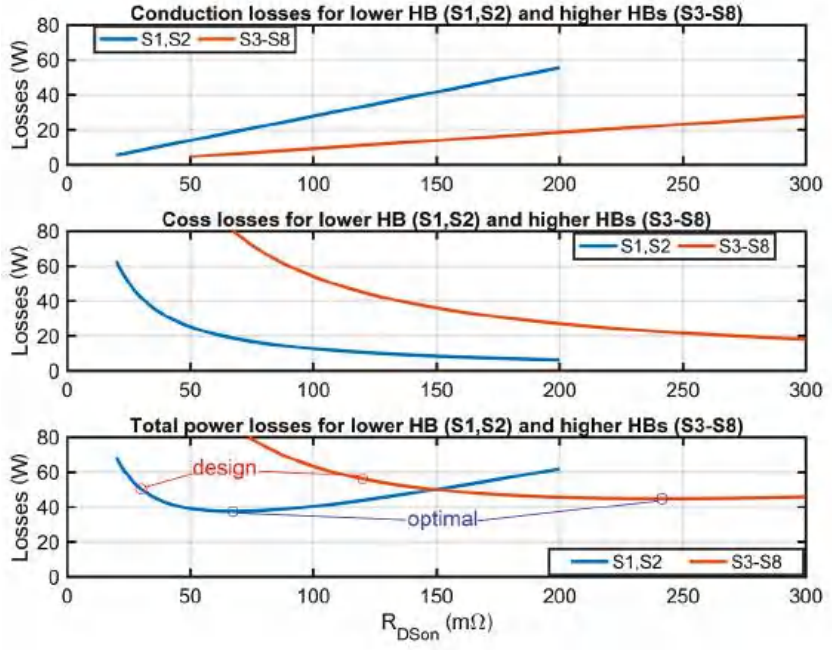


Figure 4. Results of the optimization of losses in power switches in terms of r_{DSon} selection.

3.1. Concept of MRSCC with Commutation Inductor

To reduce the idle power losses, the topology modification is proposed based on the application of the additional commutation inductor L_{SC}, which brings a significant reduction to the switching losses. The proposed concept and commutation sequence from odd to even switches is presented in Figure 5a–c. The inductor L_{SC} is connected between the output of the lowest HB and the output of the voltage divider created in the lowest voltage level. Due to the fact that all HBs are switched with a 50% duty ratio, the waveform of the current in L_{SC} is symmetrically triangular with the positive and negative peaks that occur during the commutation. This current charges and discharges the output capacitances of all switches during the commutation, causing ZVS operation.

When all the HBs are turned into *DT* mode (Figure 5b), the output capacitance of all HBs is charged by the current of inductor L_{SC} (HB1 directly, and the rest via C_{Ck} capacitors). The transition is finished after a certain time, which depends on the peak current of the L_{SC} and the values of the output capacitances of the switches. To finish the switching sequence, all the even switches are turned on (Figure 5c). Because the output capacitances of the switches are charged and discharged by an inductor, their switching losses are significantly reduced (in theory it is lossless).

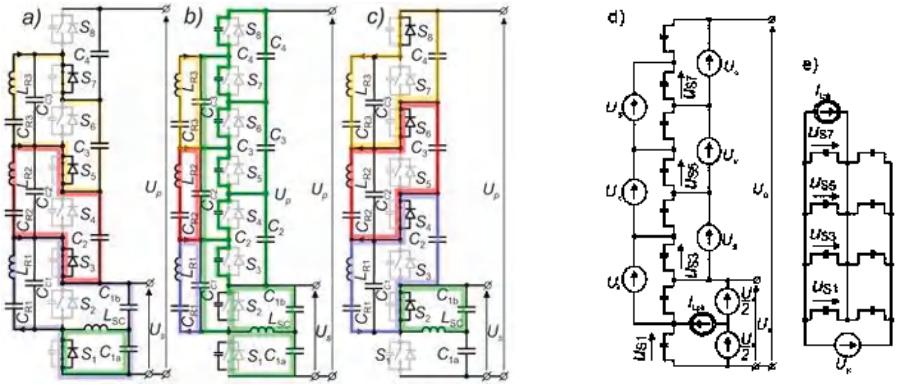
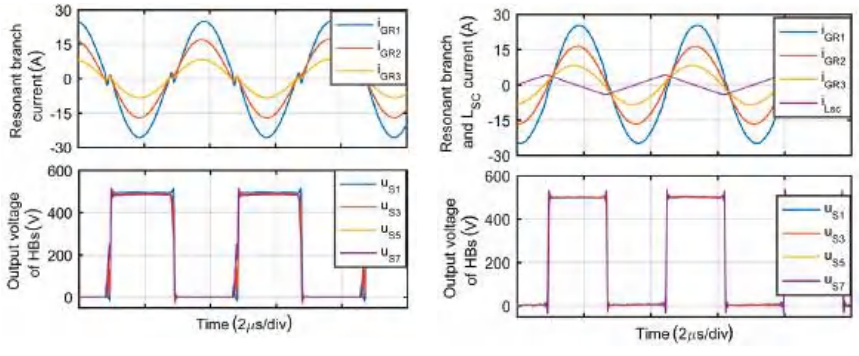


Figure 5. (**a**–**c**) The sequence of modes for commutation from odd to even switches in MRSCC with the commutation capacitors C_{Cn} and the supporting inductor L_{SC}; (**d**) Simplified equivalent circuit for charging the C_{oss} by L_{CS} current during dead time (mode b); (**e**) further simplification.

3.2. Application of Communication Capacitors in MRSCC Branches

The resonant branches contain series inductors and therefore, for very short commutation processes, they can be considered as the current sources. The values of those current sources can be assumed equal to the instantaneous current of the resonant branches at the beginning of the commutation. In the precisely tuned circuit, those values are close to zero, which means that the resonant branches have almost no effect on the commutation process. For this reason, the commutation capacitors (relatively small) are applied to the circuit, in parallel to the resonant branches. The commutation capacitors C_{Ck} can be considered as the voltage sources with the value of U_S (as well as the all C_k capacitors). They allow the output capacitances of higher-level HBs to be charged and discharged by the current of the L_{SC} inductor flow. The inductor L_{SC} can be considered as the current source with a positive (odd to even switches commutation) or negative (even to odd switches commutation) peak value. The equivalent circuit representing such conditions is shown in Figure 5d. The circuit can be further simplified, to the circuit where all C_{oss} are charged in parallel and supplied by one U_S voltage source, as shown in Figure 5e. The application of the commutation capacitors has an additional effect. In the base circuit, during the dead time, the current oscillations in the resonant branches are stopped, thus the resonant frequency of the converter is lower than the resonant frequency of the branches. The commutation capacitors clamp the resonant branches during the dead time, which allows the oscillation to continue. As a result, the resonant frequency of the converter is equal to the resonant frequency of the resonant branches. Furthermore, an additional benefit is the resonant current is a smooth sinusoidal (Figure 6b), while in the base circuit, some distortion (fast oscillation) can be observed in dead time intervals (Figures 4 and 6a). Such distortions reduce the balancing capability of the resonant branches and increase the series-equivalent output resistance of the converter, which will be presented in Section 4. The application of the L_{SC} inductor and C_{Ck} capacitors has no direct influence on the voltage gain of the converter. However, it improves the power efficiency and eliminates distortions of the oscillations, resulting in a reduction of the series-equivalent resistance of the converter.

Idle mode losses depend on the peak value of the current of L_{SC}, which will be demonstrated in Section 4 together with the research results related to the impact of the I_{LSCpk} on the switch voltage during commutation. The overall efficiency of the MRSCC is also affected by the remaining switching losses and conduction losses, which are out of the scope of this paper.



(**a**) (**b**)

Figure 6. Waveforms of HB (Half Bridge) voltages and resonant branches currents for step-up steady-state operation of: (**a**) base MRSCC at 258 kHz, (**b**) modified MRSCC at 285 kHz. Experimental results of SiC-based converter 5 kW load (oscilloscope data exported and to MATLAB and plotted).

3.3. Selection of L_{SC} and C_{Ck} Values

Firstly, the required peak current of the L_{SC} should be determined. According to Figure 5e, the total charge Q_{ossT} that must be provided by the L_{SC} inductor during the dead time equals the sum of the $Q_{oss}(U_s)$ determined for every transistor. The charge must be transferred during the dead time interval t_{DT}, thus the required peak current of L_{SC} is given as:

$$I_{LSCpk} = \frac{1}{t_{DT}} \sum_{m=1}^{2n} Q_{oss(m)}(U_S), \tag{14}$$

where $Q_{oss(m)}(U_S)$—charge determined based on Equation (6) for the m-th transistor for voltage U_S.

The required inductance L_{SC} could be approximated as:

$$L_{SC} = \frac{U_S}{8 f_s I_{LSCpk}}. \tag{15}$$

The values of the C_{Ck} capacitors should be large enough so that the voltage across does not change significantly in the dead time interval, when the I_{LSC} flows through them, charging the C_{oss} of the transistors. The values of the C_{Ck} capacitors are given by:

$$C_{Ck} = \frac{1}{\Delta U_{CC(k)}} \sum_{m=2k+1}^{2n} Q_{oss(m)}(U_S), \tag{16}$$

where $\Delta U_{CC(k)}$—change of voltage across k-th capacitor in the dead time interval.

The selection of the values of the capacitor according to Equation (16) is therefore dependent on the permitted change of the voltage across in the dead time interval ΔU_{CCk} and C_{oss} of the used transistors. Too high ΔU_{CCk} values (too low capacitance of C_{Ck} capacitors) cause inefficient charging and discharging of C_{oss} of higher-level transistors and stimulation of resonance branches by voltage glitches during the dead time intervals. Too low ΔU_{CCk} values (too high capacitances) are unfavorable not only in terms of size and cost but also due to the increased participation of these capacitors in energy transport between level voltages, which cause unwanted inrush currents. From the conducted experimental research, it follows that the values of ΔU_{CCk} in the range of few volts (for SiC-based devices between 10 and 100 nF) bring suspected favorable effects. From Equation (16), it follows that the higher the index of the capacitor, the lower the capacitance demanded. To dampen very fast

oscillation caused by hard switching of C_{Ck} and parasitic inductances, resistors R_{Ck} should be added in series with C_{Ck}. Typically, values in the range 0.1–1 Ω are optimal.

4. Experimental Results

4.1. The laboraTory Setup and Operation of MRSCC

The laboratory setup was designed for performing tests and measurements of a 2 kV four-level MRSCC converter in a comparative manner. To mitigate the problem of high-voltage measurements, the special laboratory setup was designed. Because the topology is bidirectional, twin converters can be connected back-to-back, creating a cascade with the common high-voltage link. The input and output voltage value of the cascade was 500 V, and this allowed for utilization of the low-voltage laboratory equipment.

Figure 7 presents the schematic of the experimental setup. Tables 1 and 2 contain the crucial parameters of the experimental system. Figure 8a presents the picture of the experimental system. The setup consists of two identical converters designed as a PCB module, which contains all the power and auxiliary components. Every voltage level was equipped with two channel gate driver ICs (UCC21520, Texas Instruments, Dallas, USA). The driver incorporates DT logic and a timer, thus only one control signal was sufficient for each voltage level. The fiber wires were used for signal delivery because of the great isolation that they provide. The controller was designed with an FPGA device and provided control for both converters, with eight control signals in total. The control algorithm included simple pattern generation in open loop mode. The resonant branches were designed to achieve a unified voltage ripple across all the resonant capacitors (about 100 $V_{pk\text{-}pk}$), and the same resonant frequency. The resonant branches were composed of the inductors based on ferrite gapped toroid- and FKP1 (WIMA, Mannheim, Germany)-type capacitors.

Figure 6 presents the waveforms of the resonant branch current and the output voltages of every single HB (which in fact are the voltages of the switches with an odd index). The waveforms in Figure 6a were obtained in MRSCC in the base configuration while the waveforms in Figure 6b were measured in the modified MRSCC.

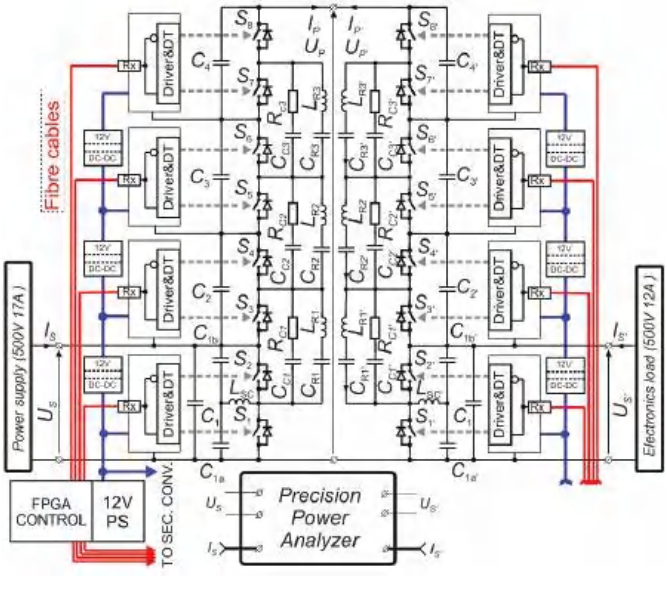


Figure 7. Schematic of the MRSCC laboratory back-to-back setup with modification applied (L_{SC} + $C_{Ck}R_{Ck}$).

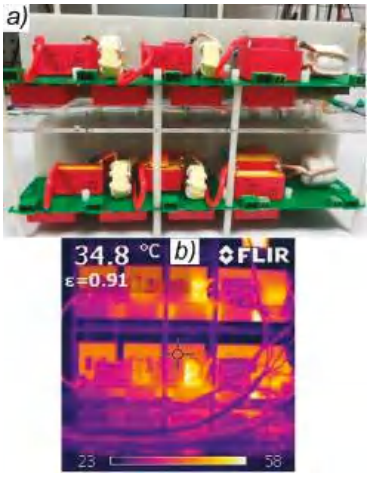


Figure 8. (**a**) Picture of the MRSCC laboratory back-to-back setup (**b**) IR (Infrared) picture under full load (5 kW)—both SiC design.

4.2. Efficiency Measurement Results and Discussion

Figure 9 presents the experimental results related to the efficiency of the MRSCC converter. The measurements presented in Figure 9a,b are related to the single converter but those in Figure 9c are related to the whole cascade. The measurement was performed for different configurations of the converter. The power efficiency of the converter for the base configuration was relatively low (Figure 9c-curves no. 4). The influence of the high idle power losses was significant because a typical peak of the efficiency in the chart efficiency versus power was not observed. Despite this, the efficiency increased with the power load. In the first modification, the $C_{Ck}R_{Ck}$ branches were added but with no inductor L_{SC} (Figure 9c-curves no. 1). The power efficiency was even worse for the low load because the frequency (285 kHz) was higher due to the lack of oscillation breaks in DT intervals. Therefore, the C_{oss} losses were proportionally higher in this case. However, the distortions in dead time intervals were eliminated, which improved of the voltage efficiency. After the application of the commutation supporting inductor L_{SC}, outstanding results were obtained (Figure 9c-curves no. 2). Figure 9a,b presents the detailed results related to the improvement of the efficiency of the converter by a reduction of the C_{oss} losses. As described in Section 3, it was achieved by the application of the supporting inductor (L_{SC}) and operation at the appropriate peak current of L_{SC} during commutations. Figure 9a presents the waveforms of the rising slope of the low side transistor in a half bridge for a different peak value of the L_{SC} current, and Figure 9b presents the respective idle power measurements for the SiC-based design. The results were performed on the experimental setup with SiC switches operating with 285 kHz. The current of L_{SC} should be low but sufficient to effectively perform the transition. A current of L_{SC} that is too high causes hard switching and increases of the losses (Figure 9c). It is remarkable that the idle mode power losses were reduced from approximately 100W in the case when I_{LSCpk} = 0A to nearly 3 W for I_{LSCpk} = 6A.

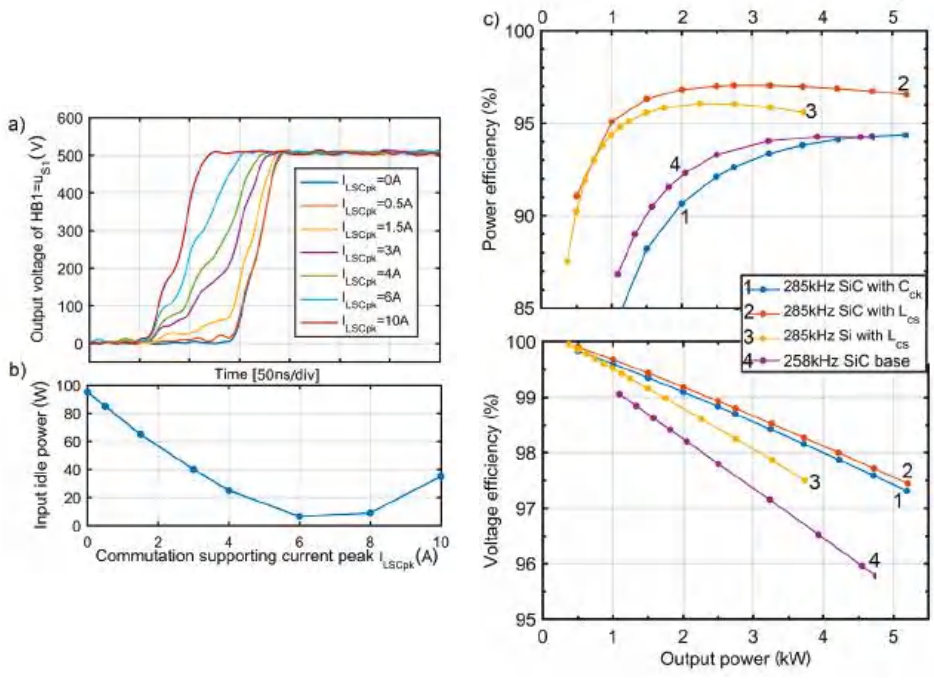


Figure 9. Experimental results: (**a**) waveforms of voltage rising slope HB1. (**b**) idle power losses of the single MRSCC converter-SiC design 285 kHz, (**c**) Power and voltage efficiency characteristics vs. output power for different configurations of the cascaded setup. Yokogawa WT1800 Precision Power Analyzer.

For further references, the power and voltage efficiency curves are presented in Figure 9c-curves no. 3. The parameters of the Si design were insignificantly worse only when compared to outstanding SiC. Higher R_{DSon} losses for Si MOSFETs (Table 1) limited the voltage efficiency and maximum load of the converter. The Si-based design was not able to operate with 285 kHz without the L_{SC} supporting inductor due to huge commutation losses (in theory, 270 W per single converter based on Table 2 and simple calculation). This extreme case shows how effective the proposed modification is. In Table 2, the power consumed by a single non-loaded HB is listed (for different transistors, given frequency, and common DC link voltage). As can be noticed, the power losses are significant, especially for Si devices, even when the types with definitely higher R_{DSon} are compared. The results of the case of the Si-based design L_{SC} inductor and f_s = 285 kHz are presented in Figure 9c-curve no. 3.

A thermography picture presented in Figure 8b shows that the heating of both the converters was nearly the same. It means that the efficiency of a single converter can be properly estimated on the basis of the efficiency results presented in Figure 9c taking into account half of the total losses in the system. Therefore, the peak efficiency of the SiC-based MRSCC with the L_{SC} inductor was approximately equal to 98.5%.

5. Conclusions

In this paper, the research results under the operation of a modified SiC and Si-based MRSCC converters were presented. The MRSCC converter is a relatively novel topology and its improvement was proposed in this paper. The solution assumes the application of a commutation supporting inductor to reduce the switching losses associated with Coss in a converter made up of any number of levels.

The majority of research was performed in the 5 kW laboratory setup, which demonstrates the feasibility of boost and buck operation of the MRSCC. The conversion between the levels of 500 and 2 kV at a switching frequency 285 kHz, with the use of switches with VDS = 900 and VDS = 650 V, was demonstrated. Both the converters were tested simultaneously in the system with a common high voltage DC link. The input and output of the system remained on a low voltage level, which made it possible to perform high-precision efficiency measurements. Furthermore, it is a good example of a low-cost laboratory test setup for high voltage ratio converters.

The major goal of the research focused on a verification of the topology improvement in a four-level bi-directional MRSCC with a 0.5/2 kV voltage conversion ratio with the use of SiC and Si switches. It was accomplished with very promising results and the following conclusions:

- The solution with a commutation supporting inductor in MRSCC is feasible and brings a significant increase of the power efficiency.
- A near-total elimination of the C_{oss} power losses was observed in MRSCC with the commutation supporting inductor and the suitable switching applied.
- An increase of the voltage efficiency was observed as well (lowering of the output-equivalent series resistance). The voltage gain was more stable vs. load and the difference between the theoretical and practical voltage gain was lower than in the case without the proposed improvements.
- The method is very efficient in MRSCC with Si MOSFET as well. Through the application of the commutation supporting inductor, the performance measured in the case of the Si MOSFET MRSCC increased to the level comparable with the converter based on outstanding SiC switches.
- In the SiC-based MRSCC, a high power efficiency of 98.5% was measured.

The efficiency versus power characteristic showed an insignificant decline when the power increased, which is also beneficial. The voltage drop versus power was not significant in the demonstrated design cases of MRSCC. The best solution of 2.5% of the voltage decrease in the 5 kW range was observed. The results of the heat distribution in the converter showed that it can be regular. Overheating of particular cells was not observed.

Author Contributions: Conceptualization, A.K.; methodology, A.K.; software, A.K.; validation, A.K. and R.S.; formal analysis, A.K.; investigation, A.K.; resources, A.K. and R.S.; data curation, A.K.; writing—original draft preparation, A.K. and R.S.; writing—review and editing, A.K., and R.S.; visualization, A.K.; supervision, R.S.; project administration, A.K.; funding acquisition, A.K. and R.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Polish National Science Center, grant number 2016/21/N/ST7/02355.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

DT	Dead Time
FOM	Figure Of Merit
HB	Half Bridge
MRSCC	Multi-level Resonant Switched Capacitor Converter
SC	Switched Capacitor
SCVM	Switched-Capacitor Voltage Multipliers
ZVS	Zero Voltage Switch
ZCS	Zero Current Switch
$C_{oss_{low}}\left(u_{DS_{low}}\right)$	Output capacitance characteristic of a MOSFET
F_M	FOM for MOSFET
$I_{GR(k)DTmax}$	Peak current of *k*-th resonant branch

k_{UTE}	Ideal Voltage Gain
ΔP_{Rds_L}, ΔP_{Rds_H}	Conduction losses for lower HB (S_1, S_2) and for all higher ones (S_3–S_8)
ΔP_{Coss_L}, ΔP_{Coss_H}	losses for lower HB (S_1, S_2) and for all higher ones (S_3–S_8)
P_S	Power of lower voltage side
r_{DSon_L}, r_{DSon_H}	On state resistance for lower switches (S_1, S_2) and for all higher ones (S_3–S_8)
U_p, I_p	Voltage, Current Higher Side
U_S, I_S	Voltage, Current Lower Side
U_{HB}	DC link voltage of a Half Bridge

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DC-DC High-Voltage-Gain Converters with Low Count of Switches and Common Ground

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Received: 1 September 2020; Accepted: 26 October 2020; Published: 29 October 2020

Abstract: This paper presents a new concept and research results of DC-DC high-voltage-gain, high-frequency step-up resonant converters. The proposed topologies are optimized towards minimizing the number of switches and improvements in efficiency. Another relevant advantage of such type of converters is that they have a common input and output negative point. The proposed converters are based on the resonant switched-capacitor voltage multiplier circuit, and that is why they are compared with a classic converter from this family. The included results show the operating principle, possible switching methods with the consideration of their impact on the voltage gain level, as well as the voltage and current ripples. The operating concepts and analytical calculations are confirmed by simulation and experimental results.

Keywords: DC-DC converter; resonant converter; high-voltage-gain converter; switched-capacitor converter; inductiveless converter

1. Introduction

Switched capacitor (SC) circuits can be effectively used in power electronic converters [1]. The significant advantages of SC-based DC-DC power converters are high-voltage-gain, low volume, and quasi inductiveless design. To achieve oscillating currents, low-volume inductors can be used in those converters. They can be designed as air-chokes, or even be based on parasitic inductances of the circuits, resulting in a decrease in the weight of the converter. The design without ferrite chokes allows for the use of the converter in high ambient temperature and/or with a low-volume heat sink.

SC DC-DC converters represent one of the classes of non-isolated step-up converters [2–4]. Nowadays, there are a significant number of applications where isolated DC-DC step-up converters are required [3], due to technical reasons and safety requirements. However, various kinds of non-isolated converters are extensively developed as well. One of the prospective applications for non-isolated DC-DC step-up converters proposed in the literature [5–10] are photovoltaic (PV) systems. High step-up DC-DC converters are often required in grid-connected PV systems to transfer the energy from a low-voltage PV source to the grid [5,6]. In transformerless PV systems [7,8], as well as in microinverters [9], dual-stage DC-AC converters are one of the investigated solutions.

The SC step-up DC-DC converter could be a competitive solution to the switch-mode boost converter. An example of such an idea is presented in Reference [10]. The non-isolated step-up converter can be used not only for a single stage supply, but as a part of a system composed of series-connected converters as well. In such systems, isolation can be implemented in another stage of conversion, e.g., by using a series resonant converter [6,11].

High-voltage-gain in SC-based DC-DC converters can be achieved by applying a suitable topology concept. In References [12–14], an SC voltage multiplier (SCVM) has been presented. It is a series-parallel converter in that a high-voltage-gain can be obtained, as it is proportional to the

number of switching cells. The advantage of an SCVM is its modular topology; however, the number of required transistors is relatively high. Series-parallel SC converters have also been presented in recent publications [15,16]. In Reference [15], a converter with regulated voltage gain has been discussed. This device utilizes three switches, which means that the voltage gain can reach three. Reference [16] has presented a very effective method that allows the switch count in high-gain series-parallel converters to be decreased. However, the converter presented in Reference [16] does not have a common input and output negative point, and the output voltage is asymmetrically divided. In Reference [17], a converter that combines Dickson-based and ladder SC converter concepts has been presented. In the proposed topology, high-voltage-gain is achieved with limited voltage and current stresses on the switches. The Dickson-based SC concept has also been used in the converter presented in Reference [18] that is composed of an SC part and an interleaved boost converter. The converter achieves a very high-voltage-gain with the output voltage regulation and soft switching operation, using four switches and seven diodes. In Reference [19], high-voltage-gain is achieved in a converter with switched-capacitor and switched-inductor networks. A concept of a family of converters composed of a boost stage and switched-capacitor-inductor cells has been presented in Reference [20]. This increases the voltage gain of the converter significantly with favorable voltage stress levels, efficiency, and component count. References [21–24] have demonstrated high-voltage-gain multilevel converters based on typical multilevel converter concepts. When we take into consideration the number of the utilized components and the reached voltage gain, the multilevel SC converters can be more beneficial in comparison to the SCVMs. The converter described in Reference [21] is based on a modified classic multilevel SC topology; however, it is composed of a significant number of switches. In Reference [22], an improvement in the operation of the multilevel resonant SC converter (MRSCC) has been proposed. The MRSCC makes it possible to operate with high-voltage-gain and limited voltage stress on the switches with the ability of bi-directional energy transfer. In Reference [23], a multilevel structure has been achieved in the converter with two switches and circuits composed of diodes and capacitors. The converter can operate with zero voltage switching (ZVS) and voltage regulation. In Reference [24], a DC-DC bidirectional SC converter has been presented that improves the total device power ratings in comparison to the multilevel modular capacitor clamped converter (MMCCC) and well-established flying-capacitor converters.

One of the major issues of the SC converters is a large number of switches used in the topology. This problem can be solved by the concepts of cascaded or series systems composed of SC units [25,26] or by new concepts of topologies [16,27,28]. In the concept for the switch count reduction presented in Reference [26], a high-power converter has been analyzed in a multi-section topology. The converter is composed of the typical SCVM sections separated by LC filters. According to this concept, a significant reduction in the number of switches has been achieved. However, an increased number of passive components are utilized as LC filters between the sections in the multi-section converters [26]. The problem of the switch count reduction in an SCVM converter has been analyzed in Reference [29], where the charging of the switched capacitors is controlled by a single switch. For high-voltage-gain, the system is significantly simplified. The design of such a cost-effective converter should assume a much higher current stress of the switch that controls the charging of the switched capacitors.

The converters proposed in this paper are optimized towards a low count of transistors (and they are called Low Count of Transistors Switched Capacitor Voltage Multipliers—LCSCVMs). The basic concept of the topology and operation assumes that every second cell has no transistors whatsoever, but the utilization of all the switched capacitors remains possible, and the effect of voltage gain is comparable to that of the multipliers (SCVMs) presented in Reference [13,14]. Furthermore, the optimized concept is introduced into the cost-effective topology presented in Reference [29], which gives a new relevant converter. Taking into consideration the count of switches, SC converters, such as the SCVM [20], may not be in competition with the LLC converters or other established topologies. However, the concepts proposed in this paper demonstrate a development of the SC topologies towards a significant decrease in the number of switches. One of the converters presented in this paper requires

only three switches, which is below the number of transistors used in a full-bridge LLC converter. Other advantages of the SC converters, such as: high gain, high power density and low weight (no transformer or bulky choke), fast dynamic response [3], ability for operation in high temperature (no ferrites), and simple control, can make them an alternative solution for existing topologies intended for high-voltage-gain non-isolated DC-DC conversion. SC-based topologies can be suitable for the miniaturization of converters that can be applied in emerging power electronics applications, such as wearable technology.

For the operational parameters of an SC converter, the switching strategy applied for a given topology can be essential, which has been demonstrated in Reference [14]. For the optimization purposes analyzed in this paper, various switching strategies are proposed for the new topologies. This makes it possible to determine the advantages of the presented topologies, also taking into consideration a variety of qualities, other than the count of switches.

The proposed converters are nearly pure switched-capacitor circuits, where a vast majority of energy is transferred via capacitors rather than inductors. The resonant inductors are used to achieve oscillatory currents. The inductors can be designed as air chokes, which reduces the weight of the converters and allows them to work in higher temperatures. However, another trend in the development of very high-voltage-gain converters can be observed in the literature. The concept presented in Reference [30] is based on coupled inductor (CI) converters that achieve good parameters such as voltage ratio, efficiency, low number of switches, or low voltage stress on switches. Notwithstanding, such converters use chokes and, therefore, differ from the presented SC-based concept regarding admissible ambient temperature of operation, weight, and volume. The design comparison can be analyzed in particular case studies.

In this paper, the qualities introduced by the new topologies will be compared with those of a classic SCVM and of other converters discussed in recently published papers.

The paper is organized as follows. Section 2 demonstrates two proposed topologies of the SC converters and presents the principles of their operation. For both converters, switching strategies are analyzed. The discussion is supported by the results of computer simulations of their operation in five cases of switching strategies. Moreover, with the use of the simulation results, a number of parameters of the converters operating under various switching strategies are compared as well. Section 3 contains efficiency models of the proposed converters that demonstrate their efficiency as a function of their parameters. Section 4 presents the laboratory setup and the experimental verification of its operation, including the efficiency of the converter. All the research results are concluded in Section 5.

2. Operating Principle of the Converters

The operating principle of the converters in Figure 1 is similar to that of other SC multipliers, and is based on the charging and discharging of the switched capacitors in consecutive stages (time intervals). However, various switching strategies can be proposed for the new converters, which creates differences in their parameters. In the SCVM, as well as in the case of the converters proposed in this paper, the switched capacitors are recharging in resonant circuits composed of a switched capacitor and a low-volume resonant inductor. This creates ZCS (zero current switching) operating conditions, and limits the current flow between the capacitors and the voltage source connected in parallel.

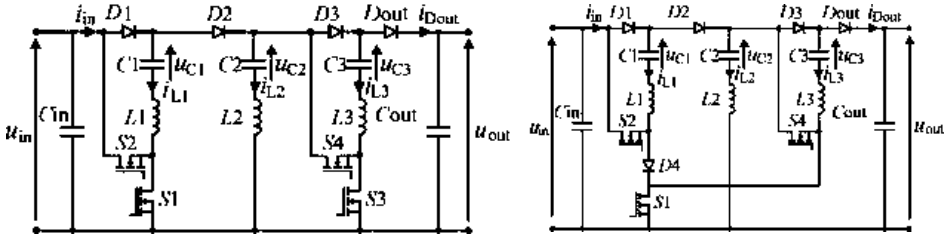


Figure 1. Proposed new resonant converters with low count of switches and common input/output negative point: (**a**) LCSCVMa, (**b**) LCSCVMb.

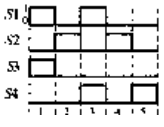
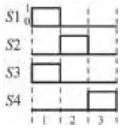
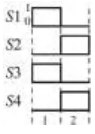
The main difference between the topology of the proposed converters and the classic SCVMs is that in the former case, an LC circuit that is not a part of a traditional cell is used, usually consisting of a diode and two transistors [13]. This circuit is charged using the energy of the input source and the electric charge of the switched capacitor that is the nearest to the input source. Then, the middle capacitor is discharged to the output capacitor or to the switched capacitor nearer to the output. Its function is to increase the output voltage and the amount of converted power, simultaneously maintaining the same value of the input voltage and the same cell number as in the case of a typical SCVM.

The LCSCVMa (Figure 1a) offers a larger number of strategies than the LCSCVMb (Figure 1b), due to the possibility of independent control of switches S_1 and S_3. The basic switching strategies can be composed of 2, 3, or 5 stages.

2.1. Switching Strategy Concepts for the LCSCVMa

Table 1 presents three switching strategies for the LCSCVMa, and Figures 2–5 depict the corresponding simulation waveforms.

Table 1. Switching strategy concepts of the LCSCVMa. States of switches S_1–S_4.

The Concept for Switching Strategy of LCSCVMa		Description—Stages of Charge Transfer in the Converter
Strategy C1		1.Simultaneous charging of all the switched capacitors 2. Discharging of the capacitor that is the nearest to the source (C_1) to the internal branch (C_2) 3. Charging C_1, and discharging C_2 and the next SC capacitor (C_3) to the output 4. Discharging C_1 to the internal branch (as in 2) 5. Discharging C_2 and C_3 to the output
Strategy C2		1. Simultaneous charging of all the switched capacitors 2. Discharging C_1 to the internal branch (C_2) 3. Discharging C_2 and C_3 to the output
Strategy C3		1. Simultaneous charging of all the switched capacitors (C_1 and C_3) 2. Simultaneous discharging of all the switched capacitors and charging the internal branch capacitor (C_2)

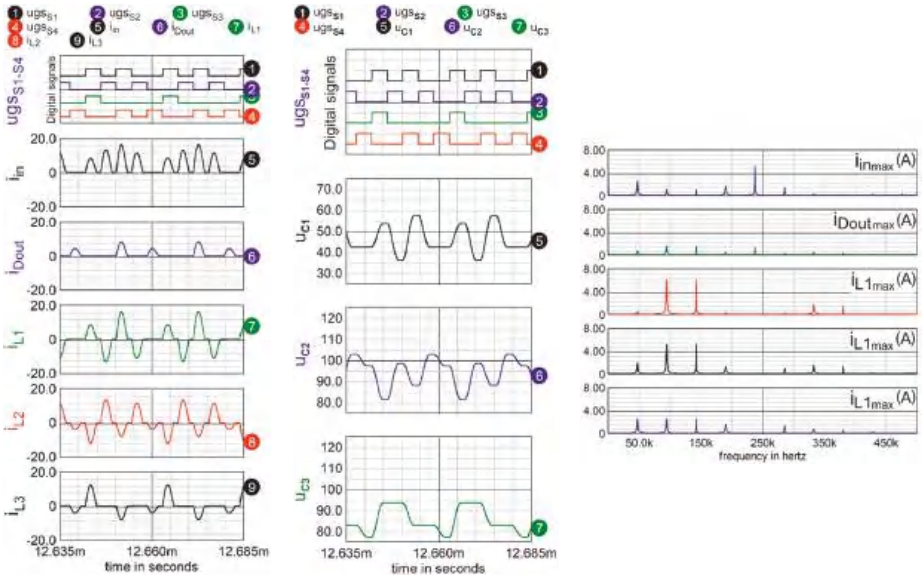
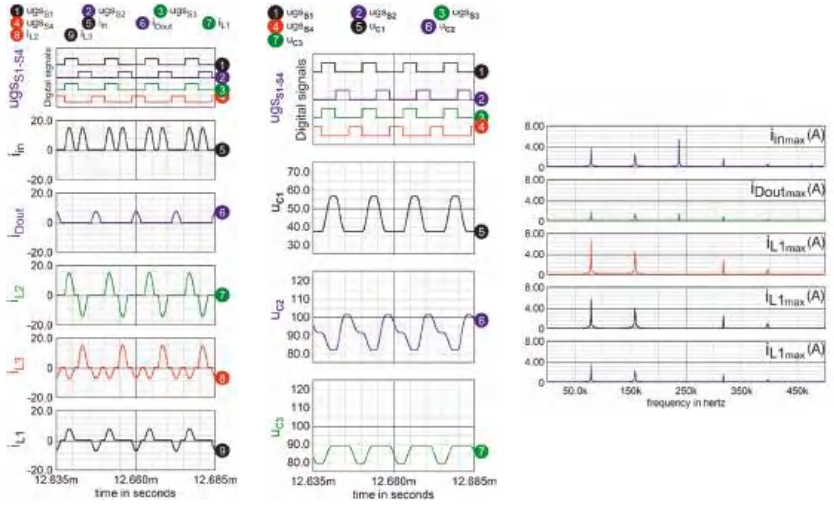


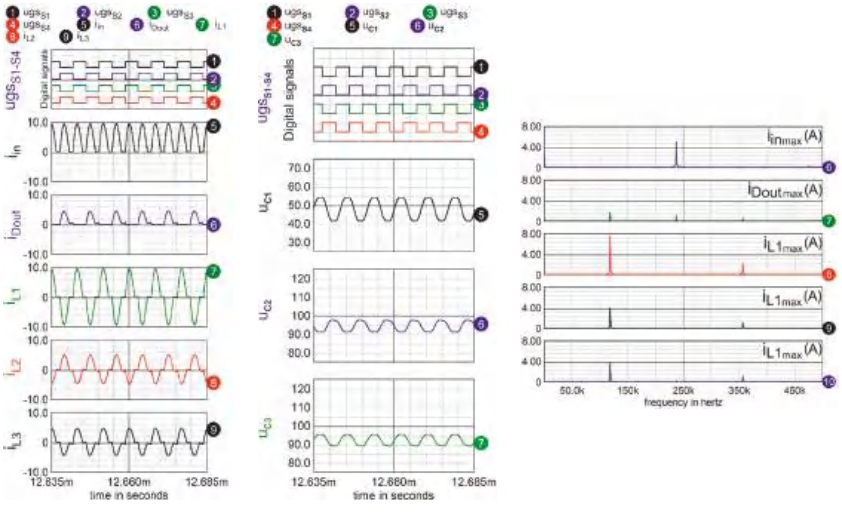
Figure 2. Steady-state operation of the LCSCVMa converter under switching strategy C1: (**a**) waveforms of the gate to source signals of transistors (presented with level shift), input current (in amperes), and voltages (in volts) on capacitors C_1, C_2, and C_3. (**b**) Spectrum of the input current, and currents of switched capacitors and output capacitor. The results were obtained with the use of ICAP/4 simulation software.

Figure 3. Steady-state output current and voltage waveforms of the LCSCVMb converter under switching strategy C1 (4 A/div and 100 mV/div). The results were obtained with the use of ICAP/4 simulation software.



(**a**) (**b**)

Figure 4. Steady-state operation of the LCSCVMa converter under switching strategy C2: (**a**) waveforms of the gate to source signals of transistors (presented with level shift), input current (in amperes), and voltages (in volts) on capacitors C_1, C_2, and C_3. (**b**) Spectrum of the input current, and currents of switched capacitors and output capacitor. The results were obtained with the use of ICAP/4 simulation software.



(**a**) (**b**)

Figure 5. Steady-state operation of the LCSCVMa converter under switching strategy C3: (**a**) waveforms of the gate to source signals of transistors (presented with level shift), input current (in amperes), and voltages (in volts) on capacitors C_1, C_2, and C_3. (**b**) Spectrum of the input current, and currents of switched capacitors and output capacitor. The results were obtained with the use of ICAP/4 simulation software.

To characterize the switching strategies, Table 1 contains the idealized control logic waveforms of the transistors (signals S_1 to S_4), as well as the description of the particular operation stages. Dead times have been neglected in Table 1, but they have been taken into account in the simulations and experiments. Capacitor C_2 (Figure 1) is not referred to as a switched capacitor. The maximum switching frequency (strategy C3) is defined as:

$$f_{\mathrm{Smax}} = \frac{1}{2T_{pulse}} \tag{1}$$

where T_{pulse} is the sum of the duration time $T_0/2$ of a single current pulse of any transistor and the dead time t_d (any period of time denoted as 1–5 in Table 1),

$$T_0 = \frac{1}{f_0} = 2\pi\sqrt{LC} \tag{2}$$

and $L = L_1 = L_2 = L_3$, $C = C_1 = C_2 = C_3$ (Figure 1).

All the simulation results were obtained for the following parameters: $U_{\mathrm{in}} = 50$ V, $L_n = 620$ nH, $C_n = 1.47$ µF, $f_0 = 166.7$ kHz, $T_{pulse} = 4.2$ µs ($f_{\mathrm{Smax}} = 119$ kHz), $C_{\mathrm{out}} = 100$ µF, $P_{\mathrm{out}} = 200$ W ($n = 1, 2, 3$). A resistance of 100 mΩ has been inserted into each branch as an equivalent to parasitic resistances. The time period T_{pulse}, as well as the duty cycle of the switching signals of the transistors, remain constant in each switching strategy. The selection of the switching frequency depends on the power of the converter, achievable resonant inductance, and switching losses [13]. This parameter, as well as the others, can be fixed in the following steps. In the ZCS mode, the SC converters' transistors do not operate in the ZVS mode, and during their turn-ons, the output charge is shorted (C_{oss} losses). The limit of C_{oss} losses determines the switching frequency of the transistors taking into consideration their type and voltage stresses. The oscillation frequency should be nearly equal to the switching frequency to minimize conduction losses [13]. This frequency depends on the product of L_nC_n, and allows to select C_n for a known value of L_n. The maximum power of the converter depends on capacitance C_n and the switching frequency [13], and it should be higher than or equal to the rated power for the selected parameters. The simulation results presented in this section have been obtained with the use of ICAP/4 simulation package based on the IsSpice4 simulator.

2.1.1. Simulation Results of the Switching Strategy C1

Figure 2 presents steady-state simulation waveforms of the LCSCVMa controlled according to strategy C1. From all the results, it can be seen that the switched capacitors are recharged by oscillatory currents and each stage of the switching is longer than the half-period of the oscillations.

The entire switching cycle is composed of five stages (Table 1). According to the principle of operation, turning on switches S_1 and S_3 involves the charging of the switched capacitors C_1 and C_3. Capacitor C_3 is being charged from capacitor C_2 of the internal branch whose voltage is going down in this stage. The diode D_2 remains turned off, as $u_{\mathrm{C2}} > u_{\mathrm{C1}}$ and $u_{\mathrm{C2}} > u_{\mathrm{in}}$ (Figure 2). In the next stage, switch S_2 is turned on, and capacitor C_2 is being charged from the source u_{in} and capacitor C_1 connected in series with it. The charging of the output capacitor, from capacitors C_2 and C_3 connected in series, occurs in the next stage when the switch S_4 is turned on. At the same time, capacitor C_1 is being charged from the source. In the next two stages, capacitor C_2 and capacitor C_{out} are being charged, consecutively.

The advantage of this switching strategy is reducing the number of the performed switching operations, which leads to switching losses limitation. In three of five stages of the switching period, only one switch is affected.

The input current has various values in each switching state, which is a drawback of this strategy. Therefore, a low-frequency component $f_{\mathrm{S}} = f_{\mathrm{ac\text{-}in}} = f_{\mathrm{Smax}}/2.5$ appears in current i_{in}, as well as in all other currents and voltages in the circuit. Using this kind of switching requires using a large input

filter and a large output capacitor. From the standpoint of the components' volume and input current filtering, this strategy is not favorable.

The output voltage used for the voltage gain calculation in relation (3) has been measured as the average value of the waveform presented in Figure 3 together with the output current. Further results, given in Equations (4)–(7), were obtained in the same manner.

In this strategy, the measured average value of the output voltage of the converter equals U_{out} = 178 V. For the input voltage of the converter U_{in} = 50 V (maintained by the voltage source in simulations), the voltage gain of the converter under switching strategy C1 equals:

$$G_{UC1} = \frac{U_{\text{out}}}{U_{\text{in}}} = \frac{178.0}{50.0} = 3.56 \tag{3}$$

2.1.2. Simulation Results of the Switching Strategy C2

Figure 4 presents simulation waveforms in the LCSCVMa controlled according to strategy C2. In this strategy, each switching period consists of three stages. The first two switching stages correspond to those in strategy C1. In the third stage, only transistor S_3 is on. The last two stages of strategy C1 do not occur here, and capacitor C_2 is charged and discharged only once in a switching period. The number of the switching operations is lower in comparison to that in strategy C1. The spectrum of currents and voltages shows more favorable qualities in strategy C2 versus C1, as the 50 kHz components are not present (the lowest frequency is 75 kHz).

In this strategy, the measured average value of the output voltage of the converter equals U_{out} = 177 V. For U_{in} = 50 V, the voltage ratio is

$$G_{UC2} = \frac{U_{\text{out}}}{U_{\text{in}}} = \frac{177.0}{50.0} = 3.54 \tag{4}$$

2.1.3. Simulation Results of the Switching Strategy C3

Figure 5 presents simulation waveforms in the LCSCVMa controlled according to strategy C3. In this strategy, there are only two stages. In the first stage, the charging of the switched capacitors takes place (switches S_1 and S_3 are turned on). During the second stage, the output capacitor and C_2 are being charged (with switches S_2 and S_4 turned on).

In this strategy, each switch operates with a much higher frequency than in the case of strategies C1 and C2. This brings an improvement in the spectrum of the currents and voltages, as the lowest frequency is 120 kHz. It is favorable from the passive components volume optimization standpoint.

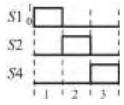
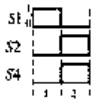
In strategy C3, the measured average value of the output voltage of the converter equals U_{out} = 185 V, and for U_{in} = 50 V, the voltage ratio is

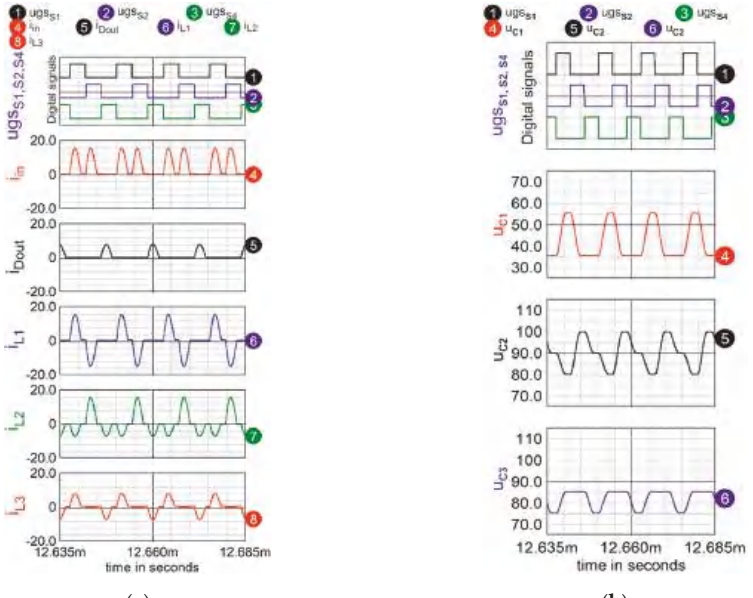
$$G_{UC3} = \frac{U_{\text{out}}}{U_{\text{in}}} = \frac{185.0}{50.0} = 3.7 \tag{5}$$

2.2. Switching Strategy Concepts for the LCSCVMb

The LCSCVMb converter is simpler than the LCSCVMa, and contains three switches only. There is only one stage of charging the switched capacitors, realized by the switch S_1, and two possible stages of discharging them, controlled by switches S_2 and S_3. This creates two switching strategies for this converter, which are presented in Table 2. Figures 6 and 7 depict simulation waveforms of the LCSCVMb controlled according to these strategies.

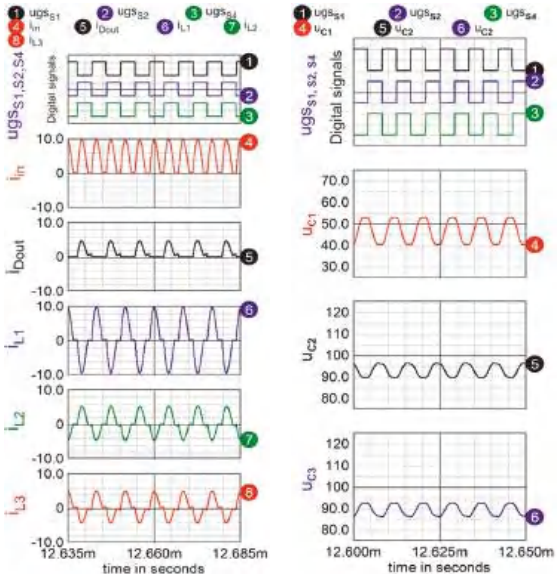
Table 2. Switching strategy concepts of the LCSCVMb. States of switches S_1, S_2, and S_4.

The Concept for Switching Strategy of LCSCVMb	Description—Stages of Charge Transfer in the Converter
Strategy C4 	Similarly to strategy C2 for the LCSCVMa, strategy C4 gives the following characteristic in the LCSCVMb: 1. Simultaneous charging of all the switched capacitors 2. Discharging C_1 to the internal branch (C_2) 3. Discharging C_2 and C_3 to the output
Strategy C5 	Similarly to strategy C3 for the LCSCVMa, strategy C5 gives the following characteristic in the LCSCVMb: 1. Simultaneous charging of all the switched capacitors 2. Simultaneous discharging of all the switched capacitors and charging the internal branch (C_2)



(**a**) (**b**)

Figure 6. Steady-state operation of the LCSCVMb converter under switching strategy C4: (**a**) Waveforms of the input current, inductor currents, and the current of the output diode (in amperes). (**b**) Voltages (in volts) on capacitors C_1, C_2, and C_3. The results were obtained with the use of ICAP/4 simulation software.



(**a**) (**b**)

Figure 7. Steady-state operation of the LCSCVMb converter under switching strategy C5: (**a**) Waveforms of the input current, inductors currents, and the current of the output diode (in amperes). (**b**) Voltages (in volts) on capacitors C_1, C_2, and C_3. The results were obtained with the use of ICAP/4 simulation software.

2.2.1. Simulation Results of the Switching Strategy C4

Figure 6 presents simulation waveforms of the LCSCVMb controlled according to strategy C4. The current and voltage waveforms in strategy C4 are nearly identical with those in strategy C2.

In this strategy, the measured average value of the output voltage of the converter equals U_{out} = 172.1 V, which yields (for U_{in} = 50 V):

$$G_{UC4} = \frac{U_{\text{out}}}{U_{\text{in}}} = \frac{172.1}{50.0} = 3.44 \tag{6}$$

2.2.2. Simulation Results of the Switching Strategy C5

Figure 7 presents simulation waveforms for the LCSCVMb controlled according to strategy C5. The current and voltage waveforms of the strategy C5 are nearly identical with those in strategy C3.

In this strategy, the measured average value of the output voltage of the converter equals U_{out} = 181.4 V. For U_{in} = 50 V, the voltage ratio is:

$$G_{UC5} = \frac{U_{\text{out}}}{U_{\text{in}}} = \frac{181.4}{50.0} = 3.63 \tag{7}$$

2.3. Comparison among the Topologies and Switching Strategies

In Section 2, a significant number of waveforms are presented for the particular strategies. The differences in the waveforms of the currents and voltages are clear, but to compare the concepts of the converters and the switching strategies, the following parameters will be taken into consideration and presented in charts:

- Number of components,
- Voltage gain,
- The lowest frequency in the input current (f_{ac_in}),
- The lowest frequency in the output current (f_{ac_out}),
- Voltage pulsation on capacitors ($U_{C1p\text{-}p}$, $U_{C2p\text{-}p}$, $U_{C3p\text{-}p}$),
- rms values of inductor currents (I_{L1_rms}, I_{L2_rms}, I_{L3_rms}),
- Maximum values of inductor currents (I_{L1_max}, I_{L2_max}, I_{L3_max}),
- Symmetry of inductor currents (Sym_i_L).

The data are presented in Table 3, where the parameters of the SCVM (on the basis of Reference [14] for an appropriate strategy) are included as well.

Table 3. Major parameters comparison among the parameters of LCSCVMa and LCSCVMb converters in the tests of 200 W operation.

Parameter	LCSCVMa Strategy			LCSCVMb Strategy		SCVM
	C1	C2	C3	C4	C5	
No. of switches	4	4	4	3	3	6
No. of diodes	4	4	4	5	5	4
U_{out}, V	178.0	177.0	185.0	172.1	181.4	191.2
T_S, µs	21.0	12.6	8.4	12.6	8.4	8.4
f_{ac_in}, kHz	47.6	79.4	238.1	79.4	238.1	238.1
f_{ac_out}, kHz	47.6	79.4	119.0	79.4	119.0	119.0
$U_{C1p\text{-}p}$, V	21.02	19.41	12.4	19.8	12.6	5.98
$U_{C2p\text{-}p}$, V	21.61	19.41	6.54	19.8	6.65	5.98
$U_{C3p\text{-}p}$, V	16.08	9.7	6.18	9.92	6.29	5.98
I_{L1_rms}, A	6.75	7.25	5.65	7.41	5.75	2.73
I_{L2_rms}, A	6.22	6.28	2.92	6.42	2.97	2.73
I_{L3_rms}, A	4.11	3.63	2.75	3.71	2.80	2.73
I_{L1_max}, A	16.1	14.8	9.46	15.1	9.60	4.57
I_{L2_max}, A	13.2	14.8	5.01	15.2	5.09	4.57
I_{L3_max}, A	12.3	7.43	4.74	7.56	4.80	4.57
Symmetry of current i_{L1}	no	yes	yes	yes	yes	yes
Symmetry of current i_{L2}	no	no	yes	no	yes	yes
Symmetry of current i_{L3}	no	yes	yes	yes	yes	yes

Figures 8–10 present a comparison between the values of parameters of the discussed converters, and the corresponding parameter of the SCVM.

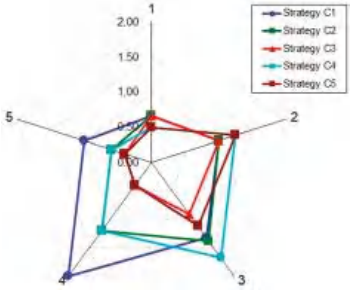
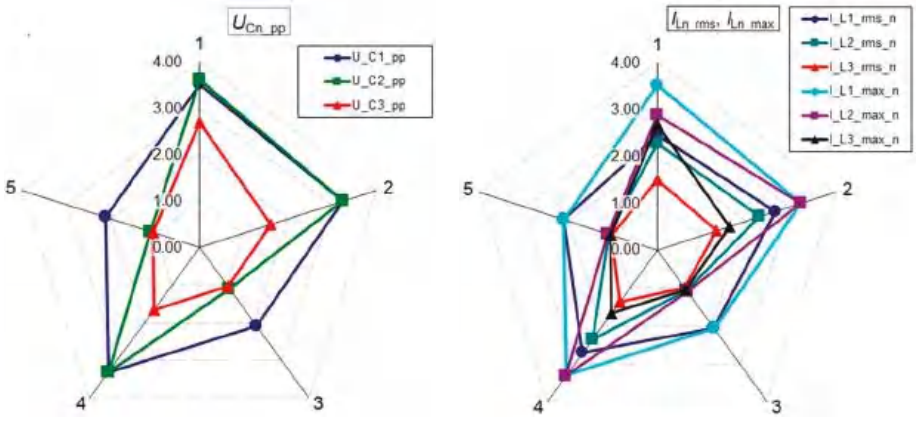
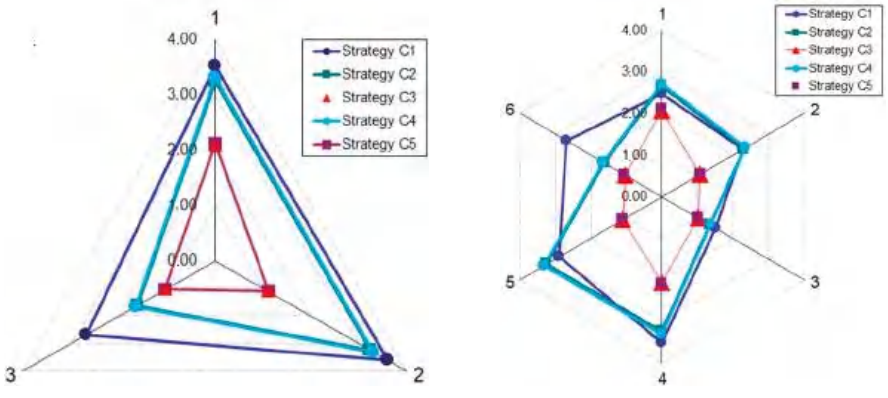


Figure 8. Comparison of converters' parameters under strategies C1–C5: Ratios of number of switches (axis 1) and number of diodes (axis 2) to those in SCVM (on the basis of data in Table 3). Quantity proportional to undesired output voltage decrease: 0.06·(200 – Uout) (axis 3). Ratios of the lowest frequencies in the input and output current: 0.4·f_{ac_in} SCVM/f_{ac_in} (axis 4), 0.4·f_{ac_out} SCVM/f_{ac_out} (axis 5).



(**a**) (**b**)

Figure 9. Ratios of the following parameters of strategies C1–C5 (axes 1–5): (**a**) Peak-to-peak voltages across capacitors C_1–C_3, (**b**) rms and maximum values of currents in inductances L_1–L_3. The results are based on the data in Table 3.



(**a**) (**b**)

Figure 10. Ratios of the following parameters (strategies C1–C5) to the corresponding parameter of SCVM: (**a**) Peak-to-peak voltages across capacitors C_1–C_3, (**b**) rms (axes 1–3) and maximum values of currents in inductances L_1–L_3 (axes 4–6). The results are based on the data in Table 3.

In Figure 8, the coefficients 0.06 and 0.4 are used respectively, to better visualize the undesired output voltage decrease in regard to the theoretical value of 200 V, and the lowest frequencies in the input and output current of the discussed converters compared to those in the SCVM. In each case, a lower value on the graph is better.

From the chart presented in Figure 9a, it follows that the lowest peak-to-peak (p-p) voltages, in all the strategies, are equal the voltage across capacitor C_3. Moreover, the strategies C3 and C5 show the lowest p-p voltages for all the internal capacitors (C_1–C_3). Figure 9b demonstrates that the currents of inductor L_3 are the lowest, and the strategies with the lowest inductor currents are C3 and C5.

The same qualities are visible in charts presented in Figure 10, which clearly demonstrate that the parameters of strategy C4 are nearly the same as those of strategy C2. The same refers to strategies C5 and C3.

The LCSCVMa and LCSCVMb converters can be further extended to units of higher voltage gain, similarly as in the case of the converters presented in References [13,22,25,26,29]. Taking into consideration the number of switches and diodes, as well as the frequency of the input current, both the proposed converters are very attractive for high-voltage-gain (Table 4). It should be noticed that the converter extension is very effective in the case of the LCSCVMb concept. For voltage gain $G_U = 8$, it requires only four switches, which is an excellent result in comparison to other pure SC converters. Other parameters such as voltage stresses on the switches can be found in the literature.

Table 4. Comparison of the number of switches and diodes, and the lowest frequency of the input current in selected topologies versus the voltage gain. Ref. = Reference.

Parameter	Toplogy								
	Gain	**LCSCVMa**	**LCSCVMb**	**Ref. [13]**	**Ref. [22]**	**Ref. [16]**	**Ref. [25]**	**Ref. [26]**	**Ref. [27]**
No. of switches (and diodes)	4	4 (4)	3 (5)	6 (4)	8 (0)	-	8 (0)	4 (4)	4 (6)
	7	-	-	12 (7)	14 (0)	7 (5)	-	-	7 (12)
	8	6 (6)	4 (7)	14 (8)	16 (0)	-	12 (0)	6 (6)	8 (14)
$f_{\text{iin\_min}}/f_{\text{Smax}}$ for all gains(f_{Smax}—in (1))		1	1	0.5	1	1/4	1	1	0.5

3. Efficiency Model of the LCSCVM Converters

The analysis below concerns the LCSCVMa operating under the strategy C3 (Table 1) and LCSCVMb operating under the strategy C5 (Table 2). In both cases, there are two stages of operation. Figure 11 depicts the current paths in the LCSCVMa. In the LCSCVMb, the switch S_1 conducts the sum of currents i_{L1} and i_{L3} in the stage 1, whereas the current paths in the stage 2 are the same as in the LCSCVMa.

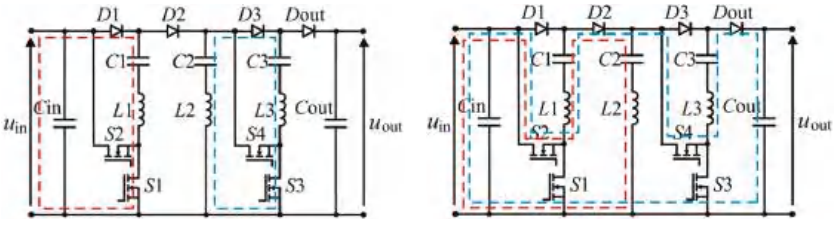


Figure 11. Current paths in the LCSCVMa: (**a**) in the stage 1 and (**b**) in the stage 2.

Assuming ideal power electronic switches, and a constant value of the input (U_{in}) and the output (U_{out}) voltage, as well as neglecting parasitic resistances and voltage drops across the power electronic devices, the currents in the stage 1 (Figure 11a) can be described as follows:

$$i_{L1}(t) = i_{C1}(t) = \frac{U_{\text{in}} - U_{C11}}{\rho} \sin\omega_0 t = I_{1\text{m}} \sin\omega_0 t \tag{8}$$

$$i_{L3}(t) = i_{C3}(t) = \frac{U_{\text{in}} - U_{C11}}{2\rho} \sin\omega_0 t = \frac{I_{1\text{m}}}{2} \sin\omega_0 t \tag{9}$$

$$i_{L2}(t) = i_{C2}(t) = -i_{L3}(t) \tag{10}$$

With the characteristic impedance and the angular resonant frequency given by

$$\rho = \sqrt{L/C},\ \omega_0 = 1/\sqrt{LC} \tag{11}$$

where U_{C11} is the initial voltage across capacitor C_1, and I_{1m} and $I_{2m}/2$ are the current amplitudes. Equation (8) presents the current of a typical series LC circuit supplied from a voltage source, and Equation (9) was obtained also taking into account the initial values of the capacitor voltages.

The values of the passive components depend on the assumed nominal power (P_{nom}), switching frequency (f_S), and the volume of the resonant inductor. The values of time T_{pulse} (1), and finally T_0 (2) and ω_0 (11), are assumed taking into account the limit of the switching losses in the converter. The capacitance of the switched capacitors is determined by the charge required to be transferred in a single switching pulse. The maximum power of the SCVM-type converter is achieved when the switched capacitors are fully discharged in a switching cycle (and then charged to the voltage equal to $2U_{in}$). This determines the minimum capacitance, which in the SCVM composed of n switching cells is defined as follows:

$$C_{min} = 2nf_S{U_{in}}^2/P_{nom}. \tag{12}$$

In a quasi inductiveless SCVM-type converter, the value of resonant inductance (L) is very small (L can be designed as a PCB air choke). Therefore, to achieve the assumed switching frequency, the capacitance of the switched capacitors can be selected considerably bigger than C_{min} (as in the case of the experimental setup presented in this paper). In the stage 2 (Figure 11b), the currents of capacitors C_1–C_3 and inductances L_1–L_3 have the same values (Equations (8)–(10)) as in the stage 1, but with the opposite signs. The voltages across the capacitors C_1, C_2, and C_3 in the stage 1 are given by

$$u_{C1}(t) = (U_{in} - U_{C11})(1 - \cos \omega_0 t) + U_{C11} \tag{13}$$

$$u_{C2}(t) = -\frac{(U_{in} - U_{C11})}{2}(1 - \cos \omega_0 t) + U_{C21} \tag{14}$$

$$u_{C3}(t) = \frac{(U_{in} - U_{C11})}{2}(1 - \cos \omega_0 t) + U_{C31} \tag{15}$$

where U_{C21} and U_{C31} are the initial voltages across capacitors C_2 and C_3, respectively.

In the stage 2 (Figure 11b), the expressions for voltages have similar forms with appropriate signs and initial values.

Based on the formulas mentioned above, all the voltage initial values and the output voltage can be computed as a function of U_{C11}. For example, we obtain

$$U_{out} = 5U_{in} - U_{C11} \tag{16}$$

U_{C11} can be calculated taking into account (8) and the following relation

$$I_{in-av} = I_{L1av} = \frac{2}{\pi} I_{1m} f_{Sn} = \frac{P_{in}}{U_{in}} \tag{17}$$

$$U_{C11} = U_{in} - \frac{\pi \rho P_{in}}{2 f_{Sn} U_{in}} \tag{18}$$

where

$$f_{Sn} = f_S / f_0 \tag{19}$$

From Equations (16) and (18), we have

$$U_{out} = 4U_{in} + \frac{\pi \rho P_{in}}{2 f_{Sn} U_{in}} \tag{20}$$

In practical converters, there are voltage drops across the circuit elements like the diodes and the transistors, which result in a variation of the output voltage with power and frequency.

The efficiency of an SCVM-type converter is determined by the resistances of its components, voltage drops on the diodes and transistors, the input voltage, power, and by the relation between the

switching period T_S and period T_0 (2), which can be expressed by f_{Sn} (19). Therefore, it is necessary to calculate the average and rms values of the currents. It is assumed that transistors S_1 and S_3 are IGBTs, and S_2 and S_4 are MOSFETs.

$$I_{D1av} = I_{D2av} = \frac{I_{L1av}}{2} = \frac{1}{\pi} I_{1m} f_{Sn} = \frac{P_{in}}{2U_{in}},\ I_{D3av} = I_{Dout-av} = \frac{I_{L2av}}{2} = \frac{I_{L3av}}{2} = \frac{I_{L1av}}{4} = \frac{P_{in}}{4U_{in}} \quad (21)$$

$$I_{S2} = \frac{1}{2} I_{1m} \sqrt{f_{Sn}} = \frac{\pi P_{in}}{4U_{in}\sqrt{f_{Sn}}},\ I_{S4} = \frac{1}{4} I_{1m} \sqrt{f_{Sn}} = \frac{\pi P_{in}}{8U_{in}\sqrt{f_{Sn}}} \quad (22)$$

For the LSCVMa, we have:

$$I_{S1av} = I_{D1av} = \frac{P_{in}}{2U_{in}},\ I_{S3av} = I_{D3av} = \frac{P_{in}}{4U_{in}} \quad (23)$$

Conduction losses, ΔPc, in both converters are

$$\Delta P_c = \sum_k r_k I_{Sk}^2 + \sum_l \Delta U_{Dl} I_{Dlav} + \sum_m \Delta U_{Sm} I_{Smav} + \sum_n r_T I_n^2 \quad (24)$$

where r_k denotes the total resistance of the branch with MOSFET transistor S_k (k = 2, 4), including the resistance of the transistor. ΔU_{Dl} is the voltage drop across diode D_l, ΔU_{Sm} is the voltage drop across IGBT transistor S_m, r_T is the resistance of each circuit with an IGBT transistor, and I_n is its rms current.

It is assumed that the voltage drops across the devices remain constant in the conducting state.

We assume that all the resistances and voltage drops are the same, i.e.

$$r_2 = r_4 = r,\ \Delta U_{S1} = \Delta U_{S2} = \Delta U_S,\ \Delta U_{D1} = \Delta U_{D2} = \Delta U_{D3} = \Delta U_{D4} = \Delta U_{Dout} = \Delta U_D \quad (25)$$

The efficiency of the LSCVMa converter can be calculated as follows. The resistive losses in the circuits containing IGBTs are:

$$\Delta P_{c2} = r_T I_{L11}^2 + 2 r_T I_{L31}^2 = \frac{3\pi^2 P_{in}^2 r_T}{32 U_{in}^2 f_{Sn}} \quad (26)$$

Taking (21)–(26) into account, the conduction losses can be presented as

$$\Delta P_c = \frac{5\pi^2 P_{in}^2 r}{64 U_{in}^2 f_{Sn}} + \frac{3\pi^2 P_{in}^2 r_T}{32 U_{in}^2 f_{Sn}} + \frac{3P_{in}}{2U_{in}}\left(\Delta U_D + \frac{1}{2}\Delta U_S\right) \quad (27)$$

The turn-off switching loss is zero, due to the ZCS switching. However, there is a turn-on switching loss, associated with charging and discharging the transistors' output capacitances. The total switching power loss, ΔP_{sw}, is

$$\Delta P_{sw} = \Delta W_{sw} f_S = \Delta P_{sw0} f_{Sn} \quad (28)$$

where ΔW_{sw} is the energy lost at turn-on in the transistor's resistances in a single switching cycle, and $\Delta P_{sw0} = \Delta W_{sw} \cdot f_0$ is power loss at resonant frequency. A way of calculating these losses is presented in Reference [31].

The efficiency is (Equations (27) and (28))

$$\eta = 1 - \frac{\Delta P_c}{P_{in}} - \frac{\Delta P_{sw}}{P_{in}} = 1 - \frac{5\pi^2 P_{in}^2 r}{64 U_{in}^2 f_{Sn}} - \frac{3\pi^2 P_{in}^2 r_T}{32 U_{in}^2 f_{Sn}} - \frac{3P_{in}}{2U_{in}}\left(\Delta U_D + \frac{1}{2}\Delta U_S\right) - \frac{\Delta W_{sw} f_S}{P_{in}} \quad (29)$$

Introducing normalized quantities:

$$r_{\mathrm{n}} = \frac{r}{U_{\mathrm{in}}^2/P_{\mathrm{in}}},\ r_{T\mathrm{n}} = \frac{r_T}{U_{\mathrm{in}}^2/P_{\mathrm{in}}},\ \Delta U_{D\mathrm{n}} = \frac{\Delta U_D}{U_{\mathrm{in}}},\ \Delta U_{S\mathrm{n}} = \frac{\Delta U_S}{U_{\mathrm{in}}},\ \Delta P_{\mathrm{sw0n}} = \frac{\Delta P_{\mathrm{sw0}}}{P_{\mathrm{in}}} \tag{30}$$

We can simplify the efficiency formula to the form

$$\eta = 1 - \frac{5\pi^2 r_{\mathrm{n}}}{64 f_{S\mathrm{n}}} - \frac{3\pi^2 r_{T\mathrm{n}}}{32 f_{S\mathrm{n}}} - \frac{3}{2}\left(\Delta U_{D\mathrm{n}} + \frac{1}{2}\Delta U_{S\mathrm{n}}\right) - \Delta P_{\mathrm{sw0n}} f_{S\mathrm{n}} \tag{31}$$

The efficiency of the LSCVMb can be calculated with the use of the following components:

$$I_{S1\mathrm{av}} = I_{D1\mathrm{av}} + I_{D3\mathrm{av}} = \frac{3P_{\mathrm{in}}}{4U_{\mathrm{in}}},\ I_{D4\mathrm{av}} = I_{D1\mathrm{av}} = \frac{P_{\mathrm{in}}}{2U_{\mathrm{in}}} \tag{32}$$

where D_4 is the LSCVMb additional diode (Figure 1b).

Conduction losses, ΔPc, of LSCVMb are as follows:

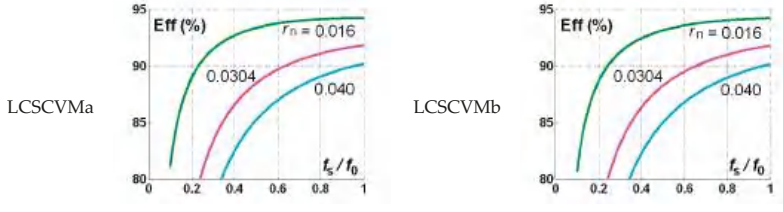
$$\Delta P_{\mathrm{c}} = \frac{5\pi^2 P_{\mathrm{in}}^2 r}{64 U_{\mathrm{in}}^2 f_{S\mathrm{n}}} + \frac{3\pi^2 P_{\mathrm{in}}^2 r_T}{32 U_{\mathrm{in}}^2 f_{S\mathrm{n}}} + \frac{P_{\mathrm{in}}}{U_{\mathrm{in}}}\left(2\Delta U_D + \frac{3}{4}\Delta U_S\right) \tag{33}$$

and the efficiency of the LSCVMb is

$$\eta = 1 - \frac{5\pi^2 r_{\mathrm{n}}}{64 f_{S\mathrm{n}}} - \frac{3\pi^2 r_{T\mathrm{n}}}{32 f_{S\mathrm{n}}} - \left(2\Delta U_{D\mathrm{n}} + \frac{3}{4}\Delta U_{S\mathrm{n}}\right) - \Delta P_{\mathrm{sw0n}} f_{S\mathrm{n}} \tag{34}$$

It can be seen from (30), (31), and (34) that the impact of the voltage drops across the diodes on the efficiency depends only on the ratio of these voltage drops to the supply voltage. The impact of the losses in the resistances is more complex. They increase with rising resistances and rising power, and decrease with rising input voltage and frequency f_S. Switching losses are proportional to switching frequency f_S.

The relationship between the efficiency and normalized frequency $f_{S\mathrm{n}} = f_S/f_0$ for three values of r_{n} (30): 0.016, 0.0304, and 0.040, $\Delta U_{D\mathrm{n}}$ (30) = 0.008 for the LCSCVMa and the LCSCVMb is shown in Figure 12. The value of r_{n} = 0.0304 corresponds to, e.g., U_{in} = 50 V, P_{in} = 200 W, L = 500 nH, C = 1.5 µF, r = 380 mΩ, and $\Delta U_{D\mathrm{n}}$ is equal to 0.008 for, e.g., ΔU_D = 0.40 V and U_{in} = 50 V. The value of relative switching losses P_{sw0n} (30) = 0.0101 (Figure 12b) is valid, e.g., for ΔW_{sw} (28) = 11 µJ, f_0 = 183.8 kHz, and P_{in} = 200 W. The efficiency of the LCSCVMb is slightly lower. In both cases, it increases with increasing normalized frequency, $f_{S\mathrm{n}}$, and strongly depends on the circuit parasitic resistances. Therefore, it is important to minimize them, and use transistors with low values of $R_{\mathrm{DS(on)}}$ and $V_{\mathrm{CE(on)}}$.



(**a**) (**b**)

Figure 12. Theoretical charts of efficiency vs. $f_{S\mathrm{n}} = f_S/f_0$ for three values of r_{n}: 0.016, 0.0304, and 0.040, and $\Delta U_{D\mathrm{n}}$ = 0.008: (**a**) LCSCVMa at switching losses ΔP_{sw0n} = 0.0138, (**b**) LCSCVMb at switching losses ΔP_{sw0n} = 0.0101.

The efficiency can be computed in a similar way for the other switching strategies. However, the calculations will be more complex in the case of the strategies with more than 2 stages.

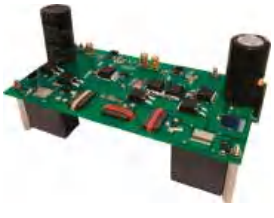
4. Experimental Verification

This chapter presents the experimental results of the LCSCVMb converter operation. All the tests were carried out under switching strategy C5. The experimental verification confirms the proper operation of the converter, according to its concept. The measured voltage gain was on the expected level, and all the relevant waveforms were consistent with the simulation results as well.

4.1. Experimental Setup

All the parameters of the converter used during the experimental research, as well as a photograph of the investigated converter, are collected in Table 5. The parameters of the experimental setup correspond to the simulation model, and the major difference can be found in the inductance of the planar PCB choke. The switching frequency in the experimental measurements has been adjusted to the oscillation period of the switched capacitor currents and differs from the value selected for the simulation tests. An IGBT switch was selected as S_1 in the LSCVMb, as this switch conducts the total charging current. This current can be significant, especially when the converter contains a larger number of the switching cells. In order to generate appropriate control signals, an FPGA evaluation board (INTEL DE0) was utilized. The basic clock frequency of this device was set at 200 MHz, and the time resolution of the generated signals was 5 ns. The test setup is an example design of the converter prepared for the purpose of research, to verify its concepts and feasibility. The tests were conducted with 50 V at the input; however, the voltage range as well as power and the design concept can be rescaled to the parameters of a target application. Moreover, it is important that the prospective applications of the non-isolated DC-DC converter should comply with safety standards.

Table 5. The most important parameters of the laboratory converter.

Parameter	Value	The Laboratory Setup
Input voltage	50 V	
Output load	200 W	
Switching frequency	133 kHz	
Resonant capacitors	1.5 µF (KEMET R76 series)	
Resonant inductances	Planar chokes: L = 500 nH, R_{ESR} = 18 mΩ @ 100 kHz	
Transistors	IKB15N65EH5 (V_{DS} = 650 V, V_{CE} = 1.65 V) as S_1 IPB50R140CP (V_{DS} = 550 V, R_{DSon} = 0.14 Ω) as S_2 and S_4	
Diodes	STTH30L06G (I_F = 30 A, V_F = 1.0 V, V_{RRM} = 600 V)	
PCB	2 layers, 35 µm	
Laboratory equipment	Digital scope: Tektronix MDO3104, current probes: Tektronix TCP0030 150 MHz (input current measurement), Rogowsky coil (switch current measurements) voltage probes: Tektronix THDP0200 200 MHz, Tektronix P5205 100 MHz, power analyzer: Yokogawa WT 1801	

4.2. Test Results

Figure 13a,b presents the waveforms of the switching signals with the input and output current. They confirm that the converter operates correctly according to strategy C5. From the waveforms presented in Figure 13c, it follows that the converter boosts the input voltage. The measured voltage ratio is 3.65. Figure 13d,e presents the input current waveform and the voltages across the resonant capacitors. From the waveforms presented in Figure 13d, the average voltage across the capacitors can be seen. To demonstrate more clearly the magnitude of the oscillation around the average voltage value of each resonant capacitor, the voltage traces in AC coupling mode were recorded as well (Figure 13e). Figure 13f presents voltage stresses across the switches. From these results, it follows that the voltage

stresses on switches are significantly below the output voltage of the converter, which is very favorable from the switching losses standpoint.

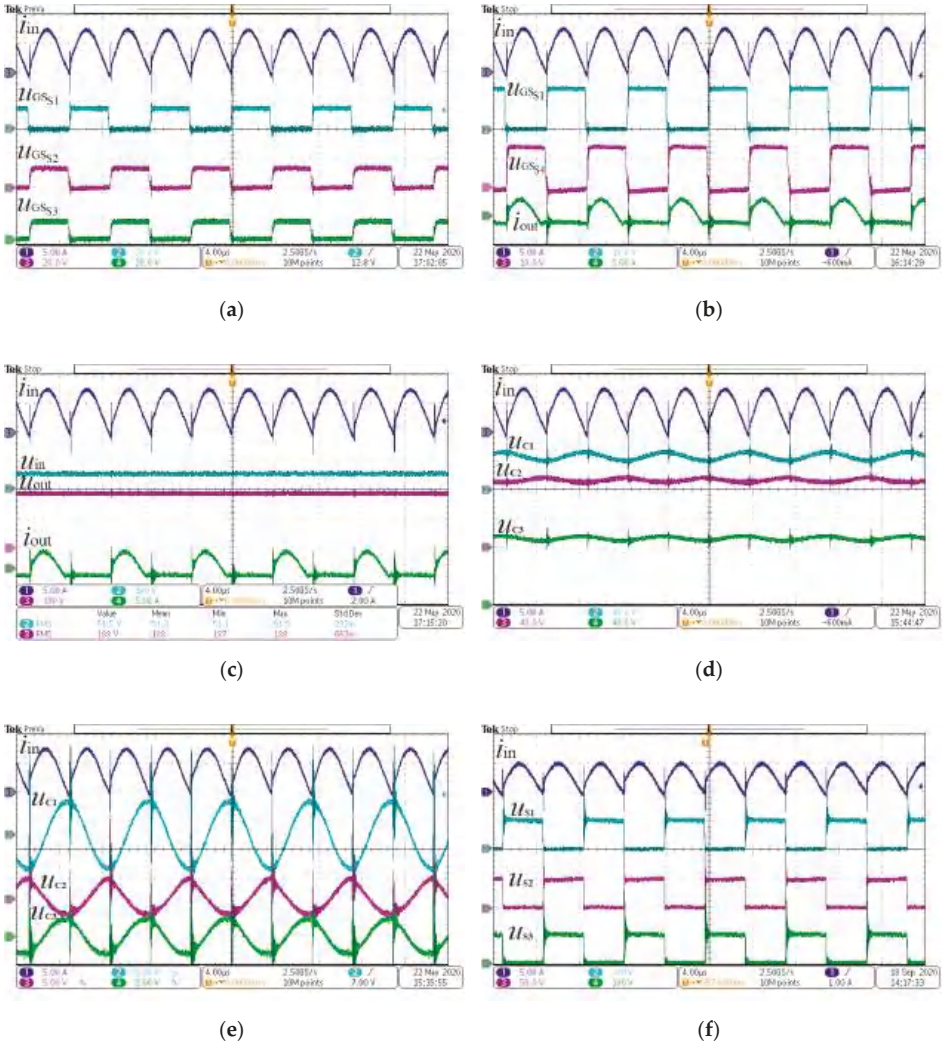


Figure 13. A set of recorded waveforms during experimental tests: (**a**) Switching signals of transistors and the input current, (**b**) input and output current of the converter on the background of switching signals, (**c**) input and output waveforms of the converter (current and voltage traces), (**d**) converter input current and voltages across resonant capacitors recorded in DC coupling mode, (**e**) converter input current and voltages across resonant capacitors recorded in AC coupling mode, and (**f**) voltage stresses across the switches on the background of converter input current. Switching strategy C5.

During the experimental research, the basic operation concept of the investigated converter has been checked. Furthermore, the working correctness of the examined device under different output loads was verified. The tests were carried out for three output load values: 62, 146, and 290 W, focusing especially on the transistor currents and voltages. Figure 14 present the results of the conducted tests

for different output load conditions. From the results, it follows that the converter operates properly in low and medium load conditions.

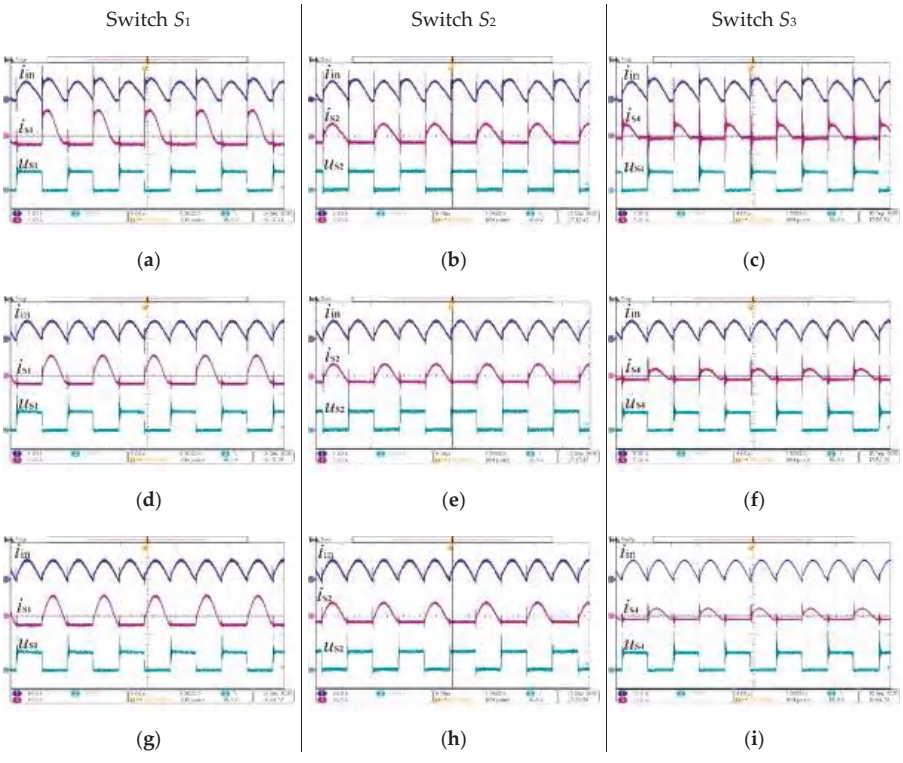
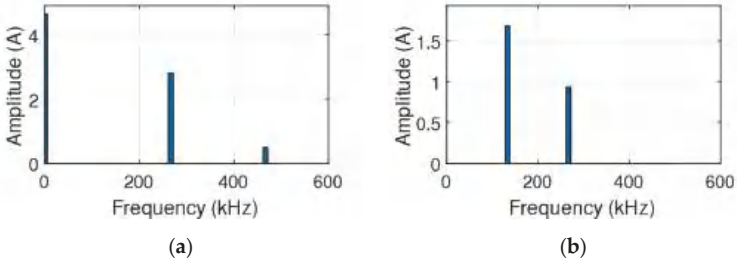


Figure 14. Waveforms of the input current as well as the currents and voltages across switches, during experimental test proceeded with different values of converter output power: (**a**–**c**) P_{out} = 62 W, 2A/div, 100V/div, (**d**–**f**) P_{out} = 146 W, 5A/div, 100V/div, (**g**–**i**) P_{out} = 290 W, 10A/div, 100V/div. Switching strategy C5.

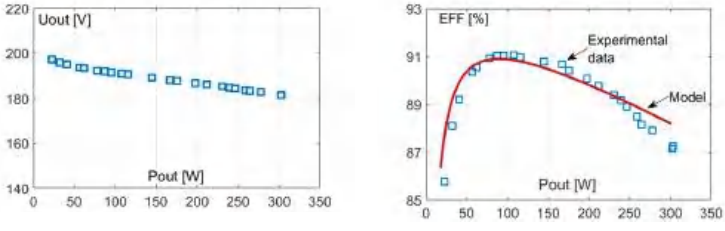
Figure 15 presents the results of the spectral analysis calculated for the input and output currents. The calculations have been carried out with the use of MATLAB software, based on the recorded experimental data. The data was collected by the digital oscilloscope (Tektronix MDO3104) with the sampling rate of 1 MS/s.



(**a**) (**b**)

Figure 15. Results of spectral analysis for: (**a**) The input current and (**b**) the output current.

The experimental results of the output voltage of the LCSCVMb converter and its efficiency are presented in Figure 16. The efficiency is on an acceptable level. The voltage and efficiency drop versus power is typical for such SC-based converters, and results from their resistive losses. It should be noticed that the presented experimental setup is optimized towards the converter cost reduction. It was designed on a two-layer PCB of 35 µm. To increase the efficiency by reducing the parasitic resistance, a more expensive PCB and switches can be selected.



(**a**) (**b**)

Figure 16. Experimental and simulation results for LSSCVMb under strategy C5 at U_{in} = 50 V, f_S = 133 kHz: (**a**) Measured output voltage U_{out} vs. P_{out}, (**b**) measured efficiency vs. P_{out} with comparison to theoretical results obtained from (34) for r = 380 mΩ, V_F = 400 mV, $V_{CE(on)}$ = 1 V, W_{sw} = 11 µJ.

5. Conclusions

The presented concepts of the new topologies, as well as the comparison of parameters presented in Table 3, and charts in Figures 8–10, lead to the following conclusions:

- The major idea of the proposed new converters is based on the elimination of the number of switches in a voltage multiplier (SCVM), while maintaining its proper operation. By the modification of an SCVM, the new topology concepts LCSCVMa and LCSCVMb were proposed, with a reduced number of switching cells and redesigned functions of the diodes. Depending on the technology of practical implementation, either of these converters can be more attractive than the other.
- Various switching strategies are possible for the converters, which affect the parameters of operation related to switching losses and the sizing of the passive components of the converter, but also the required input and output filters.
- The converter operates properly with a wide range of output loads.
- From the compared results, it follows that the most effective topology, the LCSCVMb, can operate with nearly the lowest parameters of AC component in the voltages on capacitors, and the highest frequency in the input and output current. This allows for a reduction of the converter volume, especially by optimizing the input and output filters.
- The discussed converters demonstrated an improvement in the SCVM topology, which may result in a prospective cost reduction.

Author Contributions: Conceptualization, R.S.; methodology, R.S. and Z.W.; software, R.S., Z.W. and S.F.; validation, R.S., Z.W. and S.F.; formal analysis, R.S. and Z.W.; investigation, R.S., Z.W. and S.F.; resources, R.S.; data curation, R.S., Z.W. and S.F.; writing—original draft preparation, R.S., Z.W. and S.F.; writing—review and editing, visualization, supervision, R.S., Z.W. and S.F.; project administration, R.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

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A New Approach to the PWM Modulation for the Multiphase Matrix Converters Supplying Loads with Open-End Winding

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Received: 14 December 2020; Accepted: 13 January 2021; Published: 17 January 2021

Abstract: This article presents three variants of the Pulse Width Modulation (PWM) for the Double Square Multiphase type Conventional Matrix Converters (DSM-CMC) supplying loads with the open-end winding. The first variant of PWM offers the ability to obtain zero value of the common-mode voltage at the load's terminals and applies only six switches within the modulation period. The second proposal archives for less Total Harmonic Distortion (THD) of the generated load voltage. The third variant of modulation concerns maximizing the voltage transfer ratio, minimizing the number of switching, and the common-mode voltage cancellation. The discussed modulations are based on the concept of sinusoidal voltage quadrature signals, which can be an effective alternative to the classic space-vector approach. In the proposed approach, the geometrical arrangement of basic vectors needed to synthesize output voltages is built from the less number of vectors, which is equal to the number of the matrix converter's terminals. The PWM duty cycle computation is performed using only a second-order determinant of the voltages coordinate matrix without using trigonometric functions. A new approach to the PWM duty cycles computing and the load voltage synthesis by 5×5 and 12×12 topologies has been verified using the PSIM simulation software.

Keywords: square-type matrix converters; pulse width modulation; multiphase systems

1. Introduction

A fully controlled bidirectional semiconductor switch is an element of the Conventional Matrix Converter (CMC) which offers a direct AC–AC voltages conversion with additional input power factor control functionality. This type of converter, in comparison with the more established Voltage Source Inverter (VSI), has certain individual features that determine the innovation of such a solution [1–3]. It does not contain a bulk dc-link capacitor, thus is far more promising in terms of power density with the inherent four-quadrant operation [4,5]. Compared to traditional variable speed drives with CMC, the multi-phase electric motor drive gives some fundamental advantages. These configurations have grater system redundancy because it can operate during some fault conditions, is characterized by the lower torque ripple and lower per-leg converter rating [6]. Furthermore, the operation of multiphase motors is quieter, allowing for the independent control of two or more series/parallel connected motors [7]. Multiphase

electric machines can be fed also by the conventional matrix converter with three inputs [8–11]. The matrix topology is also presented as a unit, which control the power flow between the power generator and the electrical grid [12–16]. Multiphase generators have also been used in systems generating electricity such as offshore installations and wind farms [17,18]. Another application of the multiphase matrix converter in straight forward energy conversion is described in [19], where the 6×6 CMC and multi-winding transformer have been used to supply variable reactive power flow to the power system. A modulation approach based on the model of the 5×5 matrix converter with fictitious DC-link was shown in conference paper [20].

Multi-phase electric machines, including three-phase and five-phase variants, can be designed as a machine with open stator winding. Such a solution, especially in combination with a CMC, offers some important features. First, the possibility of direct power supply to both ends of the stator phase winding increases the maximum voltage amplitude within the linear range of the PWM modulator [21]. It should be noted here that the output voltage of the CMC cannot exceed the input voltages envelope. A quite frequency discussed problem in drives controlled by power converters, is the common voltage, which can be understood as a voltage measured between the ground potential and a virtually created star point connected with the stator terminals. The common-mode voltage in terminals of AC drives resulting in bearing currents harmful for the motor drive. The use of certain voltage modulation techniques in a matrix converter allows eliminating this problem [5,22–24]. As indicated in the brief introduction multi-phase drives with CMCs are rather niche applications. However, PWM algorithms are the subject of numerous studies, and almost all of the presented algorithms assume ideal sinusoidal input voltage and are designed for machines with the symmetric construction. The application of these methods without consideration of an input voltage asymmetry or the source harmonics in the calculation results in inaccurate load voltage generation. The approach to voltage synthesis proposed in the article takes this aspect into account and allows for the generation of the appropriate load voltage.

Due to a large number of input and output phases, the complexity of PWM algorithms based on the space-vector approach increases significantly. For a single matrix converter with three inputs and three outputs, the number of switch states is 3^3 (27). In the case of five input, five output converter, it gives 5^5 (3125) and analogically in drive with the open-end stator winding, the number of states is equal to 5^{10}. Therefore, the graphical presentation of voltage vectors corresponding to all switch states, at a given moment of time, becomes very unreadable, which makes it problematic to design and elaborate the dedicated PWM algorithms. The works [3,25] show that the synthesis of output voltages in multi-phase systems can be successfully simplified. These methods can be classified to the direct method of modulation. Compared to the transformation proposed by Clarke, the use of the Hilbert transform leads to the reduction of the number of required vectors. Therefore, for the CMC 5×5 the PWM algorithm can be developed using only 10 vectors. Apart from the modulation methods based on the space-vector approach, a group of methods of direct modulation can be indicated, such as the Venturini solution [1,26,27], while the general Venturini formulas for PWM duty cycles for several multi-phase converters, including square-type matrix converters are presented in [28]. The work in [25] proposes Wachspress formulas, which can be theoretically applied for any number of inputs. The use of either the Venturini solution or the Wachspress functions forces the commutation all switches of the given output cell (shown in the drawing later in the article). This can be explained by the fact that the switch modulating function is continuous, thus results in higher switching losses. All the PWM modulation methods discussed in the article are characterized by a lower number of switching cycles of at most 6 during the modulation period.

The paper is organized as follows. Definitions and principles of the proposed an output voltage synthesis using the DSM-CMC converter are presented in Section 2. This section also presents the method of generating quadrature signals using the Discrete Second-Order Generalized Integrator (DSOGI) structure. Then, the next three sections demonstrate variants of the proposed modulation. Abilities of the

input displacement angle control have been also discussed. Results are summarized and discussed in the conclusion section. Due to a huge number of switching elements, the realization of the experimental setup is very expensive. Therefore, the conclusions presented in the article are the result of circuit simulation in PSIM11 software and analytical research only. However, the proposed solution has been verified partially by an experiment and published in [3,25,29].

2. The Principle of an Output Voltage Synthesis in DSM-CMC Converter

The DSM-CMC converter consists of two square-type matrix converters, CMC_P and CMC_N, connected to load terminals as shown in Figure 1, where the simplified diagram of the circuit is depicted. If the number of load phases is equal to n, the total number of bidirectional power electronic switches is equal to $2n^2$. Both converter are connected with the n-phase AC voltage source v_{i1}, v_{i2}, ..., and v_{in}. The voltage of the phase x of the load

$$v_{ox}(t) = v_{Px}(t) - v_{Nx}(t) \tag{1}$$

measured at the load terminals, are synthesized by these converters by using the switch group h_{11}, h_{21}, ..., h_{n1}.

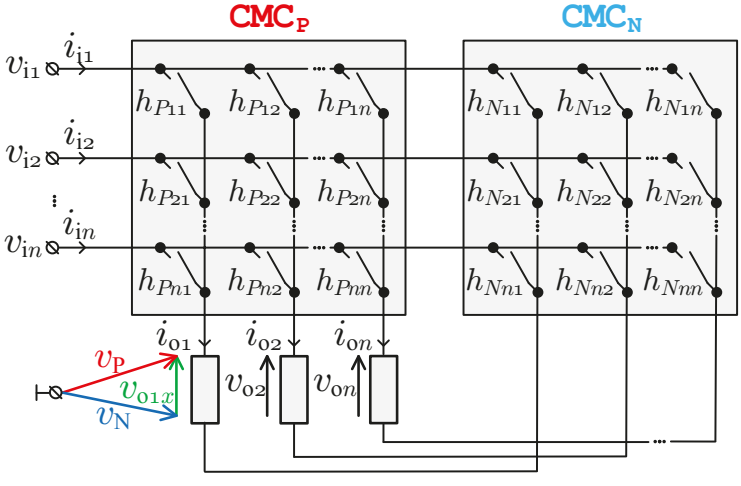


Figure 1. Simplified diagram of the square-type double conventional matrix converter.

As can be seen in Figure 2, switches on both sides of one phase of the load make the single commutation cell with two voltage multiplexers, s_P and s_N, respectively.

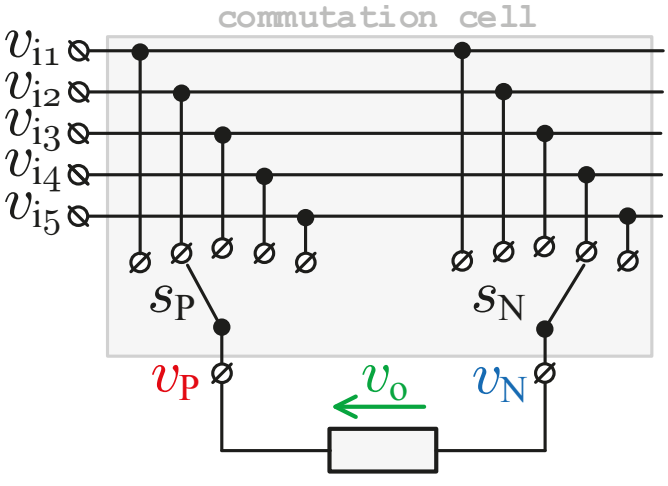


Figure 2. The single commutation cell for DSM-CMC 5 × 5.

2.1. Case of 5 Phases

The number of multiplexer switches is equal to the number of input voltages, and in this case, takes 5. For a better understanding of the proposal, let the further consideration will be focused on 5 × 5 topology.

According to the proposed concept of the voltage synthesis described in [3], all input voltages with pulsation ω_i can be represented as a collection of five rotating vectors:

$$\mathbf{v_i} = \begin{bmatrix} v_{i1x} & v_{i1y} \\ v_{i2x} & v_{i2y} \\ v_{i3x} & v_{i3y} \\ v_{i4x} & v_{i4y} \\ v_{i5x} & v_{i5y} \end{bmatrix} \tag{2}$$

with the real

$$\begin{aligned} v_{i1x} &= V_{i1} \cdot \cos(\omega_i t) \\ v_{i2x} &= V_{i2} \cdot \cos(\omega_i t - 2\pi/5) \\ v_{i3x} &= V_{i3} \cdot \cos(\omega_i t - 4\pi/5) \\ v_{i4x} &= V_{i4} \cdot \cos(\omega_i t - 6\pi/5) \\ v_{i5x} &= V_{i5} \cdot \cos(\omega_i t - 8\pi/5) \end{aligned} \tag{3}$$

and the imaginary parts of coordinates

$$\begin{aligned} v_{i1y} &= V_{i1} \cdot \sin(\omega_i t) \\ v_{i2y} &= V_{i2} \cdot \sin(\omega_i t - 2\pi/5) \\ v_{i3y} &= V_{i3} \cdot \sin(\omega_i t - 4\pi/5) \\ v_{i4y} &= V_{i4} \cdot \sin(\omega_i t - 6\pi/5) \\ v_{i5y} &= V_{i5} \cdot \sin(\omega_i t - 8\pi/5) \end{aligned} \tag{4}$$

where V_{i1}, ..., V_{i5} are the amplitudes of these voltages. Due to the analytic signal concept based on the Hilbert transform, for the pure sinusoidal input waveforms, the imaginary coordinates are just quadrature

components and an input voltage vectors collection can be presented as shown in Figure 3 as the symmetric system.

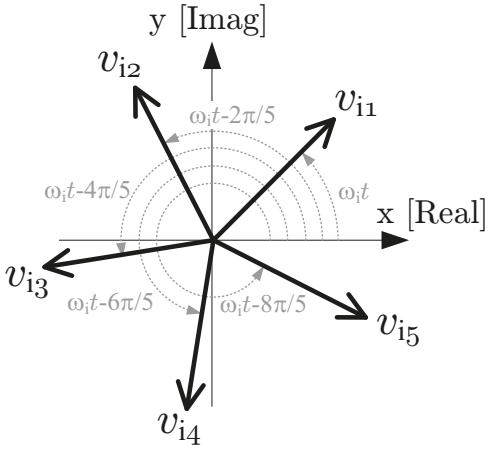


Figure 3. The collection of five the rotating input vectors.

These coordinates can be determined using the Hilbert filter or obtained through FFT/DFT based operation [30–32]. However, the Hilbert filter and algorithms based on DFT, although are quite accurate, are not the simple solution from code developing point of view. Moreover, error signals in the form of DC offsets, glitches, and momentary voltage sags may occur in measurements. Therefore, the input vector coordinates can be calculated in a different manner. A compromise solution, between accuracy and not complicated solution, maybe the use of the Double Second-Order Generalized Integrator with loop feedback extension functioned as Orthogonal Signal Generator (DSOGI-OSG), which in the OSG part prevents unexpected resonance and variables overflow. DSOGI-OSG structure in continuous time-domain is presented in Figure 4.

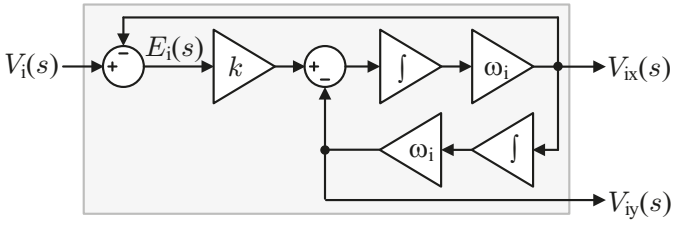


Figure 4. Double Second-Order Generalized Integrator with loop feedback extension functioned as Orthogonal Signal Generator (DSOGI-OSG) structure in continuous time-domain [33–35]: V_i—the input sinusoidal signal, V_{ix}—in-phase component of the input signal, V_{iy}—the quadrature component of the input signal, E_i the error signal, k—the gain block, ω_i—reference pulsation of the input signal, and $\int$ is an integrator block.

The transfer function takes the form of (5) for in-phase output and (6) for orthogonal output, while (7) represents the notch filter equation

$$\frac{V_{\mathrm{ix}}(s)}{V_{\mathrm{i}}(s)} = \frac{k \cdot \omega_{\mathrm{i}} \cdot s}{s^2 + k \cdot \omega_{\mathrm{i}} \cdot s + {\omega_{\mathrm{i}}}^2} \tag{5}$$

$$\frac{V_{\mathrm{iy}}(s)}{V_{\mathrm{i}}(s)} = \frac{k \cdot \omega_{\mathrm{i}}^2}{s^2 + k \cdot \omega_{\mathrm{i}} \cdot s + {\omega_{\mathrm{i}}}^2} \tag{6}$$

$$\frac{E_{\mathrm{i}}(s)}{V_{\mathrm{i}}(s)} = \frac{s^2 + {\omega_{\mathrm{i}}}^2}{s^2 + k \cdot \omega_{\mathrm{i}} \cdot s + {\omega_{\mathrm{i}}}^2} \tag{7}$$

where the parameter k is a value less than unity (k is taken the value of $1/\sqrt{2}$ here), $E_{\mathrm{i}}(s)$ is the error signal, while ω_{i} is an input voltage nominal pulsation. If processed signal frequency does not have an exact value, another extension of SOGI structure, called Frequency-Locked Loop (FLL), may be applied [36–38].

The load voltage v_{o} produced by the single commutation cell, shown in Figure 2, can be analogous represented by two rotating vectors, v_{P} and v_{N}, as is depicted in Figure 5. Only the geometrical distance of real (indicated by subscript x) coordinates of these vectors produce the load voltage. While the imaginary coordinate (indicated by subscript y) can generate the reactive power flow at the converter input. In general, there exists some degree of freedom for selecting the instantaneous value of this component because it does not influence on the load currents. The article is focused on the cases, which locus of each output vector is straight a circle. This means that a rotating output voltage vector moves along a circular trajectory and this movement can be clockwise or counterclockwise. Four variants of the PWM modulation scheme are shown in Figure 5.

A vector arrangement in Figure 6a, for the given commutation cell, can be presented as the rotating polygon as illustrated in Figure 6b. The polygon surface is named here as the output voltage synthesis field. All the points, which represent output voltage vectors, have to be located inside the synthesis field. Such a geometric arrangement allows for direct application the Wachspress function for the PWM duty cycles calculation [25,28]. However, the number of switching within the modulation period should be minimal, and for this reason, Venturini and Wachpress solution is not suitable. Decreasing the number of switching can be realized by applying the Nearest Three Vectors (NTV) modulation technique, which relays on the selection of a proper triangle in the synthesis field. Figure 6c shows two selected triangles for the voltages generated by $\mathrm{CMC_P}$ and $\mathrm{CMC_N}$ converters. Note that both points, representing these voltages, are located in their triangular local synthesis fields. This is the required condition of output voltage synthesizability. The selection of the optimal triangle may consist in finding the appropriate vertex of the synthesis field, which clearly indicates the input vector closest to the output vector. In the case of using NTV technique, this solution is sufficient, because the other two required vectors are adjacent to the selected one. As can be seen, vector v_{P} is closest to the vertex number 2, while vector v_{N} is closest to vertex 4. All six required PWM duty cycles can be calculated using the smooth interpolation technique, which is, in the discussed case, nothing more than an appropriate triangle area relation for the NTV modulation [3]. An area of the triangle can be computed using the second-order matrix determinant. Thus, an application of that solution only needs coordinates of the triangle vertices. As mentioned earlier, these coordinates can be computed using the DSOGI-OSG block shown in Figure 4.

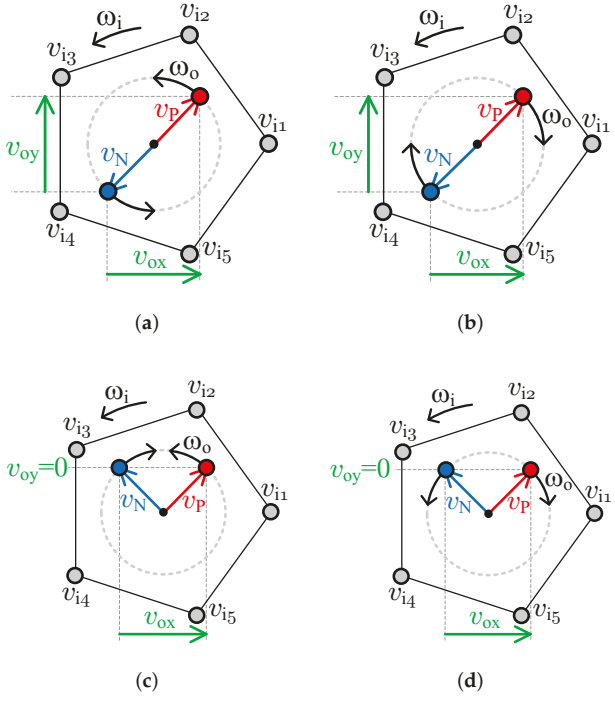


Figure 5. Four variants of output vectors rotation: (**a**) CCV-CCV, (**b**) CV-CV, (**c**) CCV-CV, and (**d**) CV-CCV.

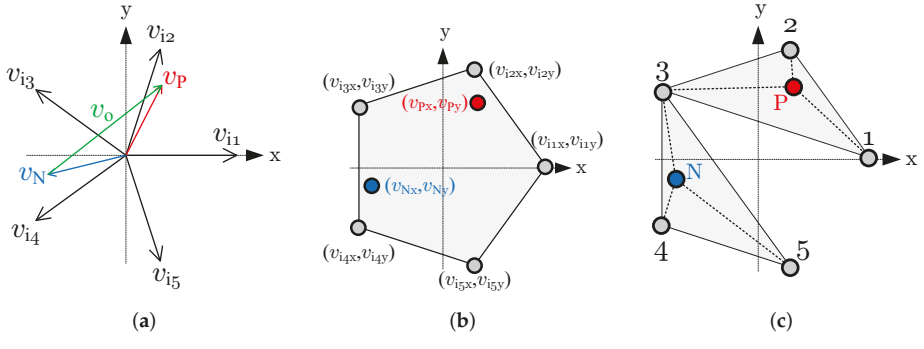


Figure 6. The principle of operation: (**a**) vectors arrangement, (**b**) synthesis field, and (**c**) selected triangles.

2.2. Case of 12 Phases

In the case of more input voltages, for example, when the number of inputs is equal to 12, the choice of the optimal triangle is not so obvious. Now, let us consider the graphical vector arrangements for 12×12 topology expressed as regular polygon shown in Figure 7a.

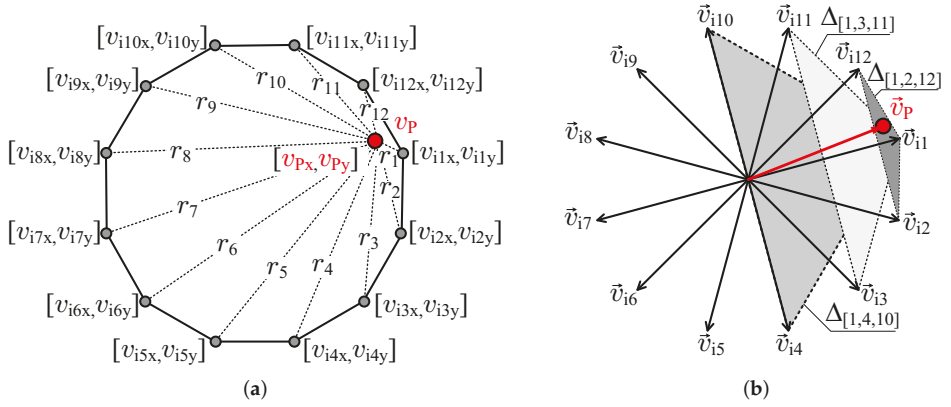


Figure 7. Synthesis field of the 12×12 matrix topology (**a**), the input voltage vectors, and an example reference output voltage $\vec{v}_{o1}$ (**b**).

One of 12 presented input vectors is referred here as the base vector. It means that the distance—defined as $r_1 \cdots r_{12}$ and shown in Figure 7b—between this vector and the reference vector $\vec{v}_{o1}$ is the smallest. There are three triangles with a common upper vertex with coordinates $\{v_{i1x}, v_{i1y}\}$: $\Delta_{[2,1,12]}$, $\Delta_{[3,1,11]}$, and $\Delta_{[4,1,10]}$. A vector $\vec{v}_{i1}$ is the base vector in this case. The given triangle $\Delta_{[p,q,r]}$ satisfies the modulation conditions when the sum

$$\Sigma_{[p,q,r]} = d_p + d_q + d_r \tag{8}$$

where

$$\begin{bmatrix} d_p \\ d_q \\ d_r \end{bmatrix} = \xi \left[\begin{bmatrix} \det \begin{bmatrix} v_{qx} - v_{o1x} & v_{qy} - v_{o1y} \\ v_{rx} - v_{o1x} & v_{ry} - v_{o1y} \end{bmatrix} \\ \det \begin{bmatrix} v_{px} - v_{o1x} & v_{py} - v_{o1y} \\ v_{rx} - v_{o1x} & v_{ry} - v_{o1y} \end{bmatrix} \\ \det \begin{bmatrix} v_{qx} - v_{o1x} & v_{qy} - v_{o1y} \\ v_{px} - v_{o1x} & v_{py} - v_{o1y} \end{bmatrix} \end{bmatrix} \right| \tag{9}$$

and

$$\xi = \left| \det \begin{bmatrix} v_{px} - v_{qx} & v_{py} - v_{qy} \\ v_{rx} - v_{qx} & v_{ry} - v_{qy} \end{bmatrix} \right|^{-1} \tag{10}$$

of PWM duty cycles d_p, d_q, and d_r takes the smallest value, ideally equal unity. When two or more triangles meet this condition, the triangle with the smallest area should be selected for further consideration. In practice, this operation can be performed by using optimized DSP functions like qsort (sorting in required order), vecmin (finding the minimum value within the set), or standard conditional operators.

When the value of transfer voltage ratio $q = V_o/V_i$ of the 12×12 topology, e.g., for CMC_P or CMC_N, is in the range

$$\frac{\cos\left(\frac{\pi}{6}\right)}{\cos\left(\frac{\pi}{12}\right)} \leq q \leq \cos\left(\frac{\pi}{12}\right) \tag{11}$$

a large number of output phases allows generating the output voltage with lower THD, therefore the cost of passive elements can be decreasing. Corresponding simulation results are presented in the further part of the text. PWM duty cycles calculation for CMC_P and CMC_N are explained in two separate subsections. While the two concepts of gating signals generation have been presented in the third subsection.

2.3. PWM Duty Cycles Calculation for CMC_P and Topology 5×5

Referred to the triangle $\Delta_{[1,2,3]}$ in Figure 6, the reference output voltage v_P is synthesized using 3 switches: h_{11}, h_{21}, and h_{31}. Taking into account previous considerations, the following formulas can be proposed for the calculation of PWM duty cycles,

$$d_{1P} = \xi_P \cdot \left|\det\begin{bmatrix} v_{i2x} - v_{Px} & v_{i2y} - v_{Py} \\ v_{i3x} - v_{Px} & v_{i3y} - v_{Py} \end{bmatrix}\right| = \frac{\Delta_{[2,P,3]}}{\Delta_{[1,2,3]}} \tag{12}$$

$$d_{3P} = \xi_P \cdot \left|\det\begin{bmatrix} v_{i1x} - v_{Px} & v_{i1y} - v_{Py} \\ v_{i2x} - v_{Px} & v_{i2y} - v_{Py} \end{bmatrix}\right| = \frac{\Delta_{[2,P,1]}}{\Delta_{[1,2,3]}} \tag{13}$$

$$d_{2P} = 1 - d_{1P} - d_{3P} = \frac{\Delta_{[3,P,1]}}{\Delta_{[1,2,3]}} \tag{14}$$

where det is the determinant of the second-order matrix, and

$$\xi_P = \left|\det\begin{bmatrix} v_{i2x} - v_{i1x} & v_{i2y} - v_{i1y} \\ v_{i3x} - v_{i1x} & v_{i3y} - v_{i1y} \end{bmatrix}\right|^{-1} \tag{15}$$

is the scaling factor, which is equal to the triangle $\Delta_{[1,2,3]}$ surface. Thus, the average value of the CMC_P output voltage can be expressed by the following formula.

$$\overline{v}_P = d_{1P} \cdot v_{i1} + d_{2P} \cdot v_{i2} + d_{3P} \cdot v_{i3} \tag{16}$$

2.4. PWM Duty Cycles Calculation for CMC_N and Topology 5×5

Referred to the triangle $\Delta_{[3,4,5]}$ in Figure 6, the reference output voltage v_N is synthesized by 3 switches: h_{31}, h_{41}, and h_{51}. The corresponded duty cycles can be calculate using the following formulas,

$$d_{3N} = \xi_N \cdot \left|\det\begin{bmatrix} v_{i4x} - v_{Nx} & v_{i4y} - v_{Ny} \\ v_{i5x} - v_{Nx} & v_{i5y} - v_{Ny} \end{bmatrix}\right| = \frac{\Delta_{[4,N,5]}}{\Delta_{[3,4,5]}} \tag{17}$$

$$d_{4N} = \xi_N \cdot \left|\det\begin{bmatrix} v_{i5x} - v_{Nx} & v_{i5y} - v_{Ny} \\ v_{i3x} - v_{Nx} & v_{i3y} - v_{Ny} \end{bmatrix}\right| = \frac{\Delta_{[5,N,3]}}{\Delta_{[3,4,5]}} \tag{18}$$

$$d_{5N} = 1 - d_{3N} - d_{4N} = \frac{\Delta_{[3,N,4]}}{\Delta_{[3,4,5]}} \tag{19}$$

where

$$\zeta_{\mathrm{N}} = \left| \det \begin{bmatrix} v_{\mathrm{i4x}} - v_{\mathrm{i3x}} & v_{\mathrm{i4y}} - v_{\mathrm{i3y}} \\ v_{\mathrm{i5x}} - v_{\mathrm{i3x}} & v_{\mathrm{i5y}} - v_{\mathrm{i3y}} \end{bmatrix} \right|^{-1} \tag{20}$$

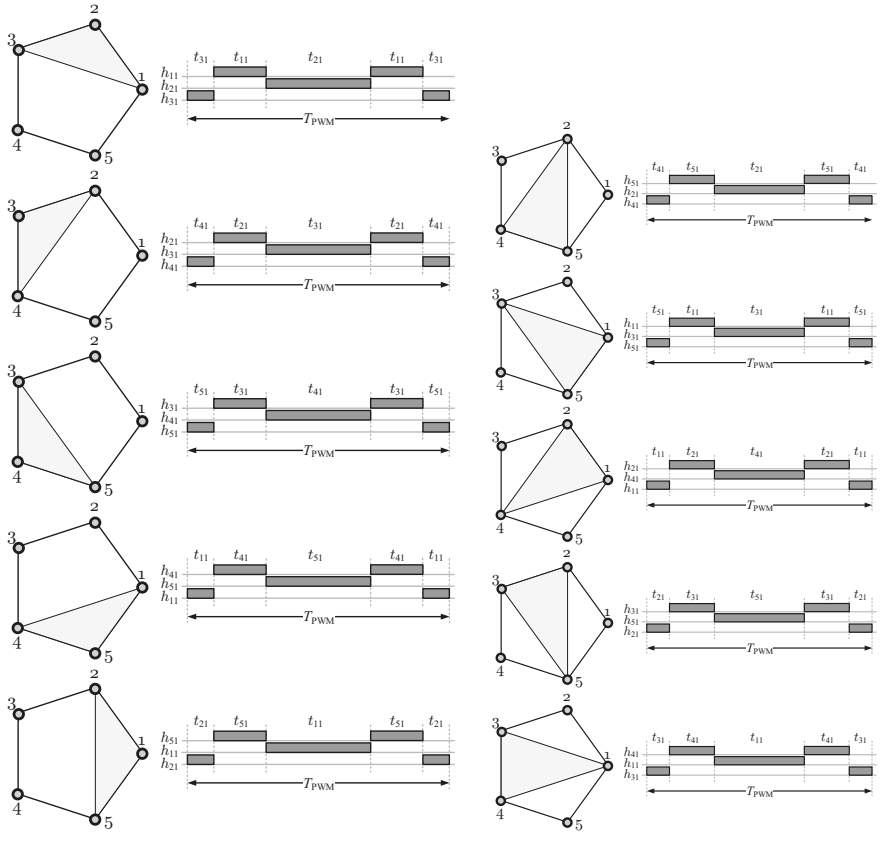
is the scaling factor, which is equal to the triangle $\Delta_{[3,4,5]}$ surface. The average value of the $\mathrm{CMC_N}$ output voltage can be expressed by the following formula

$$\overline{v}_{\mathrm{N}} = d_{3\mathrm{N}} \cdot v_{\mathrm{i3}} + d_{4\mathrm{N}} \cdot v_{\mathrm{i4}} + d_{5\mathrm{N}} \cdot v_{\mathrm{i5}} \tag{21}$$

2.5. The Concept of Gating Signals Generation

The gate signals can be controlled according to different strategies. Apap et al. [39] compared and presented several PWM signal gating methods. Among them, the cyclic Venturini and Min-Mid-Max (MMM) schemes of modulation are proposed. Two approaches have been applied to the gates signal generation: basic and mentioned MMM scheme.

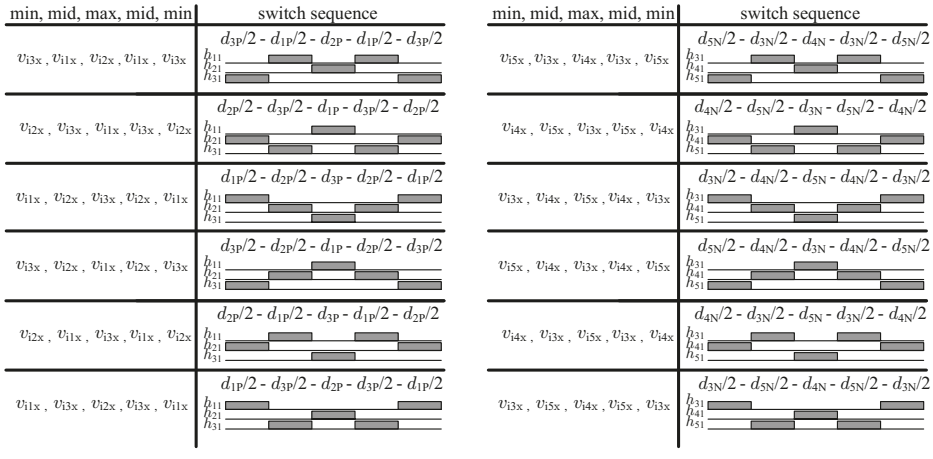
In the case of the basic solution, the sequences of the switch states always depend on the selected triangle in which the synthesis of the output voltage is realized. Therefore, these sequences can be placed in a lookup table. An overview of the basic sequences is shown in Figure 8, where the value of $\varphi \simeq 1.618$, which is so-called the golden ratio exists in the pentagon.



(a) sequences type I for $q \in \langle 1/(1+\varphi), \cos(\pi/5) \rangle$ **(b)** sequences type II for $q \in (0, 1/(1+\varphi))$

Figure 8. The switch state sequences in the basic solution of the gating signals for both converter cells CMC_P and CMC_N.

The MMM method is used to improve the quality of the voltage generated by the converter in terms of THD. The switch states sequences for the CMC_P and CMC_N converters are characterized in Figure 9. Note that these sequences correspond to the case illustrated in Figure 6b.



(**a**) for CMC_P converter (**b**) for CMC_N converter

Figure 9. The MMM type of sequences of the gating signals for both converter cells CMC_P and CMC_N for the case depicted in Figure 6c.

3. The PWM Variant 1—An Output Voltage Synthesis with Zero Value of the Common-Mode Voltage

The common-mode voltage, defined as

$$v_{cm}(t) = (v_{o1}(t) + v_{o2}(t) + v_{o3}(t) + v_{o4}(t) + v_{o5}(t))/5, \tag{22}$$

can lead to the degradation of rolling bearings in electric machines powered by PWM inverters. As indicated in the introduction an open-end windings stator fed by the double matrix converter allows for the PWM modulation without the common-mode voltage generation. The proposed approach to the load voltage synthesis with conjunction with the basic solution of the gating signals control (shown in Figure 8) give the same desired result. Elimination of the common-mode voltage can be performed by all four PWM modulation schemes: CV-CV, CCV-CCV, CV-CCV, and CCV-CV. The use of the first two cases allows obtaining an input displacement angle, which is dependent on the load parameters like in the Venturini methods [1,26].

The referenced k-output voltage vectors of the CCV-CCV modulation scheme can be expressed by following equations.

$$v_{Pxk} = q \cdot \cos(\omega_o \cdot t - ((k-1) \cdot 2\pi/5)) \tag{23}$$

$$v_{Pyk} = -q \cdot \sin(\omega_o \cdot t - ((k-1) \cdot 2\pi/5)) \tag{24}$$

$$v_{Nxk} = -q \cdot \cos(\omega_o \cdot t - ((k-1) \cdot 2\pi/5)) \tag{25}$$

$$v_{Nyk} = q \cdot \sin(\omega_o \cdot t - ((k-1) \cdot 2\pi/5)) \tag{26}$$

Above equation are proposed for the first commutation cell. Equations for the rest of the rotating vectors pairs can be represented by analogous elaboration. The referenced output voltages in CV-CV scheme can be represented by following equations.

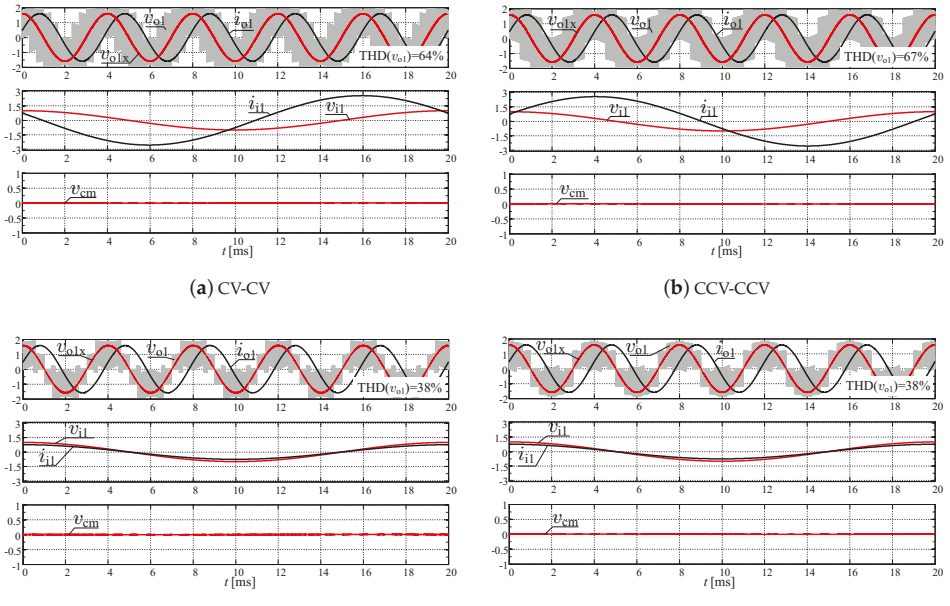
$$v_{\mathrm{P}xk} = q \cdot \cos(\omega_{\mathrm{o}} \cdot t - ((k-1) \cdot 2\pi/5)) \tag{27}$$

$$v_{\mathrm{P}yk} = q \cdot \sin(\omega_{\mathrm{o}} \cdot t - ((k-1) \cdot 2\pi/5)) \tag{28}$$

$$v_{\mathrm{N}xk} = -q \cdot \cos(\omega_{\mathrm{o}} \cdot t - ((k-1) \cdot 2\pi/5)) \tag{29}$$

$$v_{\mathrm{N}yk} = -q \cdot \sin(\omega_{\mathrm{o}} \cdot t - ((k-1) \cdot 2\pi/5)) \tag{30}$$

The possibility to change the rotation of the given output vector by changing the sign of the imaginary component allows realizing the PWM modulation, in which the resultant imaginary component of the v_{oy} takes the zero value. If vectors $\vec{v}_{\mathrm{P}}$ and $\vec{v}_{\mathrm{N}}$ rotate in opposite directions, as is typical for last two presented schemes of modulation CV-CCV and CCV-CV, the passive input current component is not generated. Simulation results of the PWM variant 1 for DSM-CMC 5 × 5 and four modulation schemes are shown in Figure 10. Simulation parameters are listed in Table A1, which can be found in an appendix.



(**a**) CV-CV (**b**) CCV-CCV

(**c**) CV-CCV (**d**) CCV-CV

Figure 10. Simulation of the PWM variant 1 for DSM-CMC 5 × 5 and four modulation schemes—RL load case.

Analogous simulation tests have been realized for the proposed converter connected to a 12-phase symmetrical power supply. Figure 11 shows the load voltage generated by DSM-CMC 12 × 12 for an output frequency equal to 10 Hz, while results obtained for 300 Hz are presented in Figure 12.

Simulation parameters for this case are available in Table A2 in Appendix A. The selection of different sets of simulation parameters did not subserve a specific purpose. The simulation tests were carried

out with the use of two independent simulation files. However, in the case of the DSM-CMC 12 × 12 simulation, a small calculation step was chosen due to the high modulation frequency. It was set to 100 kHz to get a good PWM resolution at 300 Hz of the fundamental frequency.

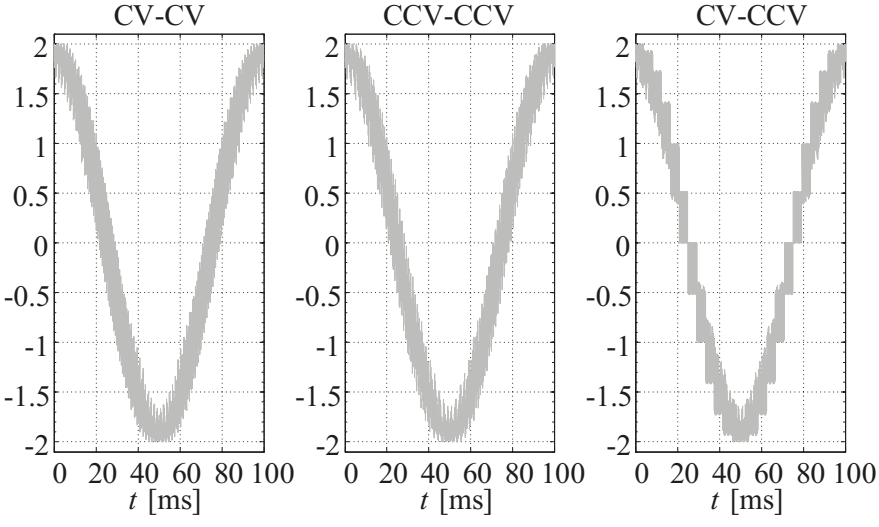


Figure 11. The load voltage v_o for DSM-CMC 12 × 12 converter for the three selected modulation schemes: $f_o = 10$ Hz, $q = 2 \times 0.95$.

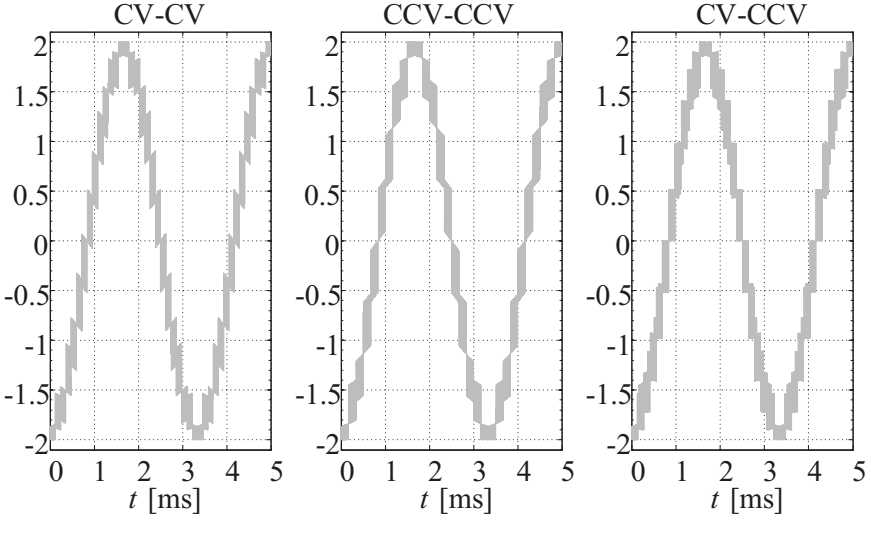


Figure 12. The load voltage v_o for DSM-CMC 12 × 12 converter for the three selected modulation schemes: $f_o = 300$ Hz, $q = 2 \times 0.95$.

Properties of this type of matrix converter, compared with counterpart 5 × 5, remains the same. In particular, the common-mode voltage is also eliminated by using the basic type of switches state sequences. The voltages shown in these figures are characterized by a low THD, which is about 12%. Comparing to the 5 × 5 topology, the resulted voltage gain for DSM-CMC is higher and takes optimally the value of 1.93.

4. The PWM Variant 2—An Output Voltage Synthesis with Less Harmonic Distortion

The basic solution of the switch states sequence has been applied in the PWM modulation with eliminating the common-mode voltage. If a lower THD of the load voltage waveform is desired, a more advanced gating signal generation mechanism can be proposed, such as MMM scheme shown in Figure 9. With regard to variant 1, this is the only change. However, the MMM method is more complicated because the input voltage vector collection should be arranged in a specific order $\{min - mid - max - mid - min\}$ within the selected triangular synthesis field. Simulation results are presented in Figure 13. A lower THD of the load voltage v_o is obtained but the common-mode voltage v_{cm} is also generated, as marked in the presented drawings.

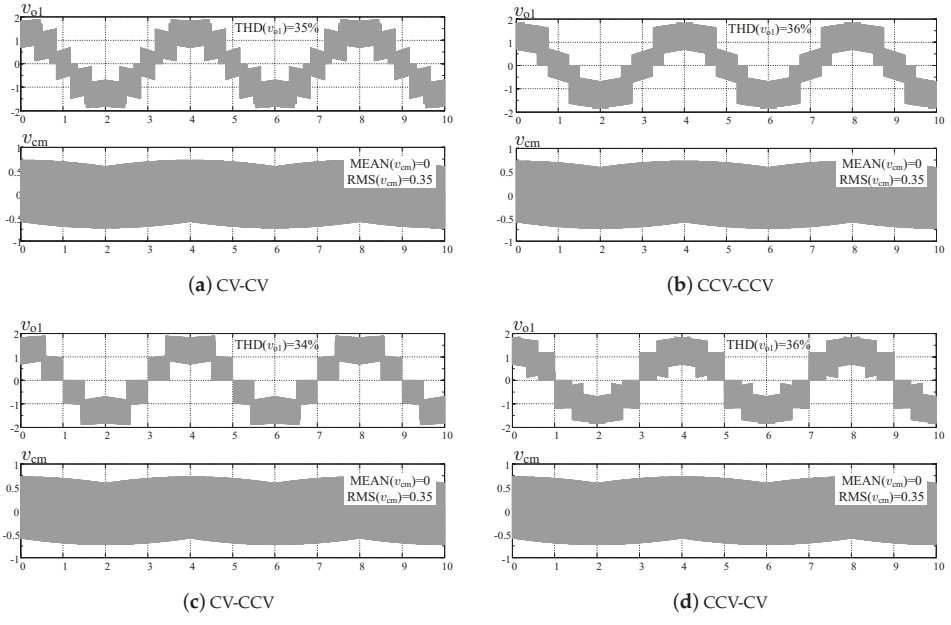


Figure 13. Simulation of the PWM variant 2 for DSM-CMC 5 × 5 and four modulation schemes: $f_o = 250$ Hz, $q = 2 \times 0.8$.

5. The PWM Variant 3—An Output Voltage Synthesis with Maximum Voltage Transfer Ratio and Minimum Number of Switching

A synthesis field for multi-phase and symmetrical AC voltage sources can be represented by a regular polygon as shown in Figures 6b and 7a. A radius of a circle inscribed of this polygon limits an output voltage amplitude in the linear range of modulation. The maximum voltage transfer ratio for CMC_N

and CMC_P, related to the input voltage amplitude and number of inputs equal to n, can be expressed as follows,

$$q_{P\max} = q_{N\max} = \cos(\pi/n) \tag{31}$$

Therefore, the maximum load voltage for DSM-CMC 5 × 5 in $p.u.$ is equal to

$$v_{o\max} = 2 \cdot \cos(\pi/5) = 1.618 \tag{32}$$

The value (32) can be increased by modifying the position of the v_P and v_N vectors. In contrast to the methods described in the previous sections, trajectories of these vectors are not a circle. The locus of each vector is not changing smoothly and contains discontinuities. This type of modulation belongs to the discontinuous group of PWM modulations. Both reference vectors v_P and v_N take exactly five positions, in which they lie on one of five input vectors. An algorithm flowchart for DSM-CMC 5 × 5 is presented in Figure 14.

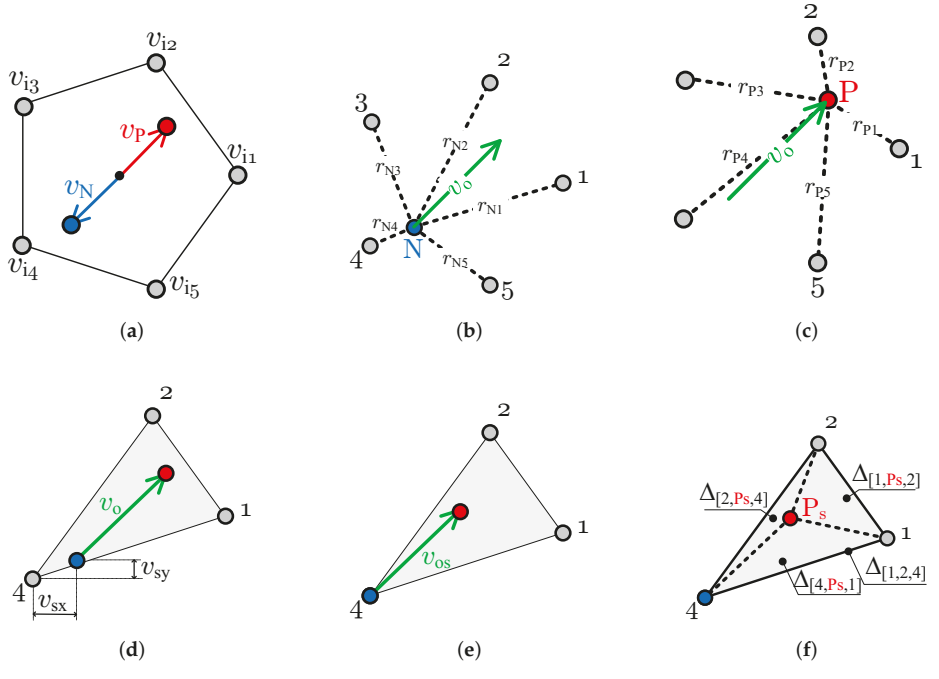
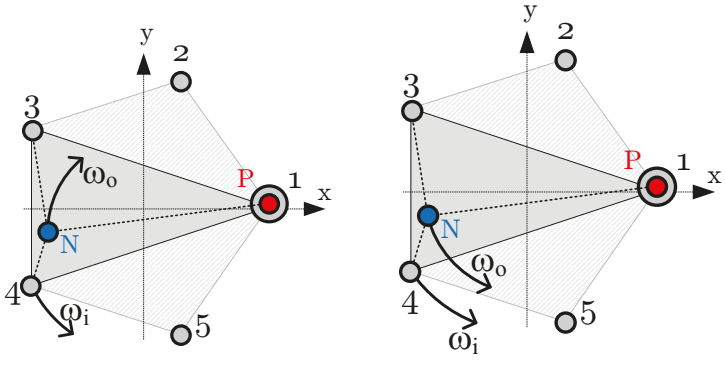


Figure 14. An algorithm flowchart of the variant 3 PWM modulation: (**a**) Step 1: generation of synthesis field and reference voltage vectors v_P and v_N. (**b**) Step 2: calculation of the set of distances between the N point and vertices of the synthesis field. (**c**) Step 3: calculation of the set of distances between the P point and vertices of the synthesis field. (**d**) Step 4: shortest distance selection, setting the origin vertex, and the vector's offset $\{v_{sx}, v_{sy}\}$ calculation. (**e**) Step 5: the reference vector v_o shift resulting in the new coordinates of P and N points. (**f**) Step 6: calculation of four areas of the triangle and PWM duty cycles.

The output voltage synthesis field is generated using the DSOGI blocks at the first step of the proposed algorithm. The reference output voltage vectors coordinates, $\{v_{Nx}, v_{Ny}\}$ and $\{v_{Px}, v_{Py}\}$, are also calculated

at this step. The vectors can rotate clockwise (CV-CV scheme) or counterclockwise (CCV-CCV scheme), as shown in Figure 15.



(**a**) CV-CV (**b**) CCV-CCV

Figure 15. An example rotation of the reference output vector.

Based on the analysis of the vector arrangement in Figure 15, it can be written that the maximum length of the voltage vector, in a linear range of modulation, is equal to the following expression.

$$v_{\mathrm{o\,max\,(variant3)}} = 1 + \cos(\pi/5) = 1.809 \tag{33}$$

However, a vector of this length has to be accordingly shifted inside the synthesis field as shown in Figure 14d,e. Therefore, new coordinates of the reference output vector for the given commutation cell can be calculated as follows.

$$v_{\mathrm{osx}} = v_{\mathrm{ox}} + v_{\mathrm{sx}} \tag{34}$$

$$v_{\mathrm{osy}} = v_{\mathrm{oy}} + v_{\mathrm{sy}} \tag{35}$$

Distances between N-point and all the synthesis field vertices are calculated in Step 2. The same procedure is applied for the point P in Step 3. Next, the shortest calculated distance in a N-collection $\{r_{\mathrm{N1}}, r_{\mathrm{N2}}, r_{\mathrm{N3}}, r_{\mathrm{N4}}, r_{\mathrm{N5}}\}$ is compared with the shortest calculated distance in a P-collection $\{r_{\mathrm{P1}}, r_{\mathrm{P2}}, r_{\mathrm{P3}}, r_{\mathrm{P4}}, r_{\mathrm{P5}}\}$. Finally, the less value is selected, which correctly indicates the optimal vertex of the synthesis field. The shift coordinates are calculated in Step 4. As can be seen in Figure 14d, vertex number 4 has been chosen. Thus, the PWM duty cycles, for the case illustrated in Figure 14f can be calculated using the following formulas.

$$d_{\mathrm{1Ps}} = \Delta_{[\mathrm{2,Ps,4}]} / \Delta_{[\mathrm{1,2,4}]} \tag{36}$$

$$d_{\mathrm{2Ps}} = \Delta_{[\mathrm{4,Ps,1}]} / \Delta_{[\mathrm{1,2,4}]} \tag{37}$$

$$d_{\mathrm{4Ps}} = \Delta_{[\mathrm{1,Ps,2}]} / \Delta_{[\mathrm{1,2,4}]} \tag{38}$$

and

$$d_{\mathrm{4Ns}} \equiv 1 \tag{39}$$

Formula (39) refers to the case where the end of the v_{N} vector coincides with the v_{i4} vector. It means the permanent connection of the input voltage v_{i4} with one side of the load phase during the PWM

modulation period. Figure 15 shows a case, which in the one side of the load is permanently connected to an input voltage v_{i1} during PWM modulation. Sequences of the switch states shown in Figure 16 correspond to the case, which in the s_N switch is connected permanently to the input phase 4. The zero load voltage is generated by using the same switch in both CMC_P and CMC_N matrix converters. Simulation results for maximal voltage transfer ratio (33) are shown in Figure 17. The common-mode voltage v_{cm} is eliminated. An application of the CV-CV and CCV-CCV scheme of modulation resulting in the non-zero input displacement angle.

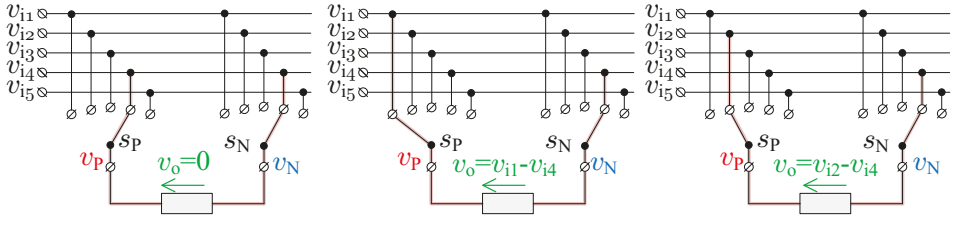
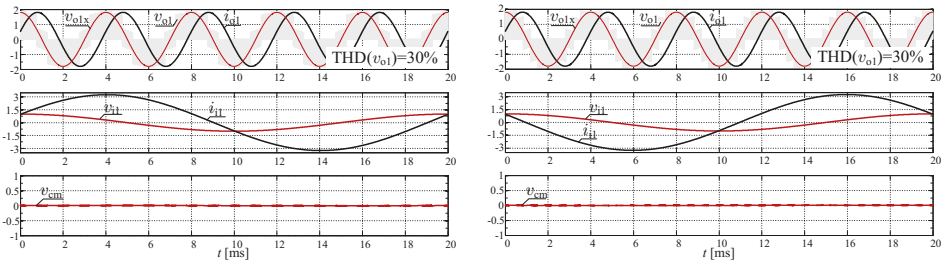


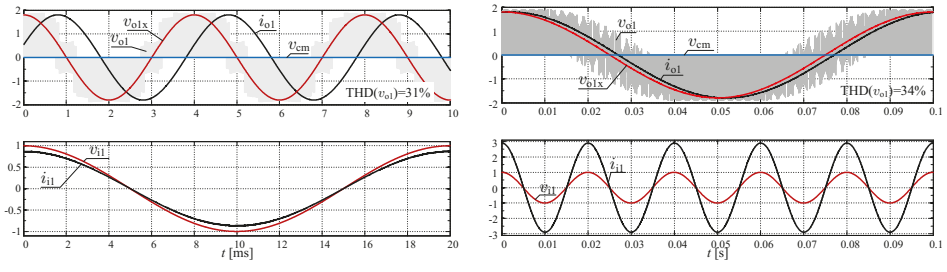
Figure 16. Sequences of the switch states in one commutation cell for the case presented in Figure 14.



(**a**) CCV-CCV (**b**) CV-CV

Figure 17. Simulation of the PWM variant 3 for DSM-CMC 5 × 5 and two modulation schemes: $f_o = 250$ Hz, $q = 1.8$.

Having half the number of switching operations during the PWM modulation period is an advantage of variant 3. In order to obtain the unity power factor at the system input, the sequence types have to be toggled continuously in the order CV-CV, CCV-CCV,..., etc. However, this mode of operation may require to redesign of an input filter. Example simulation results of the PWM variant 3 with toggling mode for DSM-CMC 5 × 5 have been presented in Figure 18.



(**a**) $f_o = 250$ Hz, $q = 1.8$ (**b**) $f_o = 10$ Hz, $q = 1.8$

Figure 18. Simulation of the PWM variant 3 with toggling mode for DSM-CMC5 × 5.

6. Summary and Conclusions

This paper presents a new approach to the PWM modulation for the multi-phase matrix converters supplying loads with open-end winding. The proposed approach is an alternative for the methods based on the space-vector modulation. Three variants of PWM modulation were presented. Animations for the first two of them (Figures S1 and S2) are available in Supplementary Materials. The first variant allows for eliminating the common-mode voltage, which is a desired feature from a practical point of view. The second variant based on a specific rearranging switches state sequences can offer quasimultilevel waveforms with low THD. However, a common-mode voltage level can be unaccepted due to influence on the bearings lifetime. Variant 3 of the PWM modulation described in a paper offer over 12% greater voltage transfer gain. Comparison of an input angle value for the proposed variants of PWM modulation is presented in Table 1.

Table 1. Comparison of an input angle value for the proposed variants of PWM modulation.

PWM Variant	Modulation Scheme		
	$\phi_i = \varphi_o$	$\phi_i = -\varphi_o$	$\phi_i = 0$
variant 1	CCV-CCV	CV-CV	CV-CCV or CCV-CV
variant 2	CCV-CCV	CV-CV	CV-CCV or CCV-CV
variant 3	CCV-CCV	CV-CV	toggling

The multi-phase matrix converters, with an equal number of input and outputs, belong to the niche solution. Recently, we can observe an increasing interest in multi-phase systems. Furthermore, the complexity of the modulation algorithms grows up. The described proposal is a research result of analytic signal and an application of the smooth interpolation method in PWM duty cycle computing. Some selected features and properties have been compared with the space-vector method. Table 2 presents such a comparison. The PWM duty cycle computation represented by equations, from (12) to (14), is performed using only a second-order determinant of the voltages coordinate matrix without trigonometry usage. Therefore, the proposed method also naturally extends the applicability of the formulas to unbalanced and distorted AC voltage sources. Moreover, all computation can be realized in the FPGA structure using the simple multipliers and adders. The important contribution of the presented article is a presentation of the novel algorithm, which is much easier than algorithms based on the space-vector approach. This property is essential in multi-phase systems because the number of vectors is very high. The proposed solution uses only vectors that represent the Hilbert analytic signal pair calculated for the input and the reference

vectors. The number of vectors needed to realize the output voltage synthesis is equal to only the sum of input and output phases.

Table 2. The comparison of the proposed modulation with the space-vector approach.

	Proposed Modulation	**Space Vector Modulation**
how the vector map is generated	using the analytic signal concept, which is based on the Hilbert transform	using the Clark transform for multi-phase systems
the difficulty of the vector map generator	comparable with SVPWM, using several methods: triple Clarke, or DSOGI, or DFT	comparable with the proposed, using the Clarke rotation operator
degree of difficulty with more phases	the number of vectors is equal to the number of converter's terminals	the number of vectors is equal to $2^{(2P)}$, where P is the number of the load phase
the common-mode voltage elimination in the multi-phase systems	yes	requires the modification of the modulation using the rotating vectors collection
minimization of the number of switching	possible for variant no. 3, in the general case a sorted and optimized the switch states sequence should be used	the minimization of the number of switching is a natural feature for the space-vector modulation, which is based on the nearest three vectors, however—for that selection can be an additional issue of computation
is it applicable for unbalanced and asymmetrical loads with the open-winding	yes	no applicable, space-vector methods assumed the symmetric loads with the open-winding
the load phase failure	ready for that failure, each load phase is controlled by an individual and independence the cell controller	in the event of the sudden change in the number of load phases, the algorithm (switches' state sequences table) must be thoroughly rebuilt, it is not possible in a real-time system, the modification can only be implemented offline
application of trigonometric functions for PWM duty cycle computing	no (it speeds up the algorithm)	yes

Supplementary Materials: The following are available at http://www.mdpi.com/1996-1073/14/2/466/s1, Supplementary data: Matlab script m-file: energies_1056291_Supplementary_Materials.m, Figure S1: A New Approach to the PWM Modulation for the Multiphase Matrix Converters Supplying Loads with Open-End Winding: two rotating the reference vectors, Figure S2: A New Approach to the PWM Modulation for the Multiphase Matrix Converters Supplying Loads with Open-EndWinding: the input and the output waveforms obtained, and the PWM duty cycles.

Author Contributions: The concept, algorithmization, simulation studies, P.S.; simulation results verification and presubmission editing, E.R.-C. and N.S. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the LINTE^2 Laboratory, Gdansk University of Technology.

Conflicts of Interest: All authors declare no conflict of interest.

Appendix A. Simulation Parameters

Table A1. Simulation parameters for DSM-CMC 5 × 5.

Parameter	**Value**
Number of input voltages	5
Number of output voltages	10
Number of an ideal bidirectional switches	50
Source phase voltage amplitude	$V_i = 100$ V
Input frequency	$f_i = 50$ Hz
Output frequencies	$f_o = 10$ Hz, 250 Hz
Voltage gain of CMC_P	$q = 0.8$
Voltage gain of CMC_N	$q = 0.8$
The load parameters	$R_o = 0.5\ \Omega$, $L_o = 1$ mH
An algorithm frequency	$f_s = 10$ kHz
Simulation step	250 ns
Simulation software	PSIM 64-bit Version 11.0.3

Table A2. Simulation parameters for DSM-CMC 12 × 12.

Parameter	Value
Number of input voltages	12
Number of output voltages	24
Number of an ideal bidirectional switches	288
Source phase voltage amplitude	$V_i = 100$ V
Input frequency	$f_i = 50$ Hz
Output frequencies	$f_o = 10$ Hz, 300 Hz
Voltage gain of CMC_P	$q = 0.95$
Voltage gain of CMC_N	$q = 0.95$
The load parameters	$R_o = 10\ \Omega$, $L_o = 0.1$ mH
An algorithm frequency	$f_s = 100$ kHz
Simulation step	100 ns
Simulation software	PSIM 64–bit Version 11.0.3

Simulation research has been performed for symmetric and balanced source and load. Obtained currents and voltages have been presented as $p.u.$ values referred to the base voltage $V_{\text{base}} = V_{\text{i}}$ and the base current equal to $I_{\text{base}} = V_{\text{i}}/Z_{\text{o}}$, where Z_{o} was a load impedance.

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Application of Grasshopper Optimization Algorithm for Selective Harmonics Elimination in Low-Frequency Voltage Source Inverter

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Received: 28 October 2020; Accepted: 2 December 2020; Published: 4 December 2020

Abstract: In this paper, an application of the recently developed Grasshopper Optimization Algorithm (GOA) for calculation of switching angles for Selective Harmonic Elimination (SHE) PWM in low-frequency voltage source inverter is proposed. The algorithm is based on insect behavior in the food foraging swarm of grasshoppers. The characteristic feature of GOA is the movement of agents is based on the position of all agents in the swarm. This method represents a higher probability of convergence than Particle Swarm Optimization (PSO) Modifications of GOA have been examined regarding their effect on the algorithm's convergence. The proposed modifications were based on the following techniques: Grey Wolf Optimizer (GWO), Natural Selection (NS), Adaptive Grasshopper Optimization Algorithm (AGOA), and Opposite Based Learning (OBL). The performance of GOA and its modifications were compared with well-known PSO. Areas, where GOA is superior to PSO in terms of probability of convergence, have been shown. The efficiency of the GOA algorithm applied for solving the SHE problem was confirmed by measurements in the laboratory.

Keywords: grasshopper optimization algorithm (GOA); particle swarm optimization (PSO); voltage source inverter (VSI); selective harmonics elimination PWM (SHEPWM)

1. Introduction

The Selective Harmonic Elimination (SHE) and Selective Harmonic Mitigation (SHM) [1,2] has been described for the first time in the 1960s in [3] and disseminated by Patel and Hoft [4,5]. Since that time SHE has been introduced in a number of industrial applications where power electronics was proposed [6]. The challenge is progress in the development of techniques for solving SHE/SHM non-linear transcendental equations

Since the early days, iterative techniques such as Newton–Raphson (N–R) [4,5], Gauss–Newton have been employed to solve these equations. The convergence of these methods depends on the initial guess, which is a complex problem and in many cases is not successful. This disadvantage encourages researchers to develop more effective techniques. Thus, Chaison et al. in [7] proposed the method based on the conversion of transcendental equations into an equivalent set of polynomials. The high degree of polynomial requires specialized software to compute it. The combination of Groebner's bases and symmetric polynomials was applied to solve the mentioned polynomials [8]. However, it generates ambiguous solutions which make it less useful. The main disadvantage of iterative techniques is they do not find an optimum solution.

The development of evolutionary algorithms opens new opportunities in the field of solving SHE equations [9]. These algorithms present numerous benefits such as independence from an initial guess, utilization of simple algebra, lower computational costs, formulation of multi-constrained problems.

One of the most popular evolutionary algorithms is Particle Swarm Optimization (PSO) proposed for finding switching angles for PWM VSI inverter to eliminate low order voltage harmonic [10] and to optimize dc-link current harmonics [11]. The application of numerous algorithms are proposed for SHE in the literature: Imperial Colonial Algorithm (ICA) [12], Genetic Algorithm [13], Ant Colony Algorithm [14], bee optimization technique (BA) [15], Bacterial Foraging Algorithm [16], Firefly Algorithm (FA) [17], Shuffled Frog Leaping (SFL) algorithm [18], Backtracking Search Algorithm (BSA) and Differential Search Algorithm (DSA) [9], Whale Optimization Algorithm (WOA) [19]. The use of the Grasshopper Optimization Algorithm (GOA) for SHE has not been studied so far.

The GOA is an algorithm recently developed and introduced by Saremi et al. [20] in 2017. In recent two years, the GOA gained great attention in many research fields due to its high efficiency of solving a different kind of optimization problems. It was tested for constrained and unconstrained test functions with promising results [21]. The GOA was proposed for solving multi-objective optimization problems [22] modified by the application of Opposition-Based Learning (OBL) [23]. Modifications of GOA to improve its performance are has been developed and studied: Adaptive GOA (AGOA), Grey Wolf Optimizer (GWO) and Natural Selection (NS) [24], Gaussian mutation, and Leavy- flight strategy [25].

The efficiency of GOA has been compared with existing evolutionary algorithms utilized for different optimization problems. In [26] GOA adaptation for energy loss reduction and voltage stability factor was proposed and compared with PSO, Gravitational Search Algorithm (GSA), and Artificial Bee Colony (BA) algorithms. In [27], the comparison of GOA with PSO and WOA (Wale Optimization Algorithm) was used to optimize the PI controller parameters in the microgrid. Since the first presentation, GOA has found its implementation in numerous industrial applications such as optimization of the parameters of proton membrane fuel cells (PEMFC) [28], the stability of microgrid applications [29] and energy management [30], medicine [31], the technology of image processing [32], and financial issues [25] as well.

In this paper, the recently developed GOA is applied to eliminate low-order voltage harmonics (5th, 7th, 11th, and 13th) in low-frequency VSI based drive. The hypothesis to prove is that GOA represents a higher probability of convergence than PSO applied for SHE problem with similar computation effort. Results for GOA and modified GOA are compared with PSO. The main criterion of comparison is the probability of convergence. The following modification of GOA are examined: Natural Selection (NS), Adaptive GOA (AGOA), Opposite Based Learning (OBL), and Grey Wolf Optimizer (GWO). Experimental results are presented to validate simulation analysis.

The rapid development of controllers for high and medium power converters provides an opportunity for the application of modulation techniques; a decade ago, they used to be known as difficult to use. This type of modulation is SHE-PWM. When it was invented its applicability was very low and nowadays it competes with the most advanced and popular modulations [33]. Its application is studied for grid connectors [34] and railway vehicles [35] as well. Moreover, the separation of a modulator from the controller brings the possibility of implementation of the SHE-PWM with space vector modulation (SVPWM) [36]. Authors of this paper claim that for railway vehicles the most efficient is hybrid modulation studied in [37] where SHE-PWM and SVPWM are used interchangeably and the choice depends on the operating conditions. This solution is the most reasonable and allows to utilize the advantages of both techniques: dynamics of SVPWM and harmonics control of SHE-PWM.

The attention focused on SHE-PWM stimulates research towards increment of efficiency in the calculation of switching angles. In [38] the comprehensive review of SHE-PWM focused on various aspects, is presented. One of the mentioned aspects is the utilization of optimization-based techniques for solving SHE equations and they were divided into four groups: Genetic Algorithms (GA) Particle Swarm Optimization (PSO) Differential Evolution (DE) and Hybrid. According to the "no free lunch" theorem applied to the bio-inspired optimization algorithms [39], there is the most suitable solver for a specific optimization task. Solving SHE equations developed for voltage source inverter is a task of variable complexity that depends on assumptions like the number of switching angles, modulation

index, dead times between switching, switching frequency, and others. Thus, there is a possibility that for different optimization region different algorithm is most suitable. Thus, every recently developed algorithm should be evaluated towards application for solving SHE-PWM equations. In this paper, the authors present the study for the application of the GOA algorithm. The novelty of this study is proof that there is a range of SHE problems where the GOA algorithm gives a higher possibility of convergence with lower computational effort than widely used and appreciated PSO. Results presented in this paper encourage further research to discover the full potential of the GOA algorithm regarding the presented problem by comparing it with a wider representation of bio-inspired algorithms.

The problem undertaken in the study is considered as a single criteria optimization problem. SHE problem could be considered as a multi-objective optimization problem as each harmonic value as a function of optimization variables could be considered as a separate objective function. However, all considered harmonics in the problem of SHE should be eliminated for the same optimization variables, therefore the desirable optimization solution is a utopian solution from the point of view of the multi-optimization approach [40]. Accordingly, the optimization functions have been aggregated to a single optimization variable by means of the dedicated relationship proposed in the article.

2. VSI Model with SHE Control

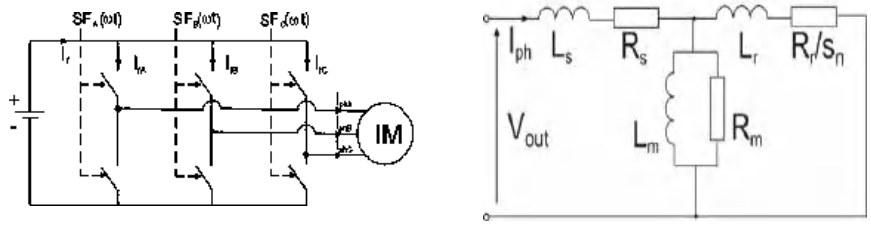
2.1. Drive's Parameters

The main goal of this work is to study the convergence of GOA applied for the calculation of switching angles for SHE-PWM for a low-frequency VSI drive with an induction motor. Therefore, to prove the validity of results obtained by the examined algorithm, the VSI drive was modeled in MATBAL/SIMULINK and verified in the laboratory. Parameters of utilized induction motor for experiments are presented in Table 1.

Table 1. Parameters of drive's mode.

Symbol	Parameter	Value
P_n	Rated power	2, 5 kW
I_n	Rated phase current	3.9 A
V_n	Rated voltage rms	230/400 V
-	Winding's connection	star
n_n	Rated rotation speed	1465 rpm
L_s	Stator's leakage inductance	0.0108 H
R_s	Stator's resistance	2.8465 Ω
L_r	Rotor's leakage inductance	0.0106 H
R_r	Rotor's resistance	2.7359 Ω
L_m	Core losses inductance	0.27597 H
R_{m_n}	Core losses resistance	1231 Ω

Figure 1a. illustrates the topology of the VSI utilized for the purpose of this work. Figure 1b shows an equivalent circuit of a single phase of the motor applied in the SIMULINK model. Inverter's transistors were controlled by binary switching function ($SF(\omega t)$) formed by switching angles (α) defined as angular "moments" of transistors state change (Figure 2). Switching angles are delivered by solving equations presented in this section.



(**a**) (**b**)

Figure 1. Analytical schema of the considered 3 phase 2-level inverter with load (IM—Model of an induction motor) (**a**) inverter schema (**b**) equivalent circuit of one phase of induction motor (sn—Slip for n-th harmonic).

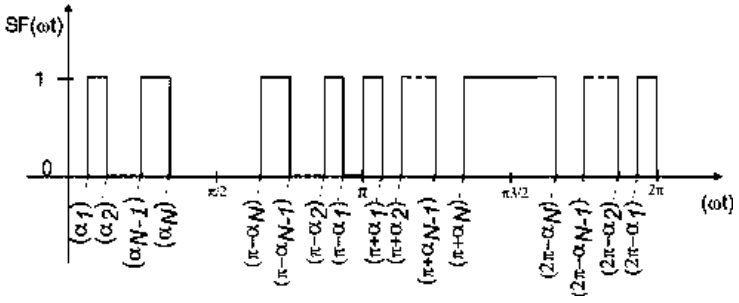


Figure 2. Waveform of switching function SF with quarter-wave symmetry and N switching angles.

2.2. SHE-PWM

In the great number of cases of SHE-PWM application, it is used in electric drives to eliminate low order harmonics, while amplitudes of high order harmonics are reduced by input filters. SHE equations are based on the Fourier series expansion of the inverter output voltage waveform:

$$V(\omega t) = a_0 + \sum_{n=1}^{\infty} [a_n sin(n\omega t) + b_n cos(n\omega t)] \tag{1}$$

where ω is an angular frequency of fundamental component, *n* is a harmonic order, and an, bn are Fourier coefficients. For quarter-wave symmetry, only coefficient an for the odd *n* coefficient represents the non-zero value:

$$a_n = \begin{cases} \frac{4U_{DC}}{n\pi}\left[-1 - 2\sum_{i=1}^{N}\left(-1\right)^i cos(n \cdot \alpha_i)\right] & ; \quad for\ odd\ n \\ 0 & ; \quad for\ even \quad n \end{cases} \tag{2}$$

$$b_n = \begin{cases} 0 \ ; \ for\ odd\ n \\ 0 \ ; \ for\ even \ \ n \end{cases} \tag{3}$$

where U_{DC} is DC-link voltage and *n* is the number of switching angles per a quarter-period. In this paper, fluctuation and ripplers of DC-link voltage were not of concern.

Assuming the odd quarter-wave symmetry of inverter output voltage, triple harmonics are canceled. The symmetry of the system brings cancelation of even harmonics as well. For $n = 5$

switching angles in quarter-period, 5 non-linear equations can be formulated (4) to satisfy fundamental component (*V1*) and eliminate 5th, 7th, 11th, and 13th harmonics:

$$\begin{cases} \frac{4}{\pi}[-1+2\cos(\alpha_1)-2\cos(\alpha_2)+2\cos(\alpha_3)-\ldots \\ \quad \ldots 2\cos(\alpha_4)+\ 2\cos(\alpha_5)] = M1 \\ \frac{4}{5\pi}[-1+2\cos(5\alpha_1)-2\cos(5\alpha_2)+2\cos(5\alpha_3)-\ldots \\ \quad \ldots 2\cos(5\alpha_4)+\ 2\cos(5\alpha_5)] = 0 \\ \frac{4}{7\pi}[-1+2\cos(7\alpha_1)-2\cos(7\alpha_2)+2\cos(7\alpha_3)-\ldots \\ \quad \ldots 2\cos(7\alpha_4)+\ 2\cos(7\alpha_5)] = 0 \\ \frac{4}{11\pi}[-1+2\cos(11\alpha_1)-2\cos(11\alpha_2)+2\cos(11\alpha_3)-\ldots \\ \quad \ldots 2\cos(11\alpha_4)+\ 2\cos(11\alpha_5)] = 0 \\ \frac{4}{13\pi}[-1+2\cos(13\alpha_1)-2\cos(13\alpha_2)+2\cos(13\alpha_3)\ -\ldots \\ \quad \ldots 2\cos(13\alpha_4)+2\cos(13\alpha_5)] = 0 \end{cases} \tag{4}$$

where *M*1 is for modulation index:

$$V_1 = M1\ \frac{U_{DC}}{2}\ ; \quad for\ M1\langle 0,\ \frac{4}{\pi}\rangle \tag{5}$$

In this case the fundamental voltage component (*V1*) is defined as the amplitude of phase voltage of the motor in the star connection of the windings. The main goal of this paper is to adopt GOA for solving Equation (4) to determine switching angles for SHE-PWM end examine its convergence.

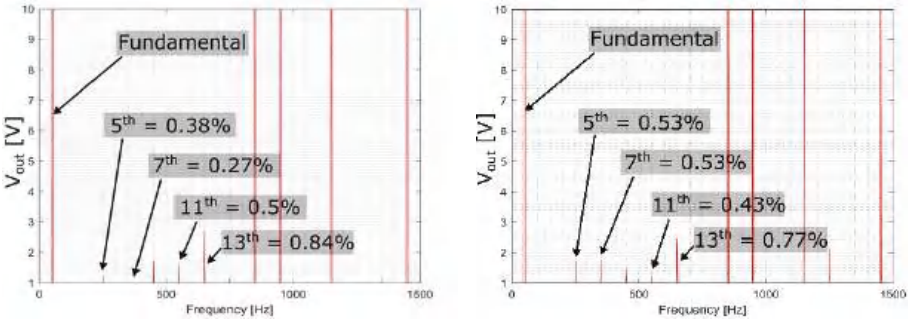
3. Formulation of The Optimization Problem

To solve SHE Equation (4) using an optimization algorithm, the fitness function must be formulated. For $n = 5$ switching angles and four harmonics eliminated the fitness function is described by following equation with constraints:

$$\begin{aligned} &Minimize,\ f_{fit}(\alpha_1,\alpha_2,\alpha_3,\alpha_4,\alpha_5) \\ &\qquad = \sigma_1 \cdot\left(V_1 - V_1^*\right)^2 + \sigma_5{\cdot}(V_5)^2\ + \sigma_7{\cdot}(V_7)^2\ + \sigma_{11}{\cdot}(V_{11})^2\ + \sigma_{13}{\cdot}(V_{13})^2 \\ &\qquad\qquad \text{subject to}:\ 0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \frac{\pi}{2} \end{aligned} \tag{6}$$

where: V_1, V_5, V_7, V_{11}, V_{13} are fundamental component and 5th, 7th, 11th and 13th voltage harmonics (p.u.) respectively, σ_x are penalty weights for the optimization process.

Thus, the aim is to apply an optimization algorithm to minimize fitness function (6) to achieve declared fundamental component (V_1^*) and harmonics elimination. The fundamental component is minimized with the highest weigh (penalty value) that equals $\sigma_1 = 100$. Thus, every 1% of difference between an actual value and the desired one will increase fitness function by 100. Harmonics are minimized with penalty weight $\sigma_5 = \ \sigma_7 = \sigma_{11} = \sigma_{12} = 10$ One of the essential assumptions of every optimization algorithm is the STOP criterion based on the maximum number of iterations and the minimum value of the fitness function. In this paper, the minimum value of the fitness function assumed to be the success is $f_{fit\_STOP} = 0.0001$. Regarding the necessity of implementation of dead-times in industrial applications (in this paper dt = 5×10^{-6} s), a lower value of the fitness function will not be recognized as higher quality performance. To prove this statement, sample results obtained by GOA with tolerance 1×10^{-3} (Figure 3a) were compared with the results obtained with tolerance 1×10^{-10} (Figure 3b). Figure 3 shows that decreasing the parameter of tolerance does not guarantee better efficiency of eliminated harmonics, only significantly increases computation time. Thus, tolerance 1×10^{-3} was assumed to be sufficient. More results will be presented in Section 5.



(**a**) (**b**)

Figure 3. Simulated output voltage spectrum for SHE-SPWM carried out using Grasshopper Optimization Algorithm (GOA) for different tolerance: (**a**) tolerance < 1×10^{-4}; M1 = 1.0; x = (0.1234; 0.4242; 0.5199; 1.2197; 1.2791); (**b**) tolerance < 1×10^{-10}; M1 = 1.0; x = (0.1225; 0.4259; 0.5206; 1.2186; 1.2783)

4. Grasshopper Optimization Algorithm (GOA)

GOA was developed and introduced by Saremi, Mirjalili, and Lewis in [20]. The first proposed application was for structural optimization to find the optimal shape of a three-bar truss, a 52-bar truss, and a Cantilever beam. In this paper, the authors present the application of GOA to solve SHE equations. The proposed algorithm mathematically models the behavior of grasshopper swarm foraging for food to survive. Their individual behavior and social interactions lead the swarm to the optimal solution. The mathematical model of grasshopper behavior is based on a formula for the position of each grasshopper described by the following equation:

$$X_i = S_i + G_i + A_i \tag{7}$$

where X_i is the position of the i-th grasshopper, S_i is the social interaction between agents in the swarm, G_i is the gravity force acting on the i-th grasshopper, and A_i models the wind effect. However, due to specifics of the problems analyzed in this work effect of gravity and wind were omitted. Thus, only social interactions were taken into account.

$$S_i = \sum_{\substack{j=1 \\ j \neq i}}^{Np} s\left(d_{ij}^*\right) \cdot \vec{d}_{ij} \tag{8}$$

where d_{ij}^* is the normalized distance between the i-th and j-th grasshopper, $s(d_{ij}^*)$ is the function of social forces and $\vec{d}_{ij}$ is an unitary vector from i-th to j-th grasshopper.

If absolute value of the distance between the i-th and j-th agent is formulated as:

$$d_{ij} = \left| x_i - x_j \right| \tag{9}$$

thus, the normalized value is defined as

$$d_{ij}^* = 2 + rem\left(d_{ij}, 2\right) \tag{10}$$

where $rem\left(d_{ij}, 2\right)$ is the remainder after division of d_{ij} by 2. Distance normalization allows for the value of the distance to be kept close to the value of 2 what gives the best effect with the *s-function*. Unitary vector $\vec{d_{ij}}$ is defined with the following correlation:

$$\begin{cases} \vec{d_{ij}} = 1;\ for\ x_i - x_j > 0 \\ \vec{d_{ij}} = -1;\ for\ x_i - x_j \leq 0 \end{cases} \tag{11}$$

Thus, $\vec{d_{ij}}$ can be defined by the following formula:

$$\vec{d_{ij}} = \frac{x_i - x_j}{\left|x_i - x_j\right|} \tag{12}$$

A characteristic feature of GOA is a comfort zone shrinking with the iteration number. The Comfort zone is the circle around the best agent. Inside the comfort zone, other agents are being repulsed from the leader and outside the comfort zone, they are being attracted to it. This behavior keeps a balance between exploration and exploitation. The decreasing coefficient c models variation of the comfort zone by changing value typically from 1 to some small number. Regarding the above considerations, Equation (7) for the d-dimensional problem can be expanded as follows:

$$X_i^d = c\left(\sum_{\substack{j=1 \\ j \neq i}}^{Np} c \cdot \frac{ub^d - lb^d}{2} s\left(d_{ij}^{d*}\right) \frac{x_i^d - x_j^d}{\left|x_i^d - x_j^d\right|} \right) + Gbest^d \tag{13}$$

where ub^d is for upper bound of the *d-th* dimension, lb^d is for lower bound of the *d-th* dimension, $Gbest^d$ is for the global best result in the *d-th* dimension, s is for *s—Function* which describes the strength of the interaction between agents and is formulated with the following formula:

$$s\left(d_{ij}^{d*}\right) = F \cdot e^{\left(-\frac{d_{ij}^*}{L}\right)} - e^{\left(-d_{ij}^*\right)} \tag{14}$$

where F and L are coefficients with suggested values 0.5 and 1.5 respectively. Variation of these coefficients will be analyzed in further sections, regarding its influence on the probability of convergence of the algorithm.

Equation (13) reveals the most significant rule of GOA. The position of agents in every iteration is determined with respect to the position of all other agents in the swarm. For instance, in the PSO algorithm position of agents is determined regarding only two vectors: personal best and global best position. That is the reason why GOA requires a lower population to keep the same computational effort. Moreover, an increment of the swarm population may result in lower convergence.

To apply the GOA algorithm for solving SHE Equation (4) the X_i^d must be correlated with the *i-th* vector of switching angles $[\alpha_1\ \alpha_2\ \alpha_3\ \alpha_4\ \alpha_5]_i$ Thus, in this case, the problem is 5 dimensional. In the following subsections, the modifications of GOA are proposed and tested in section V.

4.1. GOA with GWO Module

Grey Wolf Optimizer is a meta-heuristic algorithm inspired by the behavior of grey wolves and mathematically described by Mirjalili et al. in [41]. The GWO is well studied and can be treated as an independent algorithm. However, its main feature can be implemented in other algorithms. The specifics of the GWO is based on the determination of the three best global solutions called alpha, beta, and gamma. Positions of all particles in the swarm will be updated with respect to the position of

the three best global *Ta*, *Tb*, *Tc*. Thus, to combine GOA and GWO, formula (13) will be modified to the following form [24]:

$$X_i^d = c\left(\sum_{\substack{j=1 \\ j\neq i}}^{Np} c\cdot\frac{ub^d - lb^d}{2}s\left(d_{ij}^{d*}\right)\frac{x_i^d - x_j^d}{\left|x_i^d - x_j^d\right|}\right) + \frac{T_A^d + T_B^d + T_C^d}{3} \tag{15}$$

4.2. GOA with NS Module

The theory of Natural Selection is based on the random elimination of agents from the swarm with a certain probability P with respect to their fitness value. The better result has a higher chance to survive. Thus, NS requires a classification of the agents then the algorithm calculates P for each agent. To adopt NS for the SHE problem the following formula for P for the i-th agent was developed:

$$P_i = P_{min} + \left[(P_{max} - P_{min})\cdot\left(\frac{f_{fit\_i}}{f_{fit\_swarm}}\right)\right] \tag{16}$$

where P_{min} is the minimum assumed probability of survival assigned for the weakest agent; P_{max} is the maximum assumed probability of survival assigned for the best agent; f_{fit_i} is the fitness of the *i-th* agent; f_{fit_swarm} is the mean value of fitness functions of all agents in the swarm.

The roulette is performed for every single agent regarding its probability of survival. The eliminated agents are replaced by new random solutions.

4.3. Adaptive GOA

Adaptive Grasshopper Optimization Algorithm (AGOA) is based on a dynamic adaptation of the *c* coefficient regarding the Evolutionary Rate (ER) of the swarm of grasshoppers. ER is defined as the ratio between the number of agents whose fitness was improved in the previous iteration to the total number of agents in the swarm *Np*. Thus, *c* for AGOA is defined by the following formula:

$$c(ite) = \left(c_{max} - ite\,\frac{c_{max} - c_{max}}{t_{max}}\right)F_{ER}\,(ite) \tag{17}$$

where $F_{ER}\,(ite)$ is the dynamic adjustment function defined by the following correlation:

$$F_{ER}\,(ite+1) = \begin{cases} \frac{F_{ER}\,(ite)}{F_0};\ for\ ER < 15\% \\ F_{ER}\,(ite);\ for\ ER\ \in\ \langle 15\%; 30\%\rangle \\ F_{ER}\,(ite)\cdot F_0\ ;\ for\ ER > 30\% \end{cases} \tag{18}$$

where F_0 is a constant larger than 1. Thus, AGOA presents a dynamic change of comfort zone with a decreasing trend.

4.4. GOA with OBL Module

Opposite Based Learning is a technique of swarm algorithms modification based on the statement that the opposite solution to the developed one might bring better result. Thus, every solution (agent) should be reversed and its fitness should be evaluated. If the fitness of the reversed solution is better than the original, the agent will be replaced. Opposite value $\ddot{X}_i^d$ can be calculated as follows:

$$\ddot{X}_i^d = ub^d + lb^d - X_i^d; \tag{19}$$

$$for\ i = 1, 2, \ldots, Np; d = 1,\ 2,\ \ldots,\ N$$

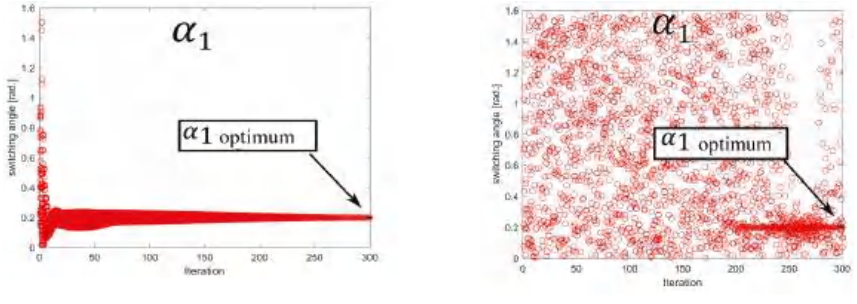
However, the application of this technique to SHE brings issues regarding the feasibility of calculated solutions. As switching angles are restricted to be sorted according to their feasibility, Equation (19) will reverse their order and make them not feasible. To implement OBL to solve the SHE problem opposite solution $\ddot{X}_i^d$ must be reordered to respect restriction: $0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \frac{\pi}{2}$.

5. Simulation Tests and Comparative Study

In this section, a simulation analysis of GOA algorithm performance is presented. Moreover, a comparative study between GOA and modified GOA (NS, AGOA, GWO, and OBL) is carried out. The optimization process has been carried out with the following assumptions:

- STOP criterion of the optimization process is obtained when reaching the assumed maximum number of iterations or the value of the fitness function is below the assumed tolerance 1×10^{-4}
- Every modification module is tested separately. The combination of all modules in one algorithm is not tested. The reason is an increment of computation effort for multi-module algorithm what makes it difficult to compare with single module modifications,
- Swarm population (*Np*) and maximum number of iterations (*max_ite*) for comparative study is established regarding similar computational effort (elapsed time of optimization) for compared algorithms.

Figure 4 shows the flow chart of the developed GOA algorithm for SHE with marked modification modules. However, as was mentioned above, only one module is active at the time.



(**a**) (**b**)

Figure 4. The trajectory of particles in the swarm searching for optimal switching angle α_1 with (**a**) GOA (**b**) Particle Swarm Optimization (PSO).

5.1. Comparison between GOA and PSO

The comparative study between GOA and PSO was carried out for $n = 5$ switching angles in a quarter-period, modulation index $M1 = 0.9$, and fundamental frequency $f_f = 50$ Hz what gives 550 Hz switching frequency. In this work 5th, 7th, 11th, and 13th harmonics are eliminated permanently. Figure 5 presents the trajectories of particles during the optimization process with GOA and PSO algorithms, respectively. The GOA algorithm is characterized by a short time of exploration and a long period of exploitation while the PSO algorithm provides a very high intensity of exploration. Figure 6 shows that PSO needs a higher number of iterations to converge comparing with GOA and its modifications.

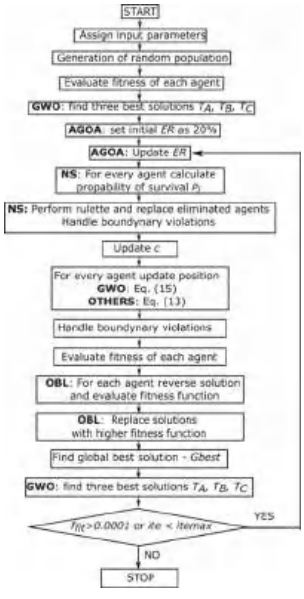


Figure 5. Flow chart of the GOA algorithm with proposed modification.

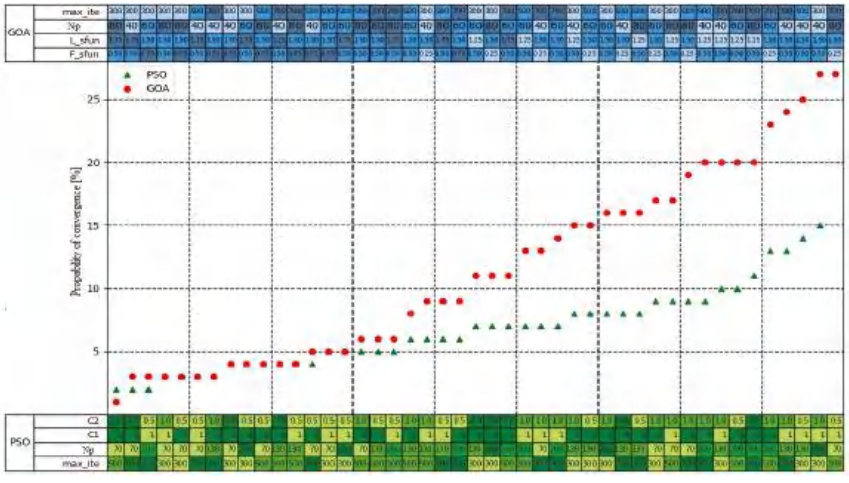


Figure 6. Comparison between PSO and GOA convergence for different values of coefficients.

In the following part of this section, the convergence of GOA and PSO has been compared. The various combinations of parameters were tested. For every set of both GOA and PSO, 100 runs were calculated. For each series of runs, the number of runs that reaches f_{fit} below 1×10^{-4} was recorded as the success. The variation of the following parameters was studied: maximum number of iterations (*max_ite*), size of the population (*Np*), PSO parameters C1 and C2, and GOA parameters used in s-function (L and F). Thus, all results have been presented in Figure 6 where the probability of convergence is compared. The value of population size for PSO and GOA was adjusted to keep similar computation times for both.

The best performance of GOA was recorded for settings: $Np = 40$ $max\_ite = 300$, $L = 1.5$ and $F = 0.5$. For the aforementioned setting, GOA achieved 27% convergence (time of computation 101 s). The PSO

achieved the best performance for: $Np = 250$, $max\_ite = 300$, $C1 = 1$ and $C2 = 0.5$. Thus, GOA presents better performance than PSO regarding higher convergence for lower population size. Results presented in Figure 6 proves that for the SHE problem the GOA presents a significantly higher probability of convergence than the PSO algorithm. The most interesting result was achieved by using the GOA algorithm for population 40 and 300 iterations (the second-highest for this algorithm) where the probability of convergence was 28%. This result proves that the GOA algorithm can be very efficient for low population set up which reduces its computational effort. The highest recorded probability of convergence of PSO during the experiment was 15% (time of computation 260 s). The GOA algorithm gives a better result faster. The computation effort is extremely significant during the application of the optimization task for the task. In this paper, coefficients of the compared algorithm were selected in such a way to keep comparable computation time. The parameters which are affecting computation time are population size *Np* and the maximum number of iteration *max_ite*. Results presented in Figure 6 can be divided into 9 *SETS* regarding *Np* and *max_ite*. Table 2 presents computation time for the PSO and GOA performed on a computer with processor *Intel Core i7-8557U*. Results from Table 2 are presented in Figure 7. The parameters *Np* and *max_ite* were selected to keep similar computation time for GOA and PSO for one SET. The GOA in every iteration calculates the position of every agent (grasshopper) related to every agent in the swarm, PSO calculates the only position of the agent related to the position of the pest particle. That is why GOA needs higher computational effort than PSO for the same *Np*. Thus, to make it comparable the *Np* for GOA was reduced in every SET.

Table 2. Sets of coefficients with computation time (100 runs).

	PSO			GOA		
No.	**Max_Ite**	**Np**	**Time [s]**	**Max_Ite**	**Np**	**Time [s]**
SET 1	300	70	99	300	40	101
SET 2	300	130	169	300	60	163
SET 3	300	250	260	300	80	261
SET 4	500	70	165	500	40	152
SET 5	500	130	310	500	60	277
SET 6	500	250	470	500	80	438
SET 7	700	70	245	700	40	264
SET 8	700	130	412	700	60	385
SET 9	700	250	637	700	80	687

Figure 7. Computation time for different sets of coefficients.

Figure 8 shows the switching angles calculated by PSO and not modified GOA as the function of modulation index M1.

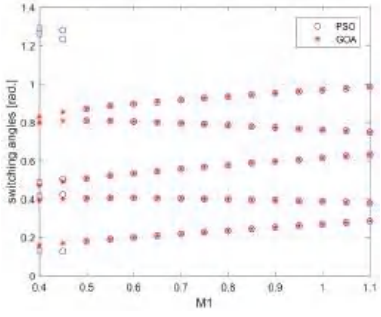


Figure 8. Switching angles as the function of modulation index M1 for SHE-PWM calculated using PSO and GOA.

5.2. Comparative Study between PSO, GOA, and Modified GOA

In this subsection, the convergence of GOA with modifications and PSO algorithms has been carried out. Assumptions from section *V A* and Table 3 are valid in this section. However, the comparison has been conducted for a wider range of modulation index $M1 = 0.4 \div 1.1$.

Table 3. Parameters for all analysis.

Algorithm	Coefficients	Value
GOA	c_{min}	1×10^{-6}
	c_{max}	1
GOA + NS	P_{min}	0.3
	P_{max}	0.95
AGOA	F_0	1.05
PSO	C1	2
	C2	2
	w_{min}	1×10^{-3}
	w_{max}	1

The comparative study reveals that the most efficient with the highest probability of convergence is the GOA algorithm modified by adding the OBL module (Figure 9). The convergence of the studied algorithm was decreasing with an increase of *M1* because higher modulation index requires smaller spaces between switching angles and reduce the feasibility of developed solutions. For *M1* in the range from 0.7 to 0.8 modification based on NS presented very good performance as well. Figure 10 presents the examination of fitness value (f_{fit}) as the function of the iteration number. The conclusion is that GOA-based algorithms present significantly faster convergence than PSO.

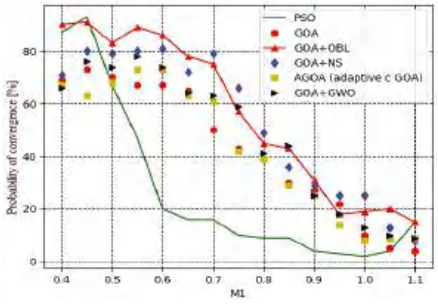


Figure 9. Comparison of the probability of convergence between PSO, GOA, and modified GOA algorithms.

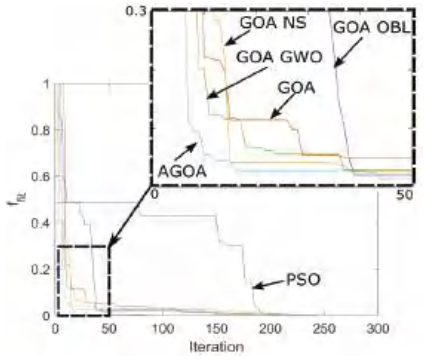


Figure 10. Fitness value versus iteration number for examined algorithms.

6. Experimental Results

The applied GOA algorithm has been experimentally verified. Switching angles calculated by the GOA algorithm were implemented into the laboratory stand (Figure 11) developed according to Figure 1. Parameters of the induction motor applied in the laboratory stand are presented in Table 1. The inverter control by switching angles input was provided by DSpace card 1104. Switching angles were applied as the look-up table for off-line control. Verification was conducted for two operating points with the same fundamental frequency f_f = 50 Hz, and different *M1* = 0.9 and 1.0, respectively.

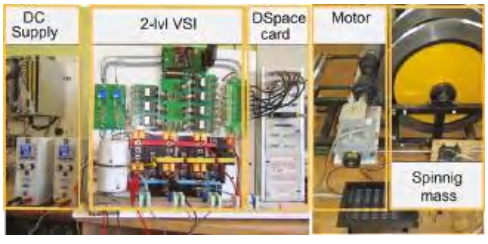
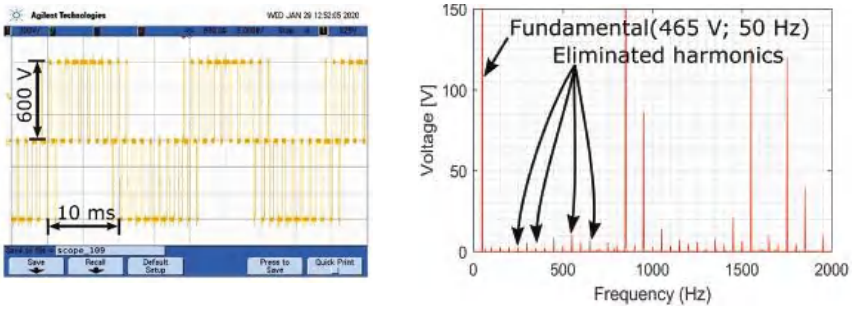


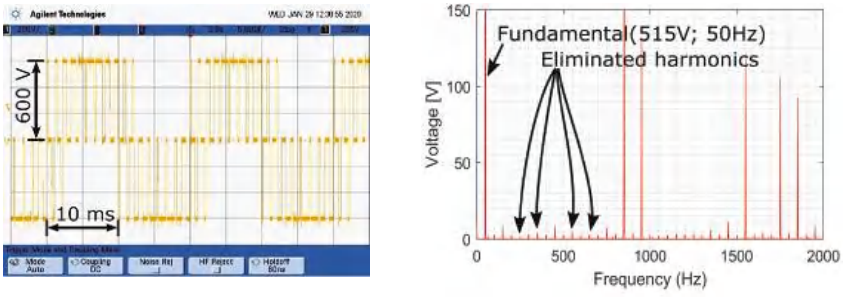
Figure 11. Laboratory stands for experimental tests.

In Figures 12 and 13 it can be noticed that amplitudes of 5th, 7th, 11th, and 13th harmonics in the output voltage have been eliminated and the GOA algorithm has successfully minimized the goal function.



(**a**) (**b**)

Figure 12. Experimental results for inverter's phase to phase output voltage for M1 = 0.9 (**a**) waveform oscillogram (**b**) spectrum.



(**a**) (**b**)

Figure 13. Experimental results for inverter's output phase to phase voltage for M1 = 1.0 (**a**) waveform oscillogram (**b**) spectrum.

7. Conclusions

In this paper, the authors investigated a novel application of a recently developed GOA algorithm, for the calculation of switching angles in SHE-PWM inverter modulation. The main goal of this paper was to examine the probability of convergence introduced by GOA applied for solving the SHE problem. Modifications of the GOA algorithm have been implemented and compared with the PSO algorithm. The GOA algorithm is based on the behavior of a swarm of grasshoppers and the most characteristic feature is that the movement of agents depends not only on the position related to the position of the best agent (best global solution) but it depends on the position related to the other agents as well. Thus, the results prove that the GOA algorithm requires a lower population size to converge with computation effort similar to PSO. The most interesting outcome of this study is that the GOA algorithm with OBL elements proves its superiority over the PSO algorithm regarding the probability of convergence for similar computational effort (lower population of particles). The second most efficient combination was the GOA algorithm with NS modification. GOA presents the highest advantage over PSO in the range of modulation index from 0.5 to 1.0. In this range, the convergence of PSO was dramatically reduced (below 5% in the worst case), and meanwhile, the probability of convergence of GOA was between 20 and 80%. The performed measurement experiments proved that the SHE-PWM waveform optimized by the GOA algorithm provided elimination of the chosen harmonics in the inverter's output voltage. In the nearest future, authors will focus their attention on the application of the GOA algorithm for optimization of waveforms generated by multilevel inverters and its applicability in traction drive solutions.

Author Contributions: M.S.: Concept and methodology of the research, development of software and application of algorithms. Formulation of conclusions. W.J.: Laboratory measurements and presentation of results. A.S.: Research supervision and text formatting. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

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