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Hybrid Modulation for Modular Voltage Source Inverters with Coupled Reactors

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Abstract: This paper proposes and discusses a concept of a hybrid modulation for the control of modular voltage source inverters with coupled reactors. The use of coupled reactors as the integrating elements leads to significant reduction in the size and weight of the circuit. The proposed modulation combines novel coarsely quantized pulse amplitude modulation (CQ-PAM) and innovative space-vector pulse width modulation (SVPWM). The former enjoys very low transistor switching frequency and low harmonic elimination, while the latter ensures high resolution of amplitude control. The SVPWM is based on the use of barycentric coordinates. The feasibility of the proposed solution is verified by simulations and laboratory tests of a 12-pulse modular voltage source inverters with two-level and three-level component inverters.

Keywords: modular; voltage source inverter (VSI); multipulse; 12-pulse; pulse amplitude modulation (PAM); pulse width modulation (PWM); three-level; coupled reactors

1. Introduction

The concept of modular voltage source inverters (VSI) with coupled reactors considered in this paper was first reported in [1] (therein dubbed multipulse voltage source converters (VSC) with coupled reactors). The idea has its roots in the well-known multipulse AC–DC converter topologies widely used in a variety of applications, including adjustable speed drives (ASD), high-voltage direct current transmission (HVDC), aircraft power systems, and renewable energy conversion systems [2–5]. The use of multipulse topologies for the DC–AC power conversion has broad coverage in the literature (see, for example, in [6–11]). The topologies proposed in [8–11] are based on the use of a transformer in an integrating circuit, which significantly increases the size of the device and is an expensive solution. If the application does not require galvanic isolation of the DC side from the AC side, the integrated circuit can be based on coupled reactors, as proposed in [1]—a solution which greatly reduces the size and cost of the circuit.

Solutions presented in [1,7–11] are focused on maximizing the achievable magnitude of output voltage, while the control of lower magnitudes is left out. The possible voltage synthesis using all allowed combinations of switch states has not been seriously addressed so far. In this paper, a control of the output voltage of the modular voltage source inverters proposed in [1,12] is considered. These converters contain standard inverter modules, but they are connected by special coupled reactors. The idea of modular VSI with coupled reactors draws on the properties of multipulse diode rectifiers with similar coupled reactors [13–15] and other converters with integrating magnetic circuits [4,16,17]. Coupled reactors were selected as integrating elements because their rated power is below 20% of that

of a transformer with similar integrating properties [5,13,14]. As the inverter modules are connected in parallel, these circuits can be used for high-current systems. Where increased operating voltages are required, multilevel inverters can be used as modules.

To clarify the terminology used in the sequel, note that the idea of "pulses" contained in the term "multipulse" has a simple interpretation in the case of diode or thyristor AC–DC converters: it denotes a section of AC input voltage transferred to the DC output. The "number of pulses", denoted M, is used to mean the number of such sections transferred in one fundamental period of the AC voltage. Although for DC–AC inverters with fully controlled power switches this idea of pulses is much less tangible, the number of pulses can still be used for the sake of discussion—as a constructional parameter of the inverter.

Transistor-based modular VSI with coupled reactors can be controlled in a variety of ways. One of the methods mimics the workings of multipulse rectifiers. This method relies on applying a succession of only M inverter voltage vectors in every fundamental period of the synthesized output voltage. This paper demonstrates that by appropriate selection of all available basic voltage vectors, it is possible to achieve coarsely quantized pulse amplitude modulation (CQ-PAM). This control approach, leading to staircase output voltage waveforms, enjoys very low switching frequency of power transistors (equal to the fundamental frequency of the output voltage). A drawback of this modulation method is low amplitude resolution. A workaround might be application of a controlled source of DC voltage, but this option is complex and costly and thus it is left out in this paper.

High-resolution voltage control can be achieved by means of pulse width modulation (PWM). Unlike CQ-PAM, PWM requires relatively high switching frequency (a multiple of the fundamental frequency of output voltage), which can be particularly disadvantageous in high-speed motor drive applications. For example, a two-pole motor operating at 150,000 rpm would call for 5 kHz fundamental frequency of the output voltage, meaning at least several dozens of kilohertz of the transistor switching frequency for PWM controlled inverter. Such high switching frequencies can cause significant mismatches between the transistor on/off commands and the actual turn-on/turn-off timing. What is more, the switching losses and electromagnetic interference resulting from high switching frequency can be prohibitive [18]. The problem of adequate voltage control increases with the increase of motor speed and/or its power. For instance, motor drives in the 1 kW power range are reported to operate at speeds of 500,000 to 1,000,000 rpm [19,20]. Concerning higher power drives, the authors of [21] report on a 60 kW drive operating at 100,000 rpm, while the authors of [22] describe a 300 kW drive operating at 60,000 rpm.

To address the above problems, this paper proposes a hybrid modulation combining CQ-PAM and PWM. This approach is capable of combining advantages of PWM (virtually unlimited resolution of voltage control) and those of CQ-PAM (radically reduced switching frequency). The CQ-PAM is intended for use at steady state, while the PWM ensures smooth passage through the transients. A somewhat similar idea of hybrid modulation was proposed in [23,24], but it relies on a combination of two different PWM methods: space-vector pulse width modulation (SVPWM) is used for smooth transients, while selective harmonic elimination PWM (SHE-PWM) is applied for low switching frequency operation at steady state. The CQ-PAM proposed here is even more effective in the reduction of switching frequency than SHE-PWM and—unlike the latter—can easily be computed in real-time. Both CQ-PAM and PWM can rely on selecting and applying appropriate voltage vectors. At steady state, a succession of only M different vectors per fundamental period is used for M-pulse inverters, with all vectors being applied for time intervals of the same length. At each interval, the voltage vector closest to the reference vector is selected. Concerning the PWM, vector selection and duty cycle computations are carried out using the barycentric coordinates [25]. This approach speeds up the calculations and allows easy inclusion of the DC link voltage fluctuations in the algorithm. The proposed modulation is exposed and discussed using the simplest case of modular VSI, that is, a 12-pulse inverter with two-level component inverter modules. The application of the proposed approach can easily be extended to inverters with higher pulse numbers and/or with multilevel

inverter modules [1,12]. Section 2 derives the formula linking the output voltage of modular VSI with coupled reactors with the voltages supplied by component inverter modules and finds the required turns ratio of the coupled reactors. Section 3 presents the proposed modulation method, while Section 4 presents and discusses selected simulation results pertaining to modular VSI using two-level and three-level component inverters and the CQ-PAM. A simulation of the passage between two different steady states using the proposed SVPWM is also demonstrated. The laboratory test results of the same two topologies are presented in Section 5.

2. The 12-Pulse Modular Voltage Source Inverter with Coupled Reactors

Twelve-pulse topology has been known as early as in the 1980s [14,26] and widely used in industry to date [5,27–29]. However, the first attempts to use this topology (with coupled reactors) in the inverter mode of operation were made only several years ago [1,7]. To the best of the authors' knowledge, there have been no other reports on the use of multipulse topologies for DC–AC conversion. This section analyses the output voltage of the considered modular VSI as a result of vector summation of the component inverter voltages and determines the required turns ratio of the coupled reactors. A schematic diagram of the 12-pulse modular VSI with coupled reactors is shown in Figure 1, while Figure 2 establishes vectorial notation of voltages used in the following analysis.

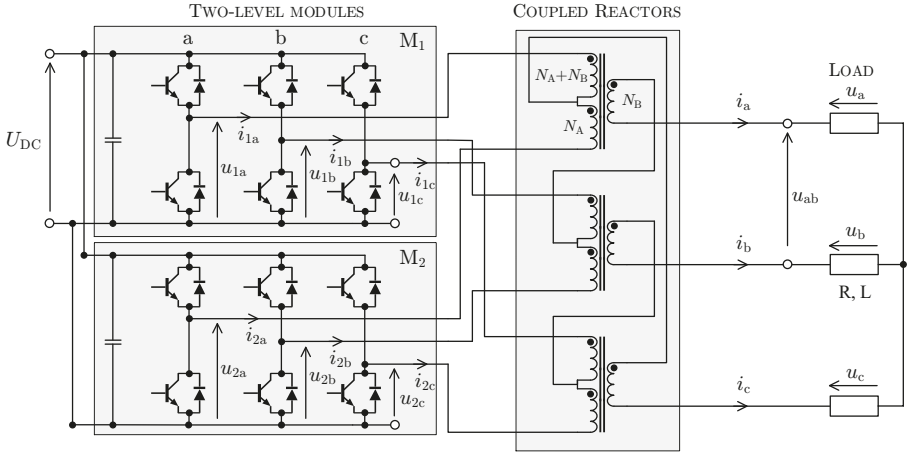

Figure 1. Twelve-pulse modular voltage source inverters (VSI) with coupled reactors.

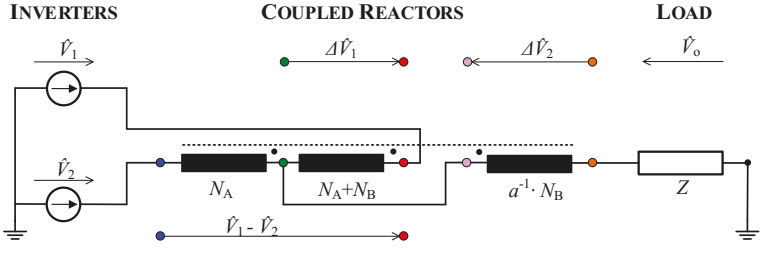

Figure 2. Vectorial equivalent circuit of the 12-pulse modular VSI.

According to the diagram in Figure 2, the output voltage vector of the analyzed modular VSI is given by

$$\hat{V}_{\mathrm{o}} = \hat{V}_1 - \Delta\hat{V}_1 - \Delta\hat{V}_2 \tag{1}$$

where

$$\Delta\hat{V}_1 = \left(\hat{V}_1 - \hat{V}_2\right) \cdot \frac{N_{\mathrm{A}} + N_{\mathrm{B}}}{2 \cdot N_{\mathrm{A}} + N_{\mathrm{B}}} \tag{2}$$

$$\Delta\hat{V}_2 = a^{-1} \cdot \left(\hat{V}_1 - \hat{V}_2\right) \cdot \frac{N_{\mathrm{B}}}{2 \cdot N_{\mathrm{A}} + N_{\mathrm{B}}} \tag{3}$$

$$\hat{V}_1 = U_{\mathrm{M}} \cdot \mathrm{e}^{j\frac{\pi}{3} \cdot ent\left[\frac{3}{\pi}\omega t\right]},\ \hat{V}_2 = U_{\mathrm{M}} \cdot \mathrm{e}^{j\frac{\pi}{3} \cdot ent\left[\frac{3}{\pi}(\omega t - \phi)\right]} \tag{4}$$

$$a = e^{j\frac{2 \cdot \pi}{3}} \tag{5}$$

Thus, on the basis of Equations (1)–(3), the output voltage can be described by

$$\hat{V}_{\mathrm{o}} = \hat{V}_1 - \left(\hat{V}_1 - \hat{V}_2\right) \cdot \frac{N_{\mathrm{A}} + N_{\mathrm{B}}}{2 \cdot N_{\mathrm{A}} + N_{\mathrm{B}}} - a^{-1} \cdot \left(\hat{V}_1 - \hat{V}_2\right) \cdot \frac{N_{\mathrm{B}}}{2 \cdot N_{\mathrm{A}} + N_{\mathrm{B}}} \tag{6}$$

After simple algebra, Equation (6) can be rewritten as

$$\hat{V}_{\mathrm{o}} = \hat{V}_1 \cdot \left(\frac{N_{\mathrm{A}}/N_{\mathrm{B}} - a^{-1}}{2 \cdot N_{\mathrm{A}}/N_{\mathrm{B}} + 1}\right) + \hat{V}_2 \cdot \left(\frac{N_{\mathrm{A}}/N_{\mathrm{B}} - a}{2 \cdot N_{\mathrm{A}}/N_{\mathrm{B}} + 1}\right) \tag{7}$$

It is assumed that the control signals of the inverter modules in the considered 12–pulse system are phase-shifted by $\phi = 30^{\circ}$, meaning the same phase shift between vectors $\hat{V}_1$ and $\hat{V}_2$. As a result, Equation (7) can be converted to

$$\hat{V}_{\mathrm{o}} = \left(\hat{V}_1 + \hat{V}_2\right) \cdot \left[\frac{(N_{\mathrm{A}}/N_{\mathrm{B}})}{2 \cdot (N_{\mathrm{A}}/N_{\mathrm{B}}) + 1}\right] - \left(\hat{V}_1 \cdot a^{-1} + \hat{V}_2 \cdot a\right) \cdot \left[\frac{1}{2 \cdot (N_{\mathrm{A}}/N_{\mathrm{B}}) + 1}\right] \tag{8}$$

In order to determine the appropriate turns ratios of the reactor coils, assume that the magnitude of voltage across a coil is proportional to its number of turns. Then, from Figure 2 it immediately follows that

$$\frac{\left|\hat{V}_1 - \hat{V}_2\right|}{2 \cdot N_{\mathrm{A}} + N_{\mathrm{B}}} = \frac{\left|\Delta\hat{V}_1\right|}{N_{\mathrm{A}} + N_{\mathrm{B}}} = \frac{\left|\Delta\hat{V}_2\right|}{N_{\mathrm{B}}} \tag{9}$$

The desirable turns ratio is such that ensures symmetric contribution of the component voltages $\hat{V}_1$ and $\hat{V}_2$ to the output voltage $\hat{V}_{\mathrm{o}}$, as illustrated in Figure 3. From the vector diagram in Figure 4, which is an enlargement of the shaded fragment in Figure 3, the following relationship can be found using Thales's theorem,

$$\frac{\left|\hat{V}_1 - \hat{V}_2\right|}{2} \cdot \tan(\lambda) = \left|\Delta\hat{V}_2\right| \cdot \sin\left(60^{\circ}\right) \tag{10}$$

where $\lambda = \frac{\phi}{2} = 15^{\circ}$. Now, using this value of λ and substituting Equation (10) to Equation (9), one arrives at

$$\frac{2 \cdot N_{\mathrm{A}} + N_{\mathrm{B}}}{2} \cdot \tan(15^{\circ}) = N_{\mathrm{B}} \cdot \sin\left(60^{\circ}\right) \tag{11}$$

whereupon, using basic trigonometric relationships, an explicit formula for the required turns ratio of the reactor coils is found:

$$\frac{N_{\mathrm{A}}}{N_{\mathrm{B}}} = \frac{\sin\left(60^{\circ} - 15^{\circ}\right)}{\sin\left(15^{\circ}\right)} = 2.732 \tag{12}$$

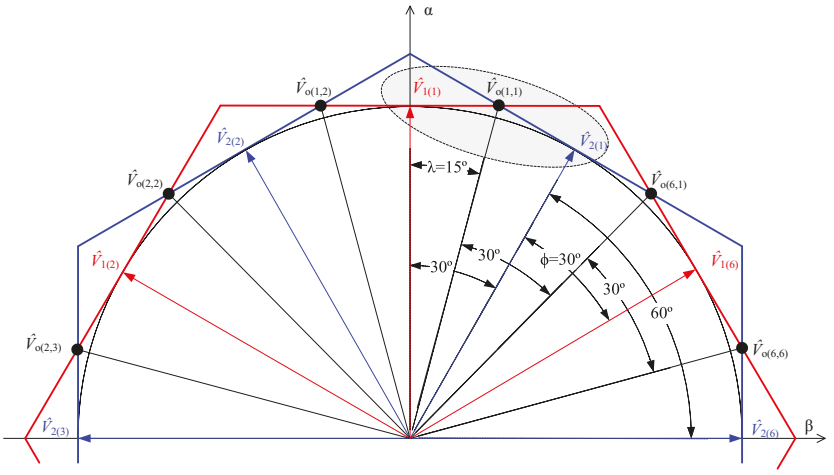

Figure 3. Desirable positions of basic output vectors of component inverters in the 12-pulse modular VSI.

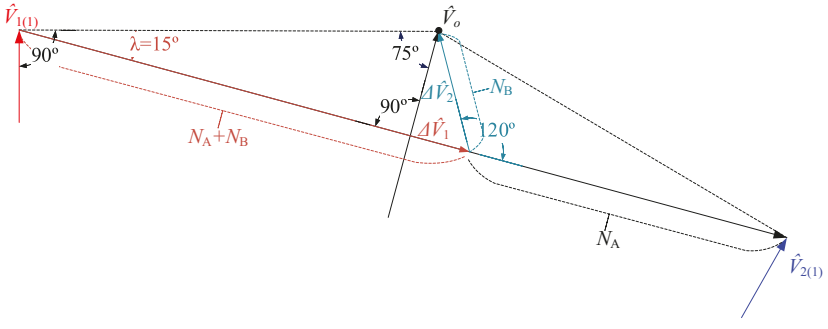

Figure 4. Details of geometric relationship between the output vector $\hat{V}_o$ of the 12-pulse modular VSI and component vectors $\hat{V}_1$ and $\hat{V}_2$.

3. Proposed Hybrid Modulation Method

In one of the proposed operation modes of the considered modular VSI, transistors of inverter modules commute with the fundamental output frequency, which means significant reduction of switching losses and electromagnetic interference (EMI) distortion, and allows high frequencies of output voltages. The problem with this type of control, referred to as the CQ-PAM, is the limited resolution of the output voltage. The proposed solution is the use of PWM as a complementary control method. Both modulation techniques are based on appropriate selection and timing of the available basic vectors, that is, voltage vectors corresponding directly to the on/off states of inverter switches. These vectors can be considered points on a two dimensional $\alpha\beta$ plane. The basic vector diagram for the considered 12-pulse system is shown in Figure 5a. The basic vectors in Figure 5 are obtained in two steps. First, the leg voltages of component inverter modules (marked in Figure 1) are transformed to phase voltages of the modular VSI by

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} u_{1b} & u_{1b} - u_{2b} & u_{1a} - u_{2a} \\ u_{1c} & u_{1c} - u_{2c} & u_{1b} - u_{2b} \\ u_{1a} & u_{1a} - u_{2a} & u_{1c} - u_{2c} \end{bmatrix} \cdot \begin{bmatrix} 1 \\ -k_1 \\ -k_2 \end{bmatrix} \tag{13}$$

where

$$k_1 = \frac{N_A + N_B}{2 \cdot N_A + N_B},\ k_2 = \frac{N_B}{2 \cdot N_A + N_B} \tag{14}$$

Then, the $\alpha\beta$ coordinates of the corresponding basic vectors ($\hat{V}_o$) are determined by the Clarke transformation:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \cdot \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{15}$$

In general, the number of different basic vectors for an M-pulse inverter with l-level inverter modules is $l^{\frac{M}{2}}$. Therefore, the considered 12-pulse converter exhibits 64 different basic vectors.

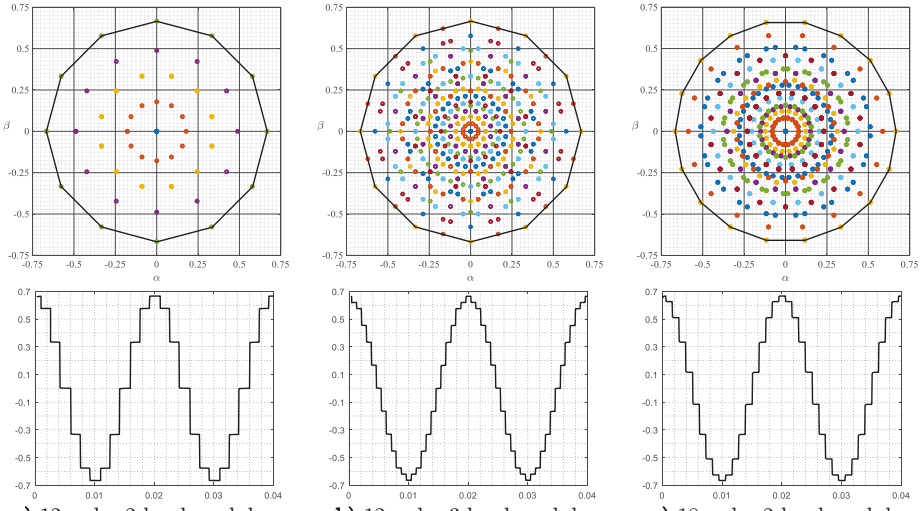

Figure 5. Space-vector diagrams of three modular VSI topologies (top graphs) and example voltage waveforms (bottom graphs) corresponding to the sequences of vectors indicated by connecting lines: (**a**) 12-pulse 2-level modules; (**b**) 12-pulse 3-level modules; (**c**) 18-pulse 2-level modules.

3.1. Coarsely Quantized Pulse Amplitude Modulation (CQ-PAM)

Basically, the CQ-PAM involves applying a succession of only M different basic vectors per fundamental period, with all vectors having the same magnitude and being applied for equal-length time intervals. The selection of basic vectors relies on the criterion of proximity between the reference vector and the basic vectors. As seen in Figure 5a, for $M = 12$ and $l = 2$ only four different non-zero magnitudes are available, meaning very limited resolution. However, as can be noticed in Figure 5b,c, as the number of inverter modules or inverter voltage levels increases, the resolution of the CQ-PAM significantly rises—for an 18-pulse modular VSI it is 16 magnitudes and for a 12-pulse modular VSI with three-level modules it is 24 magnitudes.

For increased M and/or l, some neighboring magnitudes are close to each other, and thus it can be beneficial to use their combinations rather than stick to the same-magnitude principle. This option is illustrated in Figure 5b for the 12-pulse VSI with three-level modules: the sequence of vectors leading to the waveform shown in the lower graph is a succession of 24 (that is, $2 \cdot M$) basic vectors indicated in the upper graph; the magnitude of the shorter vectors is $\cos(\frac{\pi}{M}) = \sim 0.97$ times that of the longer vectors. What is more, some magnitudes can be represented by more than M vectors. For instance,

the 12-pulse VSI with three-level modules has seven magnitudes represented by $2 \cdot M = 24$ basic vectors. Again, this fact can be exploited in the CQ-PAM algorithm.

3.2. Space Vector Pulse Width Modulation (SVPWM)

To ensure virtually unlimited amplitude resolution of output voltage control, the PWM can be used whenever necessary or desirable. An economic solution might be the PWM discussed in [17,30] for 12-pulse rectifiers. However, this PWM technique offers only limited voltage control range and does not take advantage of the natural elimination of low harmonics in multipulse systems. Another candidate solution might be selective harmonic elimination PWM (SHE-PWM), which allows to decrease the switching frequency and remove a set of selected harmonics. Such a method was applied for parallel inverters driving a single load separated by line reactors [31]. However, this method requires precomputation of the appropriate PWM patterns, which is hardly possible in real-time [32,33]. This paper proposes an innovative space-vector PWM (SVPWM) based on barycentric coordinates.

In most cases considered in the literature, the output vectors are synthesized using the nearest three vectors (NTV) approach. A similar approach is adopted in this paper. In order to select the nearest basic vectors, the magnitude of reference vector (V_{ref}) is compared with the available magnitudes of inverter basic vectors. The comparisons permit determining two neighboring magnitudes between which the reference vector is located. The closest two basic vectors of either magnitude are then searched for using a simple sorting algorithm and the following vector distance relationship

$$\Delta V = \sqrt{(V_{\text{ref}\alpha} - v_\alpha)^2 + (V_{\text{ref}\beta} - v_\beta)^2} \tag{16}$$

The so obtained closest vectors can be considered vertices of a quadrangle ABCD, as illustrated in Figure 6. The quadrangle can be divided into four triangles. The tasks of the modulation include selecting the most appropriate of the triangles and computing the duty cycles of the three corresponding basic vectors.

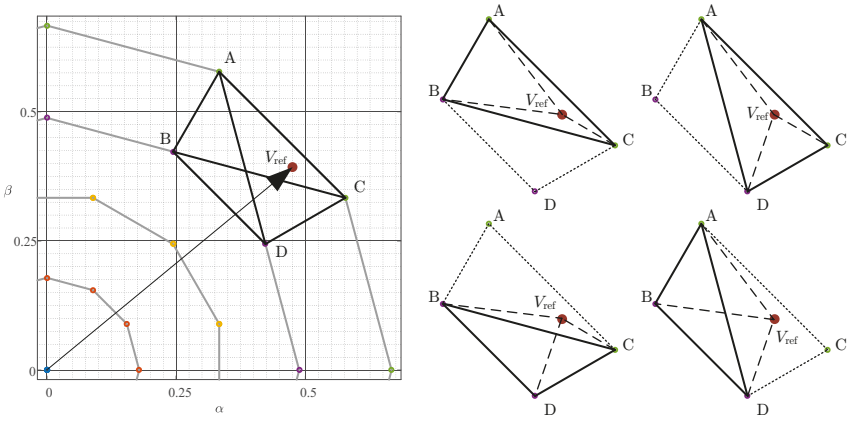

Figure 6. Example reference vector and its representation by means of barycentric coordinates.

Both of the above indicated tasks can be achieved with the aid of barycentric coordinates [25]. Unlike the most popular methods of PWM computations, which are based on trigonometric functions, the use of barycentric coordinates avoids the related inconvenience. Consider the reference vector in Figure 6. It can be considered a point inside triangle ABC or triangle ACD. To fix attention, let us focus on the former triangle. The computation of duty cycles of the corresponding basic vectors is effectively means expressing the position of the reference vector as a linear combination of basic vectors. This is equivalent to expressing the Cartesian coordinates of a point inside a triangle by the barycentric

coordinates of that point. Thus, the coordinates of vector (V_{ref}) in Figure 6 can be expressed by the coordinates of points A, B, and C:

$$\begin{bmatrix} V_{\text{ref}\alpha} \\ V_{\text{ref}\beta} \end{bmatrix} = \begin{bmatrix} A_\alpha & B_\alpha & C_\alpha \\ A_\beta & B_\beta & C_\beta \end{bmatrix} \begin{bmatrix} N_1 \\ N_2 \\ N_3 \end{bmatrix} \tag{17}$$

where N_1, N_2, and N_3 are the barycentric coordinates of V_{ref}, which can be calculated from

$$\begin{bmatrix} N_1 & N_2 & N_3 \end{bmatrix} = \begin{bmatrix} \frac{\triangle_{V_{\text{ref}}BC}}{\triangle_{ABC}} & \frac{\triangle_{V_{\text{ref}}AC}}{\triangle_{ABC}} & \frac{\triangle_{V_{\text{ref}}AB}}{\triangle_{ABC}} \end{bmatrix} \tag{18}$$

with the $\triangle_{ijk}$ symbols representing the areas of the small triangles defined inside triangle ABC by the vertices of the latter and V_{ref}. Stated differently, the barycentric coordinates are equal to the normalized areas of their corresponding small triangles. These areas can be computed direct from the $\alpha\beta$ coordinates of the appropriate basic vectors by

$$\triangle_{ijk} = \frac{1}{2} \cdot \left| \begin{bmatrix} v_{i\alpha} & v_{i\beta} & 1 \\ v_{j\alpha} & v_{j\beta} & 1 \\ v_{k\alpha} & v_{k\beta} & 1 \end{bmatrix} \right| \tag{19}$$

A useful property of the barycentric coordinates is that their sum is equal to unity if they are calculated for a point inside a triangle (e.g., V_{ref} in the triangle ABC or ACD in Figure 6), but is greater if the point lies outside the triangle (e.g., V_{ref} in the triangle ABD or BCD in Figure 6). Thus, a uniform and effective method of finding a triangle or triangles containing a reference vector may be to calculate some candidate barycentric coordinates and then select the smallest (ideally 1).

As can be seen in Figure 6, the reference vector can be located inside two different triangles, and so some additional selection criterion is necessary to make the choice unique. The proposed algorithm selects the triangle for which the distance between the reference vector and the centroid $(\text{C}_\triangle)$ is smaller. This criterion was adopted in order to minimize the occurrence of narrow pulses. The coordinates of the centroids are calculated as arithmetic means of the coordinates of vertices:

$$\text{C}_\triangle = \begin{bmatrix} C_{\triangle\alpha} \\ C_{\triangle\beta} \end{bmatrix} = \begin{bmatrix} \frac{1}{3}\left(v_{i\alpha} + v_{j\alpha} + v_{k\alpha}\right) \\ \frac{1}{3}\left(v_{i\beta} + v_{j\beta} + v_{k\beta}\right) \end{bmatrix} \tag{20}$$

The distance between V_{ref} and the centroids is determined by Equation (16).

Although the proposed computational approach may seem rather complex for a system with only 64 space vectors, the practical target for the proposed method is modular VSI inverters with higher number of pulses M (notably, 18- and 24-pulse circuits) and using multilevel component inverters [1]. For such systems, the number of basic space vectors increases rapidly with M and the number of inverter levels (see Figure 5), as shown in Table 1.

Table 1. Number of space vectors for M-pulse modular VSI with l-level modules.

$l \setminus M$	12-Pulse	18-Pulse	24-Pulse
2-level	64	512	4096
3-level	729	19,683	531,683
4-level	4096	262,144	16,777,216

It is also important to note that with the increasing number of pulses and levels, the number of available magnitudes of inverter basic vectors also increases rapidly (e.g., 18-pulse and 24-pulse inverters with two-level modules have 16 and 67 output voltage magnitudes respectively and 12-pulse modular VSI with three-level modules has 23 output voltage magnitudes), rendering the CQ-PAM

mode a true alternative to the PWM for steady-state operation, with the proposed SVPWM becoming a method for increasing the voltage control resolution, especially during transients.

3.3. Selection of Modulation Method

The selection between CQ-PAM and SVPWM can be based on a variety of criteria, depending on the application (for instance the frequency criterion: SVPWM to be selected for lower fundamental frequencies, e.g., during the start-up, and CQ-PAM for higher fundamental frequencies). For the purpose of this study, the following magnitude proximity criterion is used; CQ-PAM is selected if the reference vector lies inside an annulus A_i defined by two circles—one inscribed in and the other described on a certain M-gon made of vectors of the ith magnitude (V_i); otherwise, SVPWM is chosen.

$$A_i = \left\langle \cos\left(\frac{\pi}{M}\right) \cdot V_i \, , V_i \right\rangle \tag{21}$$

The selection of the modulation method can be based on a decision diagram shown in Figure 7.

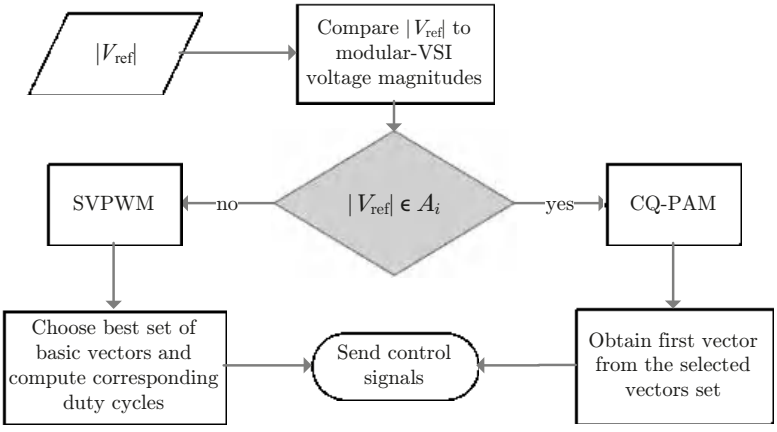

Figure 7. Control algorithm diagram.

4. Simulation Results

The proposed concept of output voltage control for modular VSI with coupled reactors has been verified using the PSIM11 simulation software and the Matlab environment. The simulated topologies included the 12-pulse inverter with two-level modules (Figure 1) and the 12-pulse inverter with three-level modules (Figure 8). The most important circuit and control parameters are given in Table 2.

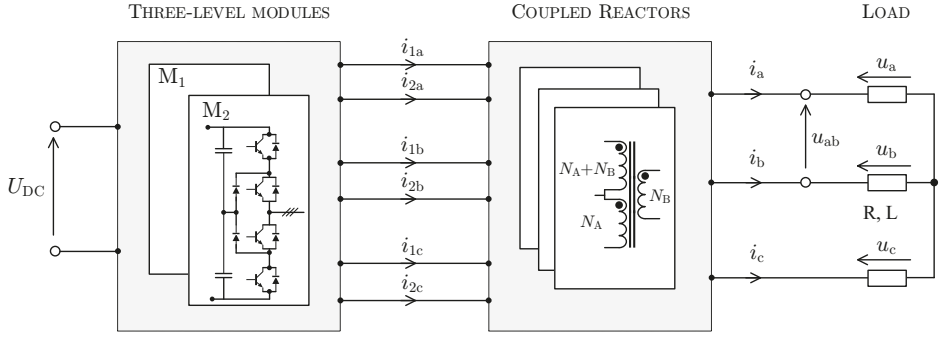

Figure 8. Twelve-pulse modular VSI with coupled reactors and three-level modules.

Table 2. Circuit and modulation parameters used in simulation.

Symbol	Value	Description
U_{DC}	100 V	DC source voltage
R	10 Ω	load resistance
L	0.2 mH	load inductance
f_o	1000 Hz	output fundamental frequency
f_m	30,000 Hz	modulation frequency
N_A	153	number of turns of coils A
N_B	56	number of turns of coils B

The operation of the considered modular VSI with CQ-PAM is illustrated in Figure 9. Characteristic values for output voltages and currents for this control mode are given in Table 3. A comparison of output voltage and current waveforms for two-level and three-level inverter modules is shown in Figure 10. To demonstrate how low the switching frequency is in relation to the output voltage frequency, the above figure also visualizes the leg voltage u_{1a} waveform (scaled down to 25% in Figures 9 and 10). The output voltages shown in Figure 9 are the time waveforms corresponding to 12-pulse space-vector diagrams presented in Figure 5a. Later in this section a passage is illustrated between two steady-state operating points with the aid of SVPWM invoked during the transients (Figure 11).

Table 3. Number of switch commutations per period of the output voltage and the THD (of voltages and currents) for the coarsely quantized pulse amplitude modulation (CQ-PAM) presented in Figure 9.

m_a	Commutations	THD U (%)	THD I (%)
0.179	5	15.58	8.4
0.345	3	15.58	8.4
0.488	3	15.58	8.4
0.67	1	15.58	8.4

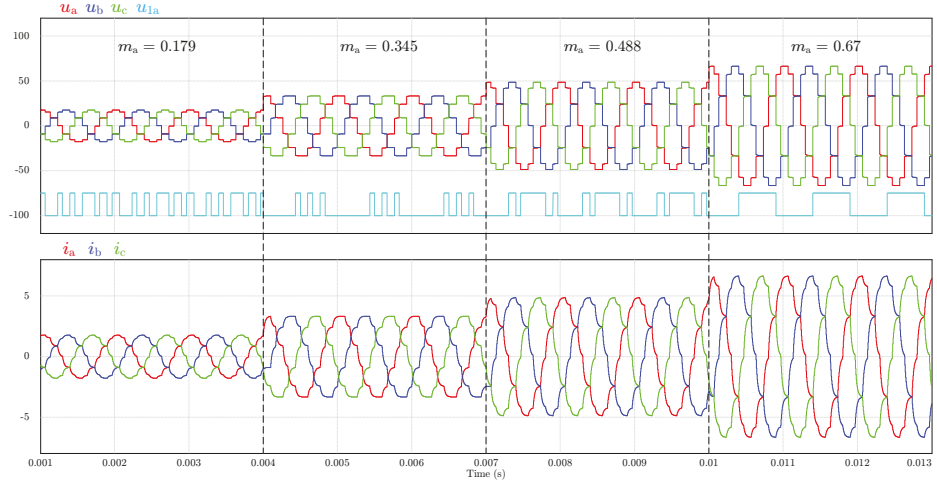

Figure 9. Output voltage and current waveforms of the 12-pulse modular VSI with CQ-PAM control.

Figure 10 illustrates the maximum-magnitude and minimum-magnitude output voltages of 12-pulse modular VSIs with two-level and three-level modules, and the corresponding currents and leg voltages. As can be seen, the use of multilevel modules can increase the number of output voltage steps, so that the total harmonic distortion (THD) of the output voltage decreases (from 15.58% for

two-level modules to 10% for three-level modules), and so does the THD of output currents (from 8.4% to 4.4% respectively). Moreover, for multilevel modules the dynamic range and resolution of output voltage magnitudes increases compared to the two-level modules. The minimum voltage for modular VSI with three-level modules is about four times lower than for two-level modules. The number of available non-zero voltage magnitudes also increases—from four in the case of two-level modules to twenty-three for three-level modules.

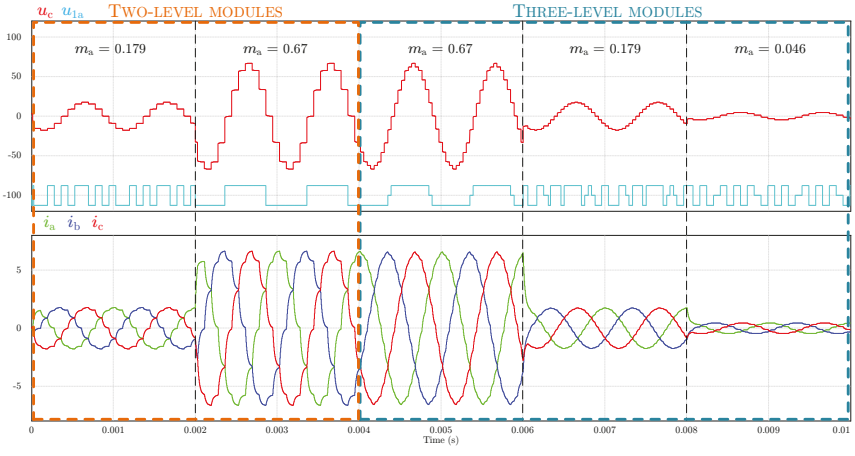

Figure 10. Example voltage and current waveforms of the 12-pulse modular VSI with two-level (**left**) and three-level (**right**) modules.

Figure 11 illustrates combined use of the proposed SVPWM and the CQ-PAM, ensuring smooth passage between different steady states. In this particular example the passage is between steady states at $m_a = 0.345$ and $m_a = 0.488$.

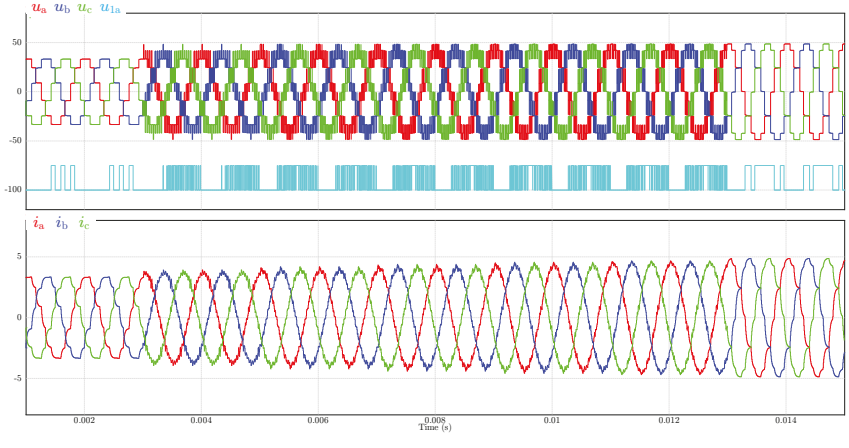

Figure 11. Example output voltage and current waveforms of the 12-pulse modular VSI during the passage between two different steady states.

5. Laboratory Test Results

The laboratory tests have been performed using two prototypes of modular VSI with coupled reactors: one using two-level inverter modules, and the other equipped with three-level modules.

The laboratory setup is presented in Figure 12. The most important circuit and control parameters are the same in both cases and identical to those used in the simulation (cf. Table 2). Measurements were taken by a Tektronix MDO4104B–3 oscilloscope. The control board contained a the two-core Texas Instruments digital signal processor TMS320C6672 and an Intel programmable logic device CYCLONE V. The coupled reactors shown in Figure 12 were designed for 30 kW (10 kW each) and rated frequency of 2.5 kHz. The numbers of turns of reactor coils are given in Table 2.

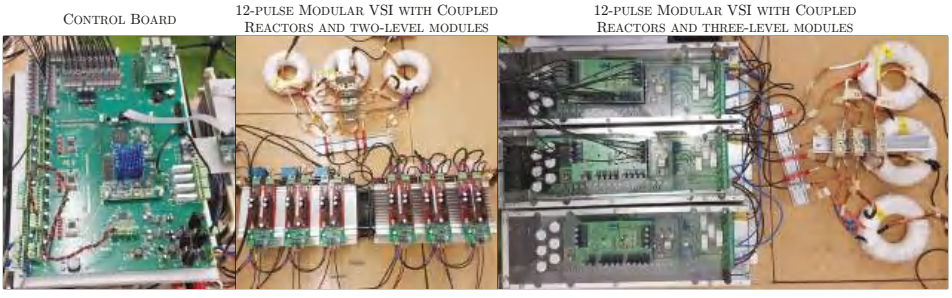

Figure 12. The laboratory set-up.

Figure 13 illustrates output phase voltages and currents, component inverter leg voltages, and the voltage across coil N_B for all output voltage magnitudes and parameters listed in Table 2 (for CQ-PAM controlled VSI with two-level modules). The waveforms correspond to the simulation results shown in Figure 9. The laboratory test results match the results of the simulation, except for the voltage spikes appearing between the steps in the laboratory waveforms. This is a consequence of the use of dead time and the fact that several inverter legs are switched simultaneously (for voltage magnitudes other than the maximum one). However, it can be noted that the amplitudes of these spikes are not significant (smaller than U_{DC}) and do not noticeably affect the current waveforms. The inverter leg voltages indicate the frequency with which the power switches commute (the waveforms confirm the data in Table 3). For the maximum available output voltage the switching frequency is equal to the fundamental output voltage frequency (in this case 1 kHz), and for the smallest CQ-PAM controlled output voltage it is equal to five times the output voltage frequency (5 kHz). One of the most important features distinguishing the coupled reactors from other magnetic integrating elements is their low rated power (related to the power of the overall system). To illustrate this feature, Figure 13 shows the voltage across the N_B coil of the coupling reactor. The voltage is not only significantly lower than U_{DC}, but may even assume values close to zero for some steps (depending on the output voltage magnitude). Therefore, the power transmitted through the reactor is only a fraction of the rated power of the inverter.

The hybrid modulation discussed in Section 3 is based on a combination of the CQ-PAM specific to the considered topologies, and the universal SVPWM—using the proposed computational approach based on barycentric coordinates. Figure 14 illustrates the phase voltages as well as phase-to-phase voltages for both modulation strategies. The voltages in Figure 14 correspond to $m_a = 0.67$ for CQ-PAM, and $m_a = 0.62$ for SVPWM. Figure 15 shows the voltages and currents obtained by SVPWM for two operating points: $m_a = 0.61$ and $m_a = 0.42$. The fundamental frequency was 1000 Hz for the higher output voltage and 600 Hz for the lower.

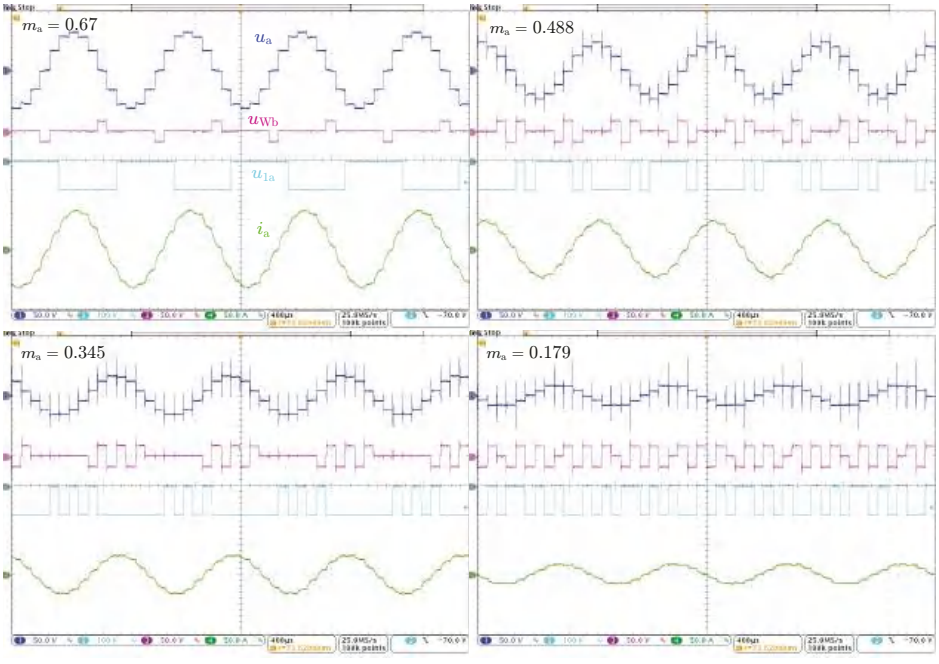

Figure 13. The output phase, leg, and coil N_B voltages and phase currents of the 12-pulse modular VSI with two-level modules for CQ-PAM control.

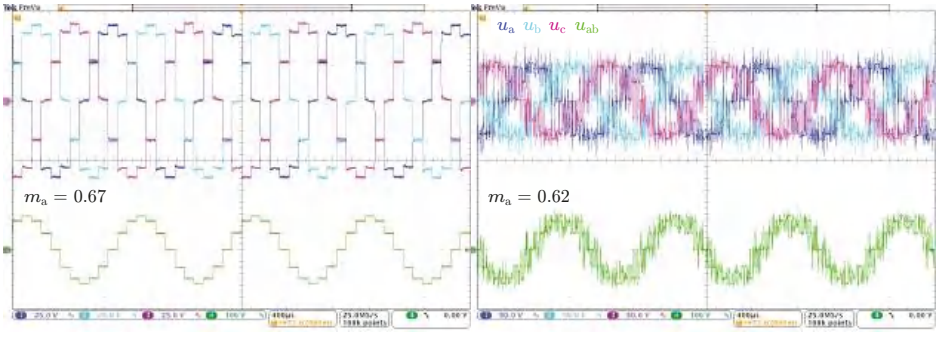

Figure 14. Output voltages for CQ-PAM (**left**) and space-vector pulse width modulation (SVPWM) (**right**) control.

The quality of output voltage and current will improve significantly with the increase in the number of inverter levels, as exemplified in Figures 16 and 17, which provide an initial comparison between the modular VSIs with two-level and three-level inverter modules. What is more, increasing the number of levels significantly increases the amplitude resolution of the CQ-PAM and reduces the voltage stresses of individual transistors. Consequently, the use of multilevel component inverters in the modular VSIs with coupled reactors will contribute to increased attractiveness of the considered topology.

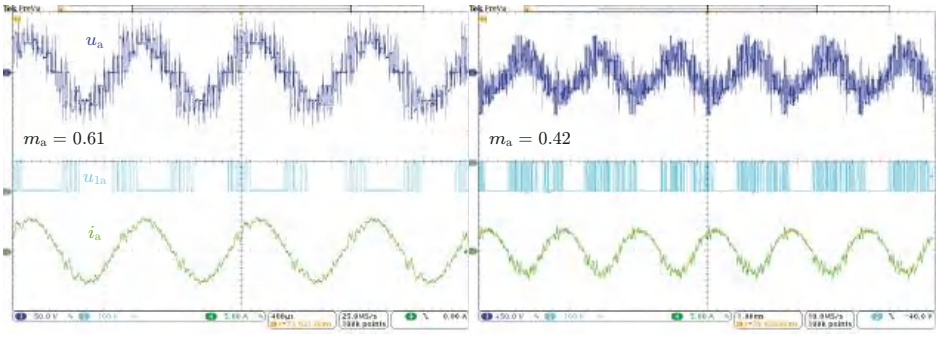

Figure 15. Example output voltages and currents for SVPWM control.

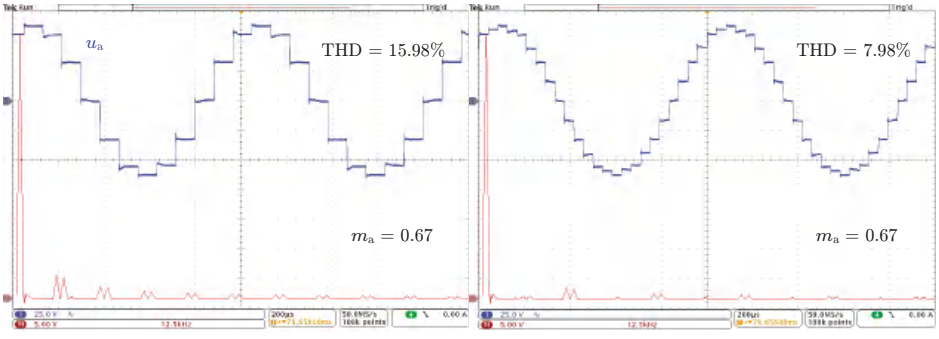

Figure 16. Output voltages and their spectra for the modular VSI with two-level (**left**) and three-level (**right**) modules.

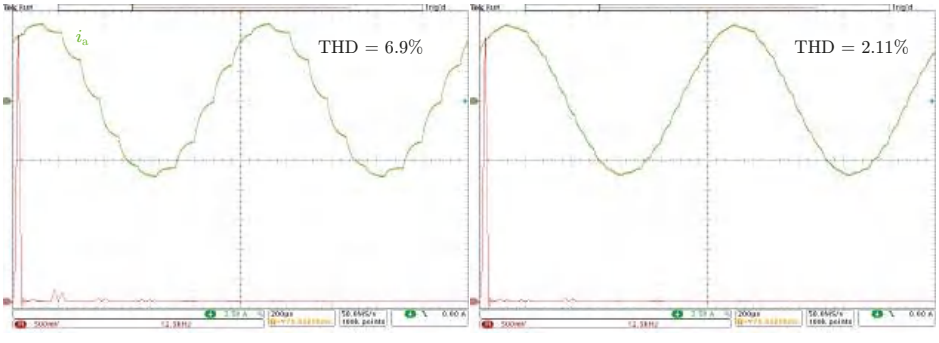

Figure 17. Load currents and their spectra for the modular VSI with two-level (**left**) and three-level (**right**) modules.

The modularity of the considered topology is an important advantage in itself. It allows, inter alia, even distribution of the overall power transferred by the inverter between the reduced-power modules. This feature is illustrated in Figure 18, which shows the phase currents of the component inverters (i_{1a}, i_{2a}) and the resultant load currents (i_a). As can be seen, the component inverter currents have the same amplitude close to half of the load current. The modularity also improves operational reliability of the considered topology, because it can continue working in case of a failure of one component inverter.

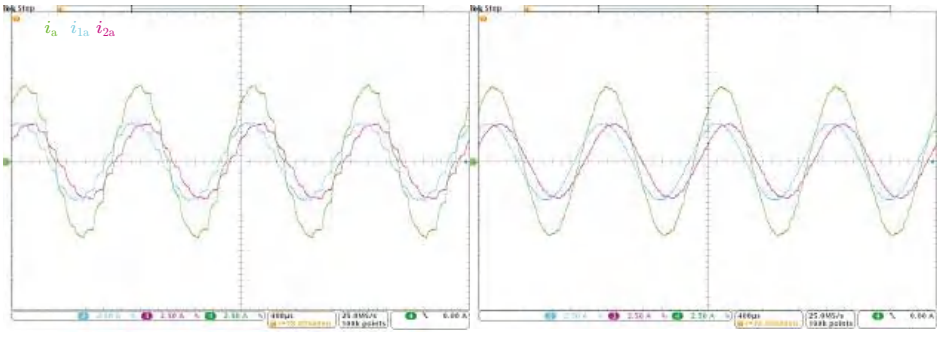

Figure 18. Phase currents of component inverters and the corresponding load currents of the modular VSI with two-level (**left**) and three-level (**right**) component inverters.

6. Conclusions

A hybrid approach to the output voltage control of modular VSI with coupled reactors has been proposed and discussed, including a novel coarsely quantized PAM and space-vector PWM based on the use of barycentric coordinates. Note that the use of these coordinates makes the SVPWM computations feasible and transparent even for such complex space-vector diagrams as those of the considered inverter topologies. The feasibility of the proposed solution has been verified by simulations and laboratory tests of the 12-pulse modular VSI with two-level and three-level component inverters. The use of multilevel inverter modules significantly improves the quality of output voltages and increases the attractiveness of the considered topology and the CQ-PAM, especially for application in high-speed motor drives (research into the latter application is planned for near future). It is also worth noting that the proposed solutions in modulation, although validated for particular inverter topologies, can be equally applicable to other topologies characterized by rich space-vector diagrams, including a variety of modular multipulse inverters.

Author Contributions: Conceptualization, K.J.S. and R.S.; methodology, K.J.S. and R.S.; software, K.J.S. and C.S.; validation, R.S., P.S., and C.S.; formal analysis, P.S. and J.N.; investigation, R.S., K.J.S., and C.S.; resources, K.J.S. and R.S.; data curation, R.S. and P.S.; writing—original draft preparation, K.J.S. and R.S; writing—review and editing, K.J.S., R.S., P.S. J.N., and C.S.; visualization, K.J.S., R.S., and C.S.; supervision, P.S., A.U., and J.N.; funding acquisition, P.S., J.N., and A.U. All authors have read and agreed to the published version of the manuscript.

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The Conceptual Research over Low-Switching Modulation Strategy for Matrix Converters with the Coupled Reactors

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Abstract: In this paper, different Pulse Width Modulation (PWM) strategies for operating with a low-switching frequency, a topology that combines Conventional Matrix Converters (CMCs), and Coupled Reactors (CRs) are presented and discussed. The principles of the proposed strategies are first discussed by a conceptual analysis and later validated by simulation. The paper shows how the combination of CMCs and CRs could be of special interest for sharing the current among these converters' modules, being possible to scale this solution to be a modular system. Therefore, the use of coupled reactors allows one to implement phase shifters that give the solution the ability to generate a stair-case load voltage with the desired power quality even the matrix converters are operated with a low-switching frequency close to the grid frequency. The papers also address how the volume and weight of the coupled reactors decrease with the growth of the fundamental output frequency, making this solution especially appropriate for high power applications that are supplied at high AC frequencies (for example, in airport terminals, where a supply of 400 Hz is required).

Keywords: matrix converter; pulse width modulation; multipulse voltage converter; nearest voltage modulation; pulse width regulation; low-switching modulation technique; multipulse matrix converter with coupled reactors

1. Introduction

The energy conversion in the AC grid realized by power electronics devices always needs efficiency, reliability, and compatibility [1]. The first element is significantly affected by conduction and switching losses of the applied semiconductors. Reliability can lead to the elimination of weak construction elements, which most often fail. Demands for Electromagnetic Intereference (EMI) compatibility have also increased in recent years [2]. Moreover, the ecological aspect of the energy-saving cannot be omitted today [3,4]. The paper proposes the Multipulse Matrix Converter with Coupled Reactors (MMCCR) [5–7] as an alternative

solution to the Variable Frequency Drive (VFD) based on the classic AC–DC–AC topology. The use of PWM techniques with a high-switching frequency in these applications can lead to significant dynamic losses but it is required to maintain the good quality of the generated AC voltage.

Reduction of switching frequency of the power electronic devices without a significant decreases of the output voltage quality can be achieved by using multilevel AC–DC–AC topology [8]. This device converts an AC input voltage into the DC voltage and the voltage smoothing bulk electrolytic capacitor in the DC-link circuit is required for this purpose. Capacitor bank stores the energy, which is converted back into AC voltage with the desired frequency using the PWM inverter [9–12]. Another concept of the AC voltage quality improvement uses magnetic elements and most often involves the use of multiphase transformers with an appropriately designed winding configuration [13]. This solution is characterized by low switching frequency but the main disadvantage of such approach related to transformers is cost. Without a doubt, the overall cost is driven by the transformer price, which can be reduced by applying instead the coupled reactors arrangement [14]. The main advantage of using coupled reactors is a significant size reduction, thus for the same load power coupled reactors will be designed for power around five times lower then transformer [15].

The Conventional Matrix Converter (CMC), in comparison with the classic AC–DC–AC frequency converter, has certain individual features that determine the innovation of such a solution [16–19]. This converter is fully bidirectional and operates without a large capacitor, with different frequencies at inputs and outputs of the system. Moreover, a matrix converter allows the power factor regulation [20]. The topology, which contains four matrix converters with coupled reactors, has been already demonstrated in literature [21] but without the inclusion of the amplitude voltage control. The proposed converters arrangement can be used in a turbine generator system equipped with a high-speed synchronous generator with permanent magnets. In such a system, the turbine transmits torque to the shaft of the electric machine directly or through a mechanical transmission, as illustrated in Figure 1.

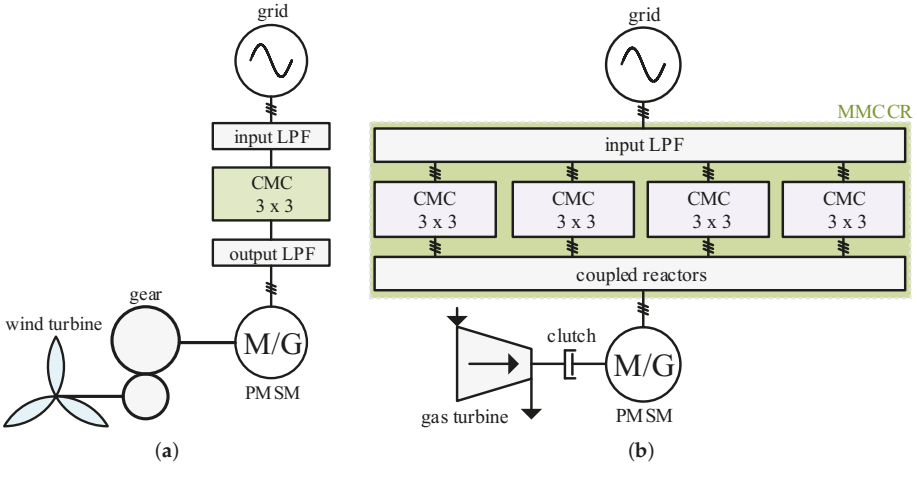


Figure 1. Examples of simplified application diagrams of turbines: (**a**) a wind turbine with a gear, (**b**) a gas turbine with a clutch. Conventional Matrix Converter (CMC) 3 × 3—conventional matrix converter with 3 inputs and 3 outputs, M/G—motor/generator, LPF—low-pass filter.

The synchronous generator produces AC voltage with a frequency dependent on the rotational speed of the turbine [22]. To transfer the obtained energy to the grid, the generated voltage should be converted and synchronized with the three-phase source. This task is performed with the use of power electronic converters, by the matrix converter in particular. Both mechanical transmission using the gear and converter losses determine the efficiency of the system. The smaller the difference between the input and output speed in the mechanical transmission, the smaller the losses [23]. Therefore, a modulation method which decreases the switching number in power converters with a small impact on the quality of voltage and current waveforms are desired. High-speed electrical machines are characterized by greater overall power than machines made for standard speeds, higher frequency of voltage at the terminals, and higher current [24].

Another factor legitimizing the frequency increase is the possibility of eliminating large electrolytic capacitors, which are the fastest deteriorating element in converters. This can be done by using a matrix converter that does not require such energy storage at all. Unfortunately, the use of standard power electronic switches and classic matrix converter topologies is limited by the upper allowable switching frequency. Therefore, the choice of such a solution may be resulting in a significant increase in the complexity of passive filters and a limit the converter dynamic, which is essential in small microgrids with distributed generation elements.

The paper proposes to use four matrix converters operating in parallel due to the modularity of such a solution and the increase in the range of operating currents. Due to new conditions, such as higher voltage frequency, modular nature of the topology and no requirement of galvanic isolation, the use of the coupled reactors circuits is an interesting idea. In addition, the leakage inductance of such reactors can also be used in controlling the power flow between the generator and the grid. The set and arrangement of the base vectors in the alpha–beta plain allow for the implementation of modulation methods with a lower switching frequency compared to Space-Vector Pulse Width Modulation (SVPWM) but with relatively good waveform quality. The switching frequency is equal to the generator frequency in particular. The purpose of conceptual research is shortly presented in the next subsection.

A multiphase transformer for multipulse rectifiers and similar topologies with the coupled reactors are known solutions. However, such an approach is mostly applied to systems that operate with the grid frequency. Considering the price of copper, these solutions are relatively expensive. The dimensions, as well as the price of these components, decrease with increasing nominal frequency. Thus, high-speed electrical machines seem to be the perspective area for the proposed converter topology. The SVPWM modulation allows for linear adjustment of both frequency and amplitude. However, it requires power electronic switches to operate at high frequency. The efficiency of that solution can be improved using the hybrid strategy of modulation. Consider the simplified gas turbine work profile shown in Figure 2.

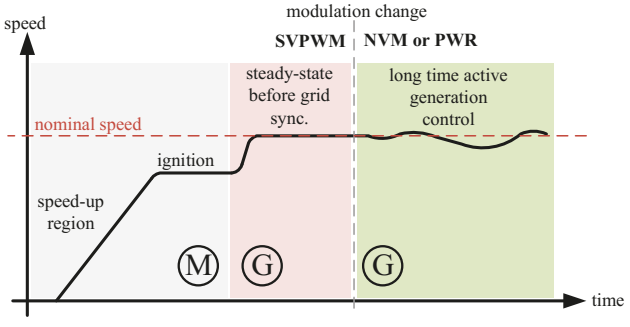


Figure 2. The simplified speed profile of the gas turbine: M—PMSM operates as a motor, G—PMSM operates as a generator, SVPWM—high-frequency modulation method based on the space-vector concept, Nearest Vector Modulation (NVM) and Pulse Width Modulation (PWR)—the low-switching frequency type of PWM modulation.

In the speed-up region, the required energy is supplied from the utility grid through the inverter converter controlled using the SVPWM algorithm. This modulation is used until the synchronisation with the grid. When the speed is stable, the long time active generation control begins, which can be performed using the proposed low-switching modulation approach. The main goal of the authors of the publication was to develop such modulation and preliminary simulation studies.

1.1. The Discrete Projection of Voltage Vectors

The essence of the solution is to achieve a very low operating frequency of power electronic switches. The forming of the output voltage in the proposed group of converters, while maintaining the power switches in the lowest operating frequency, can be formally presented as an effect of discrete projection of the reference vector, as shown in Figure 3.

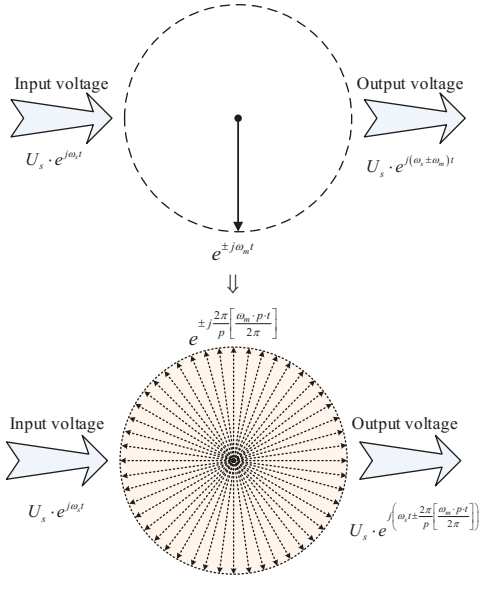


Figure 3. The general discrete reference vector projection concept: U_s—voltage amplitude, ω_s and ω_m pulsations, p a number of discrete voltage vectors [7].

Applying the idea of the projection in solutions composed of conventional 3 × 3 matrix converters, a multipulse output voltage can be obtained. Figure 4 shows a conventional matrix topology as the 3-pulse system, which does not contain any coupled reactors yet. The need of using the coupled reactors appears in the 6-pulse system. Such a converter is shown in Figure 5.

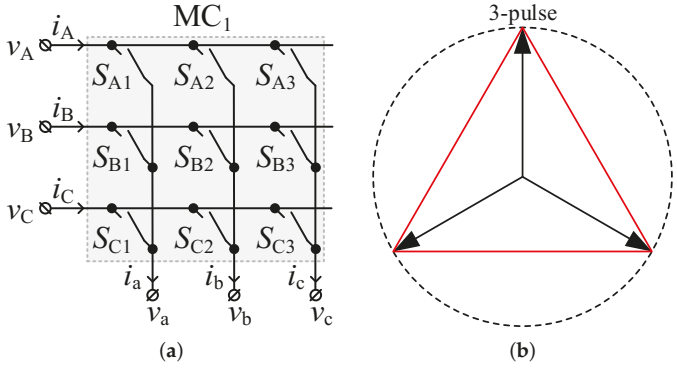


Figure 4. Conventional matrix converter as a 3-pulse system: (**a**) schematic diagram, (**b**) the voltages discrete projection.

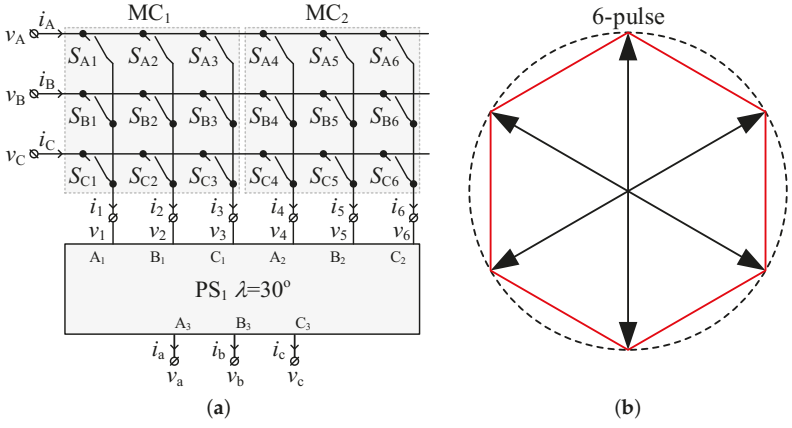


Figure 5. Two conventional matrix converters make the 6-pulse system: (**a**) schematic diagram, (**b**) the voltages discrete projection.

1.2. Coupled Reactors

Both solutions, 6-pulse and 12-pulse, require an appropriately coupled reactors arrangement [25]. The proposed topology, shown in Figure 6a, contains 36 bidirectional switches S_{A1}–S_{C12}, which are elements of four 4 matrix converters CMC_1–CMC_4 and 3 Phase Shifters (PS) PS_1, PS_2 and PS_3 respectively. The connection diagram of the simulation model of a three-phase type coupled reactor is shown in Figure 7.

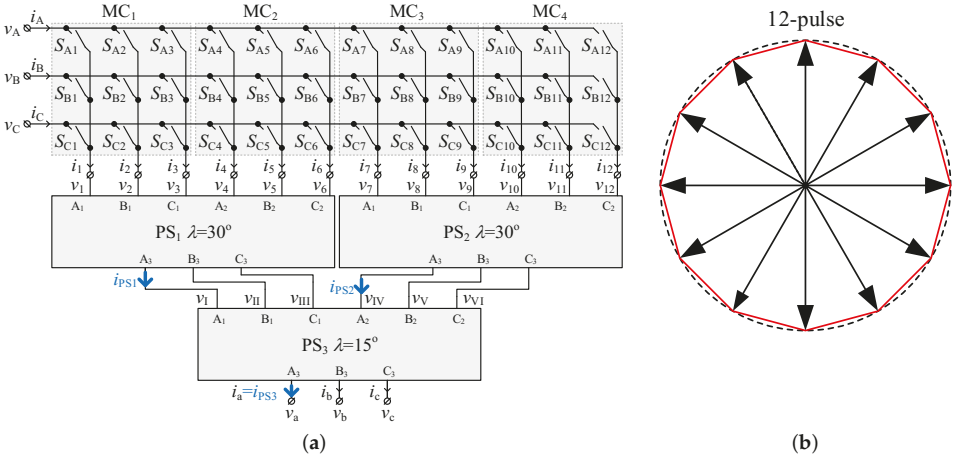


Figure 6. Four conventional matrix converters make the 12-pulse system: (**a**) schematic diagram, (**b**) the voltages discrete projection.

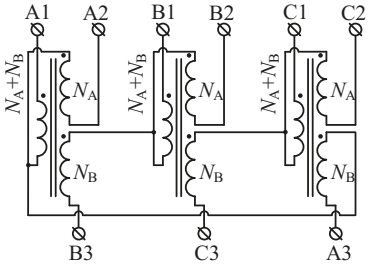


Figure 7. Phase Shifter schematic.

To obtain the desired phase shift angle λ the ratio of turns number N_A to N_B, should meet the following condition

$$n_{AB} = \frac{N_A}{N_B} = \frac{\sin\left(\frac{4\pi}{p_n} - \lambda\right)}{\sin(\lambda)} \tag{1}$$

where

p_n is the number of pulses of a given system and in the discussed example takes 12,
λ is a desired phase shift angle,
N_A and N_B is the ratio of turns number.

An example turns number for two shift angles are presented in Tables 1 and 2. The final number of windings depends on the adopted design parameters, in particular on the power of the system and the reactors' voltage spectrum. This aspect is not covered in this article.

Table 1. Turns number for shift angle equal to 30° (conversion values).

$N_A + N_B$	<100	<300	<1000
N_A	15	56	209
N_B	15	56	209

Table 2. Turns number for shift angle equal to 15° (conversion values).

$N_A + N_B$	<100	<300	<1000
N_A	41	153	571
N_B	15	56	209

The values of the turns number determine not only the shift angle but also certain properties of the presented topology, such as the amount of reactive power circulating between the coupled three-phase reactors and also the value of the maximum amplitudes of the output phase voltage. For simplicity of the rest text, let us assume that magnetic elements in circuits shown in Figure 7 are linear and lossless, and bidirectional power switches are ideal. The further part of the paper concerns the 12-pulse system only. The article is organised as follows. The space of the rotating vectors for 12-pulse MMCCR and the load voltage synthesis basic are presented in Section 2. While the control of output voltage amplitude using the low switching frequency modulation is proposed in the next section. Simulation results are shown and discussed in Section 4.

2. The Space of the Rotating Vectors for 12-Pulse MMCCR

The switch state is 0, if it is switched off, and takes unity if it is switched on. The states of all bidirectional switches can be defined by four switch state matrices $\mathbf{S}_{MC1}$–$\mathbf{S}_{MC4}$ expressed as follows

$$\mathbf{S}_{MC1} = \begin{bmatrix} S_{A1} & S_{B1} & S_{C1} \\ S_{A2} & S_{B2} & S_{C2} \\ S_{A3} & S_{B3} & S_{C3} \end{bmatrix} \tag{2}$$

$$\mathbf{S}_{MC2} = \begin{bmatrix} S_{A4} & S_{B4} & S_{C4} \\ S_{A5} & S_{B5} & S_{C5} \\ S_{A6} & S_{B6} & S_{C6} \end{bmatrix} \tag{3}$$

$$\mathbf{S}_{MC3} = \begin{bmatrix} S_{A7} & S_{B7} & S_{C7} \\ S_{A8} & S_{B8} & S_{C8} \\ S_{A9} & S_{B9} & S_{C9} \end{bmatrix} \tag{4}$$

$$\mathbf{S}_{MC4} = \begin{bmatrix} S_{A10} & S_{B10} & S_{C10} \\ S_{A11} & S_{B11} & S_{C11} \\ S_{A12} & S_{B12} & S_{C12} \end{bmatrix} \tag{5}$$

The modulation techniques presented in this article were developed for a system containing four conventional matrix converters. The proposed approach uses only six switch states among the 27 available. These selected vectors belong to the group of the rotating vectors [16]. Three of them rotate in a clockwise direction (Table 3), while the remaining three are counterclockwise (Table 4). In general, two collections of switch states can be proposed for the modulation. The first collection contains all combinations, which utilise the counterclockwise rotating voltage vectors. These states are described in Appendix A. The second collection, presented in Appendix A, comprises the clockwise rotating vectors. In summary, the total number of switch state combinations for MMCCR is equal to 3^4.

Table 3. Allowed $\mathbf{S}_{MCp}$ switch states.

States $\mathbf{S}_{MCp}$		
$\mathbf{S}_{Ip}$	$\mathbf{S}_{IIp}$	$\mathbf{S}_{IIIp}$
$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}$

Table 4. Allowed $\mathbf{S}_{MCn}$ switch states.

States $\mathbf{S}_{MCn}$		
$\mathbf{S}_{In}$	$\mathbf{S}_{IIn}$	$\mathbf{S}_{IIIn}$
$\begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$

The output voltage values for each converter depicted in Figure 7 can be calculated as follows

$$\begin{bmatrix} v_1 & v_2 & v_3 \end{bmatrix}^T = \mathbf{S}_{MC1} \cdot \begin{bmatrix} v_A & v_B & v_C \end{bmatrix}^T \tag{6}$$

$$\begin{bmatrix} v_4 & v_5 & v_6 \end{bmatrix}^T = \mathbf{S}_{MC2} \cdot \begin{bmatrix} v_A & v_B & v_C \end{bmatrix}^T \tag{7}$$

$$\begin{bmatrix} v_7 & v_8 & v_9 \end{bmatrix}^{\mathrm{T}} = \mathbf{S}_{\mathrm{MC3}} \cdot \begin{bmatrix} v_{\mathrm{A}} & v_{\mathrm{B}} & v_{\mathrm{C}} \end{bmatrix}^{\mathrm{T}} \tag{8}$$

$$\begin{bmatrix} v_{10} & v_{11} & v_{12} \end{bmatrix}^{\mathrm{T}} = \mathbf{S}_{\mathrm{MC4}} \cdot \begin{bmatrix} v_{\mathrm{A}} & v_{\mathrm{B}} & v_{\mathrm{C}} \end{bmatrix}^{\mathrm{T}} \tag{9}$$

According to the shown topology scheme, the matrix converters' output is connected with the PS PS_1 and PS_2 respectively. A simple circuit analysis, shown in Figure 7, leads to the following voltage synthesis matrices

$$\begin{bmatrix} v_{\mathrm{I}} \\ v_{\mathrm{II}} \\ v_{\mathrm{III}} \end{bmatrix} = \begin{bmatrix} v_2 & v_2 - v_5 & v_1 - v_4 \\ v_3 & v_3 - v_6 & v_2 - v_5 \\ v_1 & v_1 - v_4 & v_3 - v_6 \end{bmatrix} \begin{bmatrix} 1 \\ -k_1 \\ -k_2 \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} v_{\mathrm{IV}} \\ v_{\mathrm{V}} \\ v_{\mathrm{VI}} \end{bmatrix} = \begin{bmatrix} v_8 & v_8 - v_{11} & v_7 - v_{10} \\ v_9 & v_9 - v_{12} & v_8 - v_{11} \\ v_7 & v_7 - v_{10} & v_9 - v_{12} \end{bmatrix} \begin{bmatrix} 1 \\ -k_1 \\ -k_2 \end{bmatrix} \tag{11}$$

where the values of coefficients k_1 and k_2 can be calculated using the number of turns listed in Table 1

$$k_1 = \frac{N_{\mathrm{A}(30^\circ)} + N_{\mathrm{B}(30^\circ)}}{2N_{\mathrm{A}(30^\circ)} + N_{\mathrm{B}(30^\circ)}} \quad k_2 = \frac{N_{\mathrm{B}(30^\circ)}}{2N_{\mathrm{A}(30^\circ)} + N_{\mathrm{B}(30^\circ)}} \tag{12}$$

The final output voltage synthesis is realised by the third PS PS_3, according to the equation

$$\begin{bmatrix} v_{\mathrm{a}} \\ v_{\mathrm{b}} \\ v_{\mathrm{c}} \end{bmatrix} = \begin{bmatrix} v_{\mathrm{II}} & v_{\mathrm{II}} - v_{\mathrm{V}} & v_{\mathrm{I}} - v_{\mathrm{IV}} \\ v_{\mathrm{III}} & v_{\mathrm{III}} - v_{\mathrm{VI}} & v_{\mathrm{II}} - v_{\mathrm{V}} \\ v_{\mathrm{I}} & v_{\mathrm{I}} - v_{\mathrm{IV}} & v_{\mathrm{III}} - v_{\mathrm{VI}} \end{bmatrix} \begin{bmatrix} 1 \\ -k_3 \\ -k_4 \end{bmatrix} \tag{13}$$

where, as before, the coefficients k_3 and k_4 values can be calculated using the number of turns listed in Table 2 resulting in the following formula

$$k_3 = \frac{N_{\mathrm{A}(15^\circ)} + N_{\mathrm{B}(15^\circ)}}{2N_{\mathrm{A}(15^\circ)} + N_{\mathrm{B}(15^\circ)}} \quad k_4 = \frac{N_{\mathrm{B}(15^\circ)}}{2N_{\mathrm{A}(15^\circ)} + N_{\mathrm{B}(15^\circ)}} \tag{14}$$

Assuming that the MMCCR is supplied by a three-phase balanced AC voltage source and the load is symmetrical, the space vector α–β coordinates can be obtained using the simplified amplitude invariant Clarke transform

$$\begin{aligned} v_\alpha &= v_{\mathrm{a}} \\ v_\beta &= \frac{v_{\mathrm{b}} - v_{\mathrm{c}}}{\sqrt{3}} \end{aligned} \tag{15}$$

The space-vector diagram for $\mathbf{S}_{\mathrm{MC}p}$ switch state types, and $n_{\mathrm{AB1}} = n_{\mathrm{AB2}} = 209/209$, $n_{\mathrm{AB3}} = 571/209$, is shown in Figure 8. While the space-vector diagram for $\mathbf{S}_{\mathrm{MC}n}$ switch state types is illustrated in Figure 9. The obtained space-vector diagrams are not stationary and rotate with the frequency of the grid voltage.

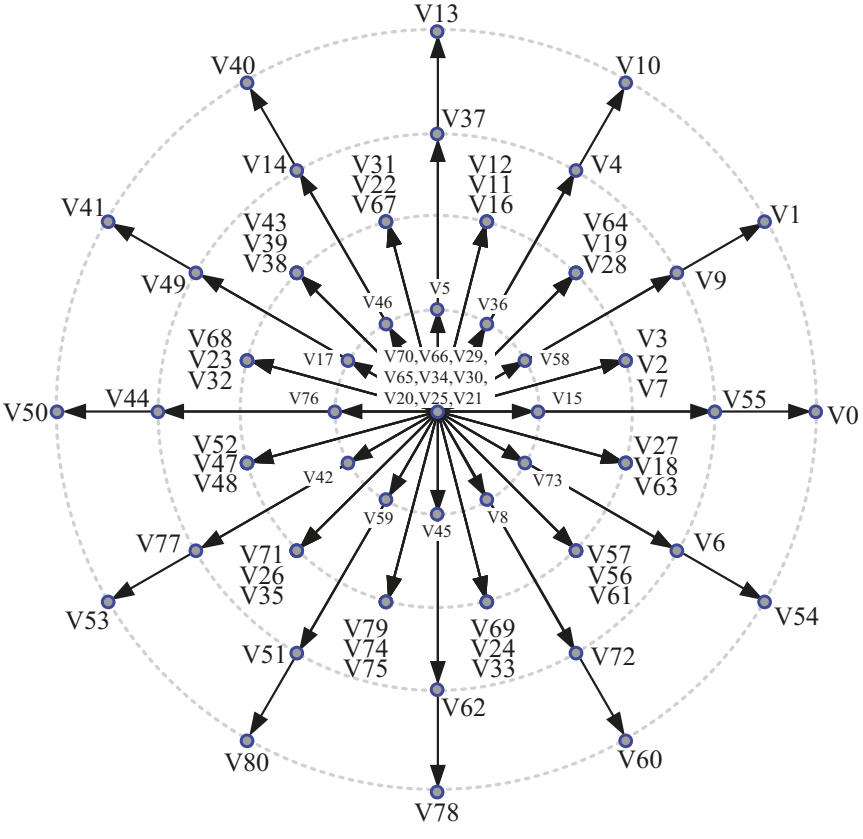


Figure 8. The space-vector diagram for $\mathbf{S}_{MCp}$ switch states.

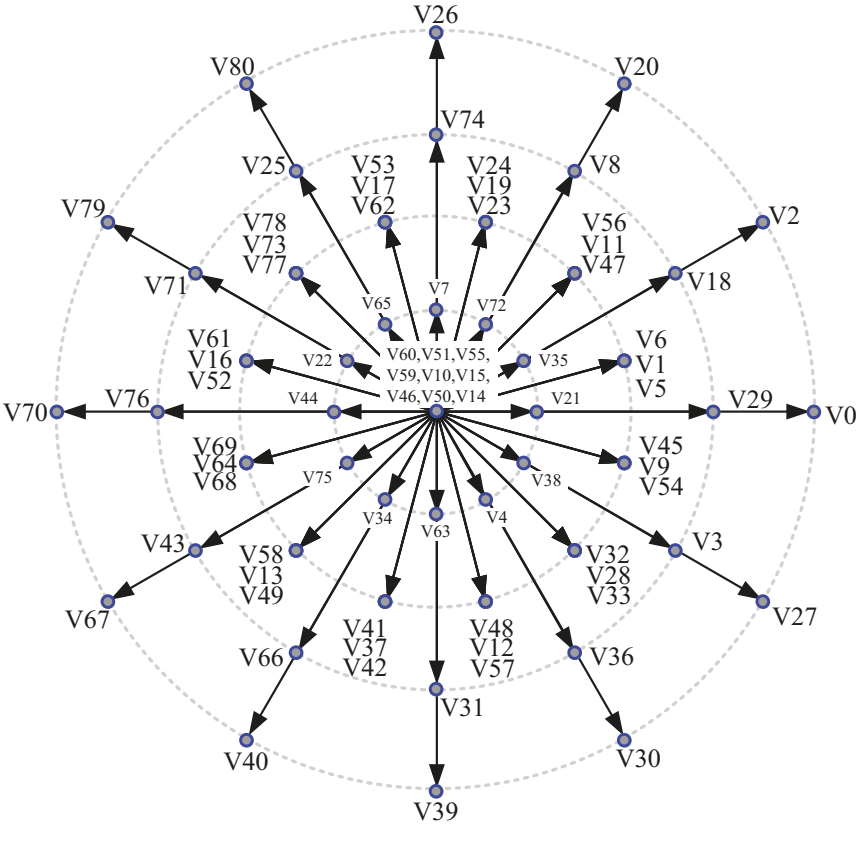


Figure 9. The space-vector diagram for $\mathbf{S}_{\mathrm{MC}n}$ switch states.

3. The Control of Output Voltage Amplitude Using the Low Switching Frequency Modulation

This section proposes two low switching frequency modulation methods—the Pulse Width Regulation PWR and Nearest Vector Modulation NVM. Both methods are successfully verified using PSIM simulation software. The load voltage is represented by one vector, which is rotating on the stationary, orthogonal α–β reference frame. This frame is built from the basic voltage vectors correspond to the switches states. The total number of switch state is equal to the M^N, where M is a number of allowed state combination across the one commutation cell, while N is a number of cells. Thus theoretically the total number of switch states is 3^{12} for the proposed converter topology. Due to the concept of magnetically coupled using the coupled reactors presented in [25] only the rotating vectors are allowed. The stationary and the zero vectors from the conventional matrix converter space-vector frame are not suitable for that kind of the reactors' circuit. There are six rotating vectors allowed for each of the conventional matrix converters. Two collections can be distinguished—the first covers vectors, that rotate clockwise—while the second set represents vectors rotate counterclockwise. Thus, if the number of the conventional matrix converter is equal to 4, as shown in Figure 6 the total number of selected vectors is reduced to 3^4. The load voltage can

be synthesised using a variety of switch states sequence. However, due to the requirement to minimise losses during modulation, only the nearest vectors are applied within the modulation period.

3.1. Pulse Width Regulation

The synthesis of voltages in the MMCCR with modular structure can be directed to the high efficiency of the power conversion system also oriented to decreasing the number of switching. However, the operating frequency should be chosen so as to preserve the multipulse nature of the generated phase voltages with the assumption of the amplitude output voltage regulation. Considering the vectors arrangement shown in Figure 10, the vectors V0–V54 belong to the outer circle with radius is equal to 1.0 p.u., while the vectors V55–V6 are located on an inner circle with radius of 0.732 p.u.. The shown reference voltage vector V_{REF} lies exactly between vectors V9 and V1 area, which refers to a sector 2 in propose modulation scheme. To obtain the symmetry effect of the states sequence in the time window corresponding to the modulation period T_{PWR}, the three–step switch states sequence has been proposed. The first three sequences are shown in Table 5. The PWR duty cycles, for each sector, can be calculated as follows

$$\begin{array}{c} d_H = \frac{V_{REF}-V_L}{V_H-V_L} \\ d_L = 1 - d_H \end{array} \tag{16}$$

where $V_H = 1.0$, $V_L = 0.732$, and d_H corresponds to the longer vector. An example waveform of the output voltage is shown in Figure 11.

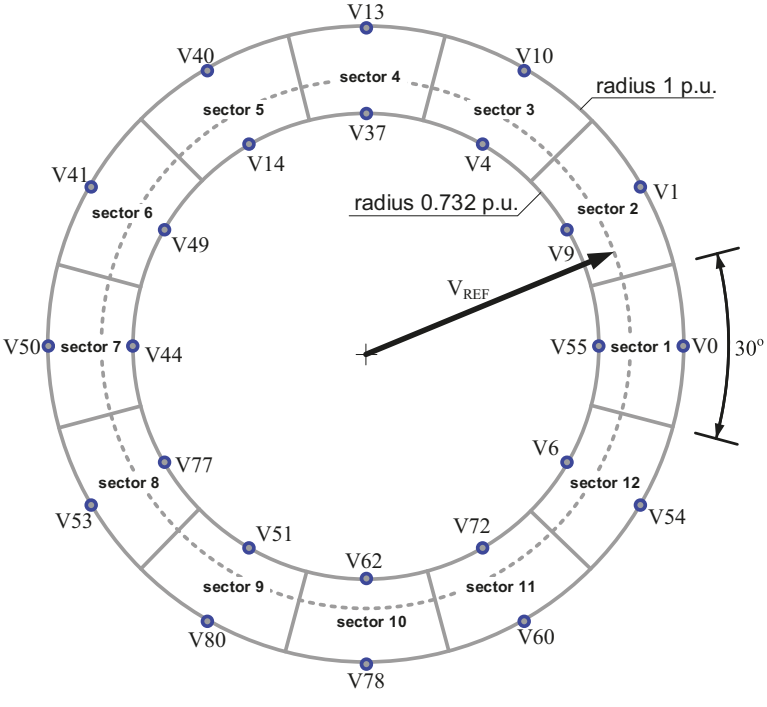


Figure 10. The PWR modulation workspace for $\mathbf{S}_{MCp}$ switch states.

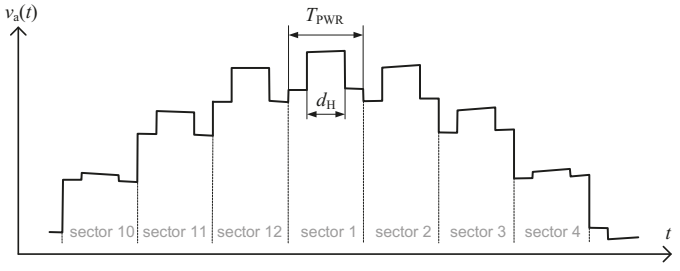


Figure 11. Fragment of phase voltage waveform for the PWR modulation using the $\mathbf{S}_{MCn}$ states.

The coordinates of the reference output voltage V_{REF} can be defined according to the selected type of switch state matrices. For selected $\mathbf{S}_{MCn}$ the $\alpha\beta$ coordinates of the V_{REF}, can be calculated

$$\begin{aligned} v_\alpha^* &= q \cdot \cos\left(\omega_i \cdot (k_f + 2) \cdot t\right) \\ v_\beta^* &= q \cdot \sin\left(\omega_i \cdot (k_f + 2) \cdot t\right) \end{aligned} \tag{17}$$

while for $\mathbf{S}_{MCp}$ we obtain

$$\begin{aligned} v_\alpha^* &= q \cdot \cos\left(\omega_i \cdot (k_f - 2) \cdot t + \tfrac{2\pi}{3}\right) \\ v_\beta^* &= q \cdot \sin\left(\omega_i \cdot (k_f - 2) \cdot t + \tfrac{2\pi}{3}\right) \end{aligned} \tag{18}$$

where

v_α^*—reference α coordinate,
v_β^*—reference β coordinate,
ω_i—input voltage pulsation,
$k_f = \omega_o/\omega_i$—pulsation ratio, and
$q = V_{REF}/V_i$ is the voltage transfer ratio.

Table 5. Example the switch states sequences in the first 3 sectors.

Type	n_{AB3}	Sector 1	Sector 2	Sector 3
$\mathbf{S}_{MCp}$	571/209	V55–V0–V55	V9–V1–V9	V4–V10–V4
$\mathbf{S}_{MCn}$	571/209	V29–V0–V29	V18–V2–V18	V8–V20–V8

3.2. The Nearest Vector Modulation

The second approach is based on the minimum distance selection criterion, in which a distance is measured between the reference vector and basic vectors belonging to the collection of rotating voltage vectors. Another control concept, also leading to the minimisation of the number of switching, depends on choosing the one space-vector within the modulation period, which is geometrically closest to the reference vector with coordinates v_α^* and v_β^*. Theoretically, the number of required distances depends on the regulation range of the output phase voltage and takes the maximum value equal to 49 (48 active vectors and one zero vector). Since the following minimum value is needed

$$r_k = \sqrt{(v_\alpha^* - v_{\alpha k})^2 + \left(v_\beta^* - v_{\beta k}\right)^2} \tag{19}$$

in the decision process, finally another expression can be chosen

$$g_k = (v_\alpha^* - v_{\alpha k}) \cdot (v_\alpha^* - v_{\alpha k}) + \left(v_\beta^* - v_{\beta k}\right) \cdot \left(v_\beta^* - v_{\beta k}\right) \tag{20}$$

where

k—the switch state index, form 1 to 49,
g_k—the proposed distance function,
$v_{\alpha k}$—vector α coordinate for k switch state,
$v_{\beta k}$—vector β coordinate for k switch state.

The new proposed expression contains no square root operation. Further optimisation of the algorithm may consist of taking into account the redundancy of certain switch states. The redundancy, in this case, means that the same voltage vector can be assigned to at least two switch states. In this paper, this aspect is omitted in further discussion. The algorithm calculations should be performed quite frequently to maintain best output voltage quality as possible. In order to counteract the appearance of undesirable effects associated with the so-called a short impulse, attention should be paid to the commutation capabilities of the used bi-directional switch. The commutation process should be appropriately performed according to the dynamic properties of the switch included in the datasheet. This issue is more important in medium and high power application characterised by the large currents values. Overvoltage across the switch can damage it. The proposed solution is able to be discussed for the nominal frequencies (50 Hz or 60 Hz) but is promising for higher frequencies used in gas turbines, ultrasounds, and high-speed drives. Such applications require modern transistors based on GaN or SiC technology. The time of the commutation process is much less compared to the IGBT switch counterparts. That feature has critical importance for NVM modulation, wherein the short impulse problem can appear. This aspect in the algorithm can be limited to the adoption of a specific frequency of the algorithm's call or using the hysteresis mechanisms in the sequence selection process. The quality of the proposed modulation method can be assessed using the error rate defined as follows

$$\varepsilon_{\mathrm{RMS}} = \sqrt{\frac{1}{T_{50\mathrm{Hz}}} \cdot \int_0^{T_{50\mathrm{Hz}}} \left(\frac{v_{\mathrm{a}}^* - v_{\mathrm{a}}}{v_{\mathrm{a}}^*} \right)^2 \mathrm{d}t} \tag{21}$$

The results are presented in Figure 12. The shown waveform contains four local optimum q values, which correspond to the optimal multipulse operation.

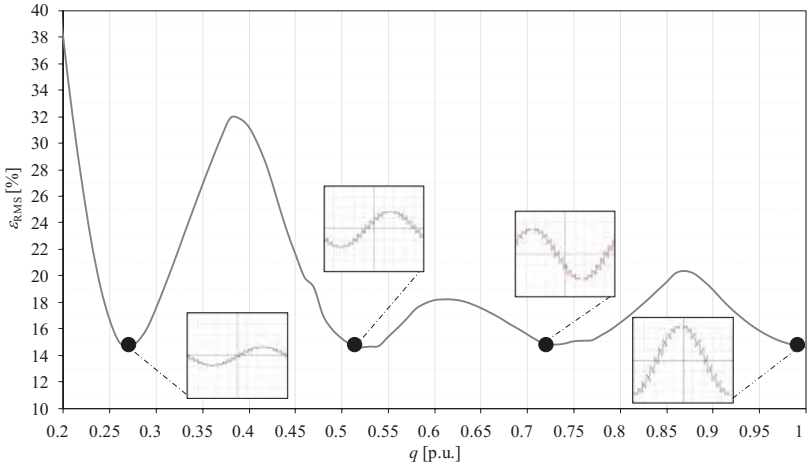


Figure 12. An error rate, defined by (21), for proposed NVM method: $n_{AB1} = n_{AB2} = 209/209$, $n_{AB3} = 571/209$, $k_f = 1/12$.

4. Research

Initial simulation studies focused on selected modulation techniques. The converter MMCCR topology is new; therefore, it was necessary to develop modulation algorithms from scratch. Three types of modulation have been developed:

- SVPWM—this type of modulation belongs to the high-frequency switching technique, is characterised by good accuracy. The nearest three vector modulation has been adopted and developed for a new space-vector diagram presented in the previous section. The formulas of the PWM duty cycles can be found in the paper [26].
- PWR—this type of modulation allows for an amplitude control only in the limited range of modulation index with the number of switching is less than in the SVPWM. However, the precise amplitude control is worst in comparing with the SVPWM.
- NVM—modulation with the minimum number of switching operations, dedicated to working in a steady state. The field of application may be inverters operating with a constant output frequency.

The results are presented in two subsections. Voltage and current waveforms for inverter operation with RL load are presented first. The next subsection is dedicated to a potential application in a system with a high-speed PMSM generator, as mentioned in the introduction.

4.1. PWR and NVM Modulations in the MMCCR Inverter Mode of Operation

Simulation has been performed using DLL block as a DSP platform emulator works with 50 µs step. The markings used in demonstrated figures are: v_a—load phase voltage, v_A—grid phase voltage, $i_{a,b,c}$—load currents, and $i_{A,B,C}$—input currents. Two load models parameters sets are applied, which are listed in Table 6. All waveforms are presented in p.u. unit.

Table 6. 20 kVA/400 V load models simulation parameters.

	R [Ω]	L [H]	Z [Ω]	PF
model-1	7.75	0.0008	8.0	0.97
model-2	4	0.0028	8.0	0.5

Simulation tests for PWR modulation were carried for the model-1, which was characterised by a power factor of 0.97. The proposed PWR modulation has been verified for both types of switches state sequence. Results for $\mathbf{S}_{\mathrm{MC}n}$ switches state sequence are shown in Figures 13 and 14, while the waveforms obtained for opposite rotation, $\mathbf{S}_{\mathrm{MC}p}$ switch state sequences, are illustrated in Figures 15 and 16.

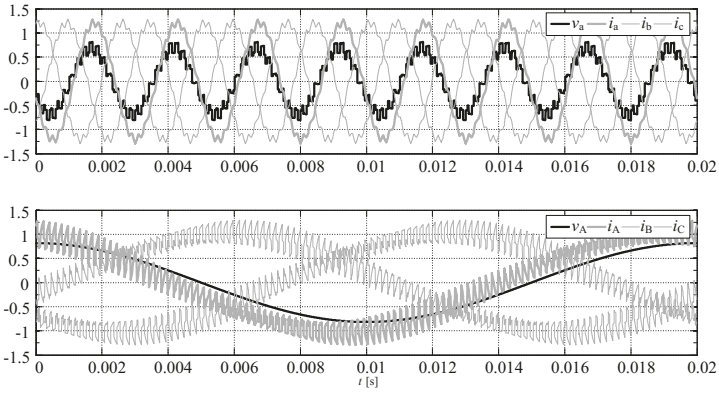


Figure 13. The waveforms of the phase voltages and currents at the output and input of the PWR controlled MMCCR for the $\mathbf{S}_{\mathrm{MC}n}$ switch state sequences: load model-1, $n_{\mathrm{AB1}} = n_{\mathrm{AB2}} = 209/209$, $n_{\mathrm{AB3}} = 571/209$, $q = 0.866$, $k_f = 8$.

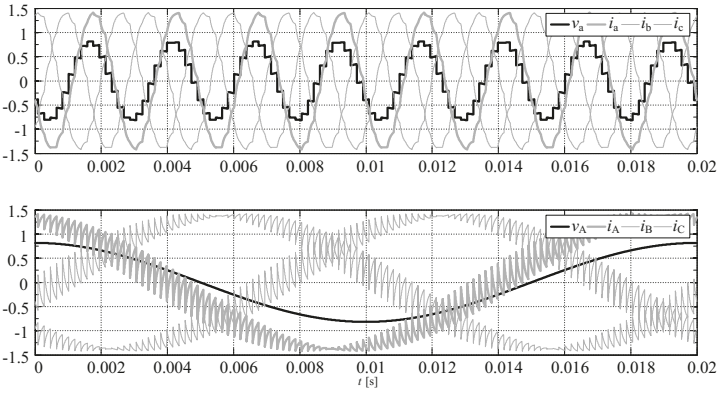


Figure 14. The waveforms of the phase voltages and currents at the output and input of the PWR controlled MMCCR for the $\mathbf{S}_{\mathrm{MC}n}$ switch state sequences: load model-1, $q = 1.0$, $k_f = 8$.

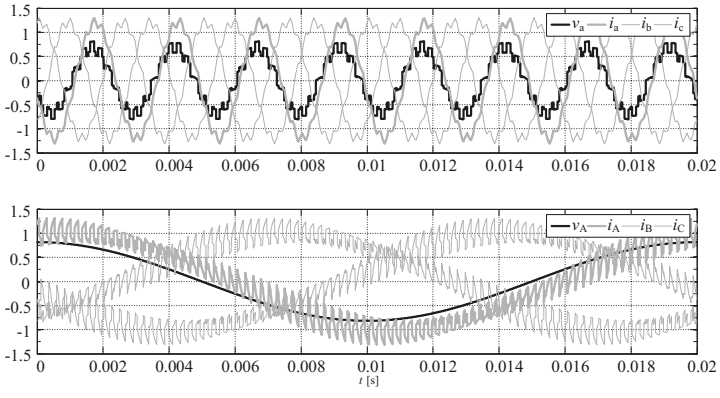


Figure 15. The waveforms of the phase voltages and currents at the output and input of the PWR controlled MMCCR for the $\mathbf{S}_{\mathrm{MC}p}$ switch state sequences: load model-1, $q = 0.866$, $k_f = 8$.

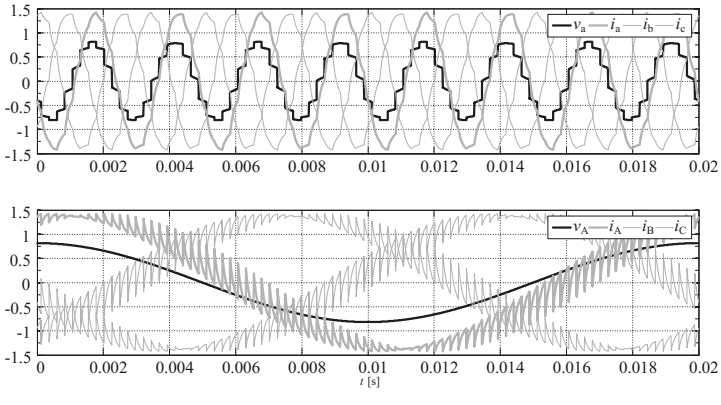


Figure 16. The waveforms of the phase voltages and currents at the output and input of the PWR controlled MMCCR for the $\mathbf{S}_{\mathrm{MC}p}$ switch state sequences: load model-1, $q = 1.0$, $k_f = 8$.

According to the proposed concept, for q equal to unity, the output voltage is formed based only on the vectors located on the outer circle. In this case, the system works in 12-pulse mode with the optimal number of switching. Note that in all simulations, a standard input low pass filter has not been used, to demonstrate the unfiltered input current shape.

Comparison of load current Total Harmonic Distortion (THD) and average switching frequency for PWR modulation using the $\mathbf{S}_{\mathrm{MC}n}$ and $\mathbf{S}_{\mathrm{MC}p}$ switch state sequences for $k_{\mathrm{f}} = 8$ is characterised in Table 7.

Table 7. Comparison of load current THD and average switching frequency for PWR modulation using the $\mathbf{S}_{\mathrm{MC}n}$ switch state sequences and $k_{\mathrm{f}} = 8$.

	$\mathbf{S}_{\mathrm{MC}n}$ Switch State Type						
q	0.732	0.75	0.8	0.85	0.9	0.95	1
THD i_{a} [%]	3.15	3.35	4.8	5.4	5.2	4.3	3.1
f_{switch} [Hz]	1350	3125	3125	3125	3125	3125	450
	$\mathbf{S}_{\mathrm{MC}p}$ Switch State Type						
q	0.732	0.75	0.8	0.85	0.9	0.95	1
THD i_{a} [%]	4.15	4.6	6.2	7.0	6.5	5.5	4.1
f_{switch} [Hz]	1050	2450	2450	2450	2450	2450	350

As can be deduced low switching frequency MMCCR operation is achieved for voltage q equal to the radius shown in Figure 10. An important feature of the matrix topology is the ability to the regulation of input angle, defined as displacement between the input current and grid voltage. The range of an angle regulation relies on the load parameters. In a simple way, the desired input angle can be selected using the $\mathbf{S}_{\mathrm{MC}n}$ or $\mathbf{S}_{\mathrm{MC}p}$ switch state sequences. The result of the rapid change of the switch state sequence for model-2 parameters is shown in Figure 17, in which an input angle ϕ is approximately equal to $\pi/3$. Note that the proposed PWR method is elaborated only for a limited range.

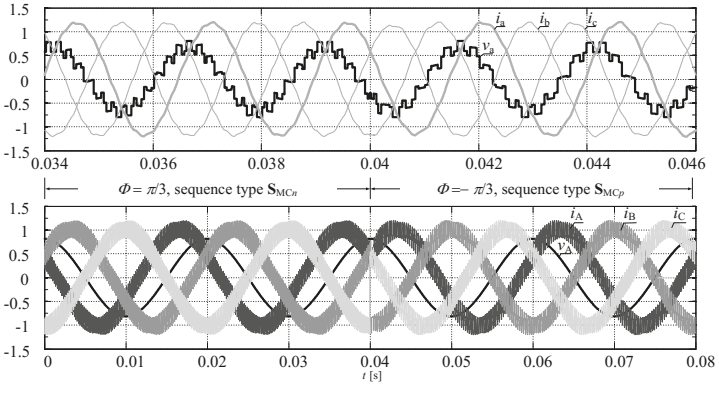


Figure 17. The zoom of the rapid change of switch sequence type for PWR modulation and load model-2, $q = 0.866$, and $k_f = 8$.

The proposed PWR modulation is not an accurate voltage synthesis method. Formula (16) calculates the proportion only in an estimated way, assuming that the voltages are constant in the modulation period.

A simulation has been performed in which the Root Mean Square (RMS) value and THD of the load current have been calculated. Figure 18 shows maximal magnetic flux values referred to the case of the 50 Hz output waveform generation in function of voltage transfer ratio q and output frequency ratio k_f. On the basis of the collected data, it was confirmed that the magnetic flux value is linearly dependent on the output frequency. On the other hand, a smaller flux allows for a smaller design of the coupled reactor circuit. Therefore, the proposed solution will work better in applications with a higher fundamental frequency.

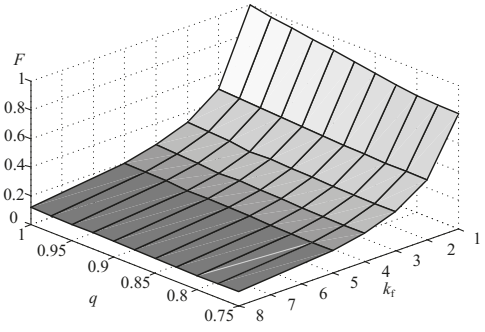


Figure 18. The maximal relative magnetic flux F in PS_3 coupled reactor in function of voltage transfer ratio q and output frequency ratio k_f.

Figure 19 presents an example of current and voltage waveforms in the case of 400 Hz voltage generation using the NVM method. The presented fragment of the waveforms refers to the case when the output voltage amplitude is gradually increased. The results were obtained for the load model-1.

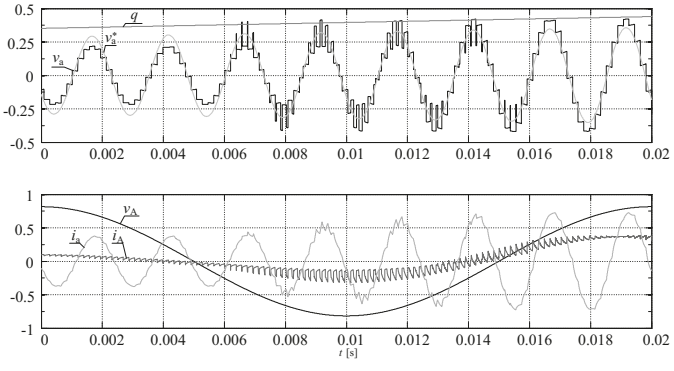


Figure 19. Example output voltage waveforms, for NVM modulation, during gradually increasing the voltage gain q from 0.27 to 0.43 for $k_f = 8$.

Figure 20a shows a comparison of THD modulation methods described in the article. Obviously, curves in the figure are not similar because they represent different approaches to low-frequency modulation. To formulate conclusions one should also consider the results presented in Figure 20b, in which the RMS load currents have been compared to the reference current.

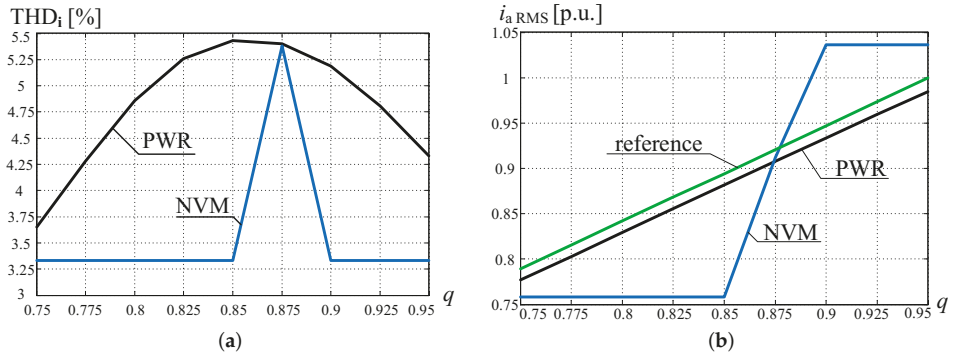


Figure 20. The comparison of the PWR and NVM modulation methods during the inverter operation: (**a**) the load current total harmonic distortion in the applicable range of modulation index, (**b**) the load current RMS value comparison of reference and proposed modulation.

4.2. A Potential Application in a System with a High-Speed PMSM Generator

The proposed MMCCR converter can be applied in a system with a high-speed PMSM generator. Figure 21 shows a simplified circuit for simulation tests, while the proposed control diagram is presented in Figure 22. The purpose of the simulation tests was as follows:

- comparing the converters CMC and MMCCR controlled by SVPWM modulation,
- investigating the possibility of the system control for active NVM modulation with the low-frequency switching within a steady-state operation (shown in Figure 2).

Precise amplitude control is required during generator start-up and synchronisation with the grid. The SVPWM method based on the three nearest vectors selection has been used. At this stage, simulation studies focused on the verification of the possibility of controlling the active component of the generator current, estimating the THD for selected waveforms, and determining the number of switching of power electronic switches.

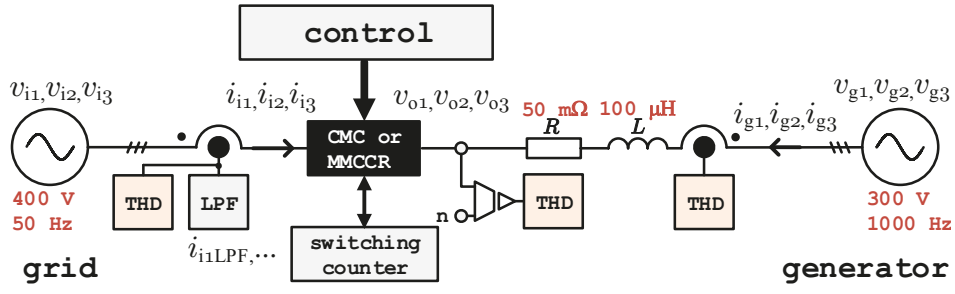


Figure 21. A potential application scheme with a high-speed PMSM generator: CMC—conventional matrix converter, MMCCR—the proposed converter, THD—calculation of the total harmonic distortion block, LPF—the low–pass filter, and "n"—the star point for the phase voltage measurement.

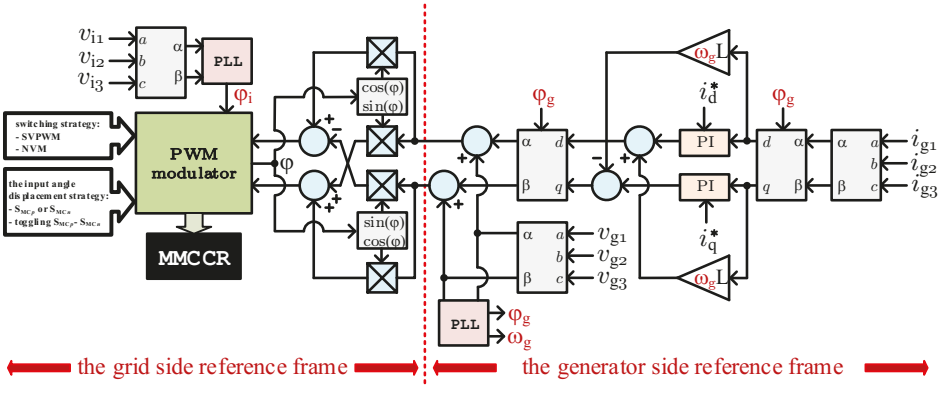


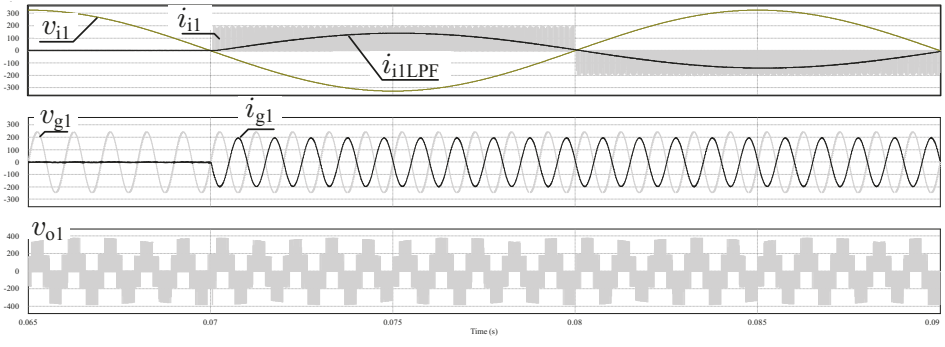
Figure 22. The proposed control scheme: PLL—phase-locked loop, MMCCR—the proposed converter, PI—standard proportional integral controller, φ_i—grid's voltage angle, φ—the synchronisations angle, φ_g—generator's voltage angle, i_d^*—an active reference current for generator, i_q—a reactive reference current for generator, $\omega_g = \omega_m$—for simplicity, mechanical pulsation is equal to electrical pulsation.

Selected results of the comparison CMC and MMCCR converters during SVPWM modulation are shown in Table 8. All presented measurements were carried out for the modulation period equal to 10 µs and the set active current of the generator 200 A. For the MMCCR converter, compared to the CMC topology, the THD factor of the input current and the output voltage is over 2.5 times lower, while maintaining a constant value of the modulation period. In addition, the quality of the generator current is better.

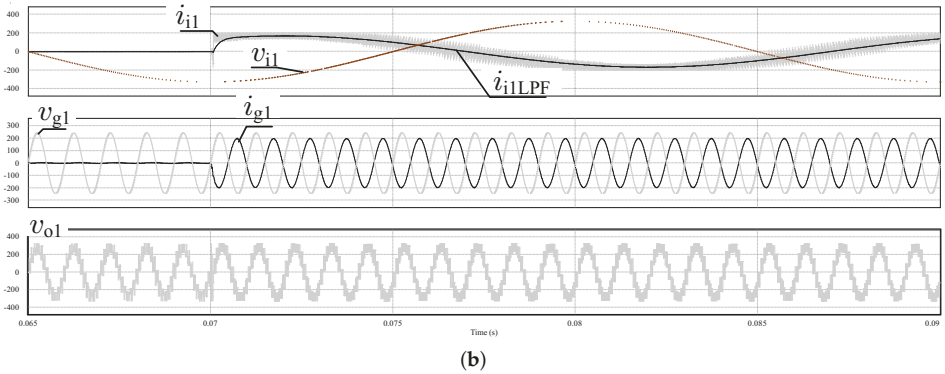
Table 8. Selected results of the comparison CMC and MMCCR converters during SVPWMmodulation.

Converter Type	THD(i_{i1})	THD(v_{o1})	THD(i_{g1})	The Relative Number of Switching Operations
CMC	74%	73%	1.6%	100%
MMCCR	28%	26%	0.85%	≃50%

Example waveforms of currents and voltages are shown in Figure 23. The simulation performed for the step change of the reference active generator current, from 0 to 200 A (approximately 75 kW power) in $t = 0.07$ s. As can be seen, the shape of the input current and the voltage generated by the converters have differed. The MMCCR generates a quasi multilevel voltage and the input current shape is near to the sinusoidal waveform. The input current spectrums for both converters are presented in Figure 24.



(**a**)



(**b**)

Figure 23. The step change 0–200 A of the reference active generator current in $t = 0.07$ s: (**a**) for CMC converter, (**b**) for MMCCR converter.

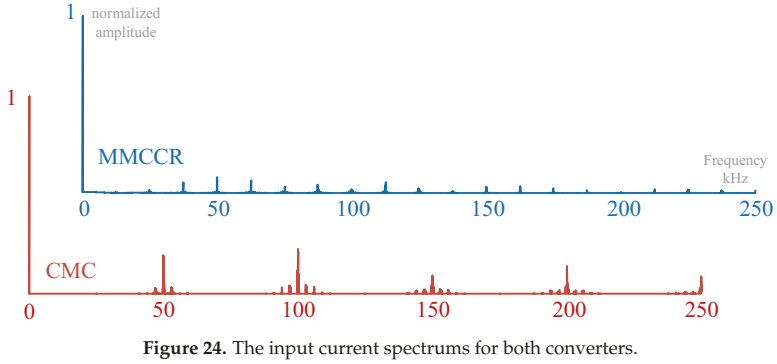


Figure 24. The input current spectrums for both converters.

The proposed MMCCR topology contains four matrix converters and three-phase shifter circuits. As mentioned in an introduction section, the power is equally divided with among these matrix converters. Example PS currents i_{PS1}, i_{PS2}, and i_{PS3} are shown in Figure 25.

In steady-state it is possible to change the control strategy. The SVPWM method can be replaced by NVM modulation, which is characterised by a much lower operating frequency of power electronic switches. However, new PI controllers settings should be selected in this case to keep the staircase character of the generated voltage. An obtained example of converter's voltage and other waveforms, during an active NVM modulation, is shown in Figures 26 and 27.

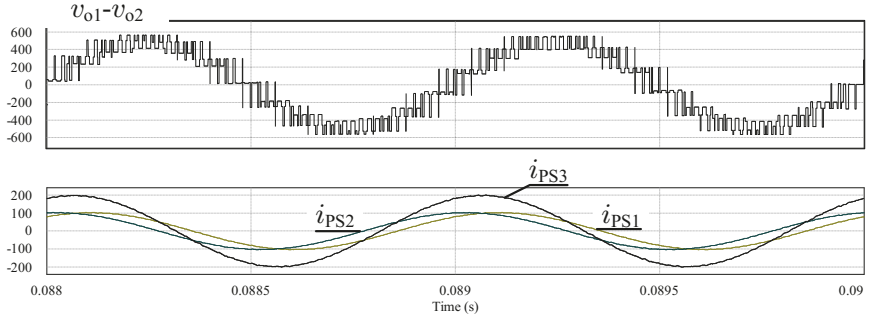


Figure 25. Converter's line–to–line output (correspond to Figure 21) voltage and the current sharing among the PS shown in Figure 6—SVPWM modulation.

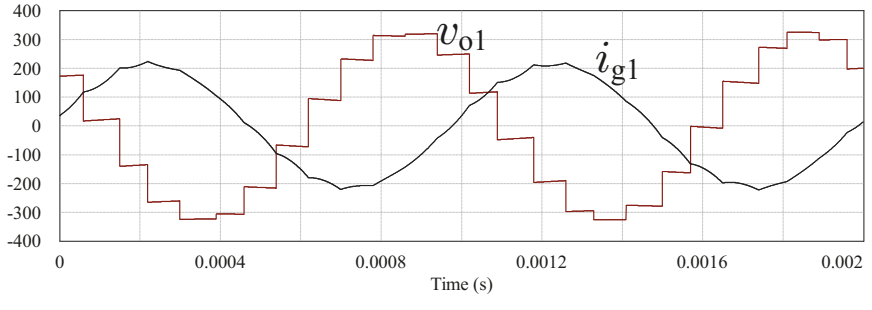


Figure 26. MMCCR converter' output voltage v_{o1} and the generator current i_{g1} for NVM modulation: THD(i_{g1}) = 3.5% and THD(v_{o1}) = 16%.

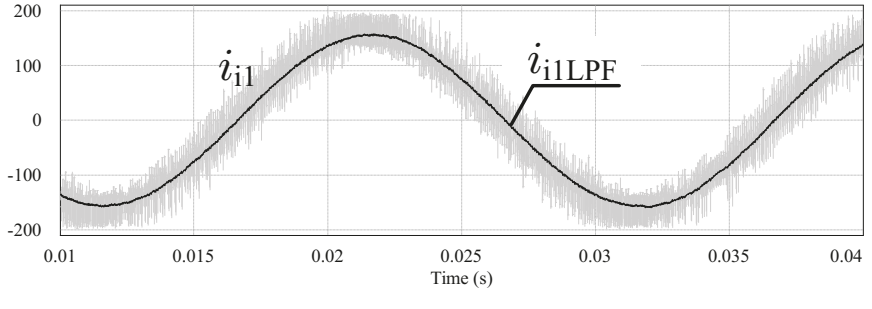


Figure 27. An input current i_{i1} and its filtered waveform i_{i1LPF} for NVM modulation: THD(i_{i1}) = 26%.

5. Conclusions

This article studies nature and presents conceptual research and discusses the different Pulse Width Modulation (PWM) strategies for operating, with a low-switching frequency for the proposed topology. It shows how the unconventional combination of CMC modules and CR could improve the quality of energy conversion. The paper also presents how this solution may be specifically appropriate for the high power systems, that are supplied by the high AC frequency sources, such as the high-speed generators or airport terminals' supply of 400 Hz.

The main features of the proposed approach are as follows:

- The use of coupled reactors allows the generation of voltages with staircase character (see Figure 26) with relatively low switching frequency operation, which depends on the value of the reference voltage. However, the staircase-type waveforms of the load voltages are obtained only for maximum voltage gain (for both NVM and PWR modulations) or for the certain values of the NVM modulation index, as shown in Figure 12.
- Increasing the number of CMC devices allows for the achievement of the voltage gain close to unity. For CMC, the voltage gain is no greater than 0.866, while for the proposed topology, the generated maximum amplitude is 11% greater. However, four PS circuits are required. Therefore, and also due to the volumes of coupled reactors, the application of the discussed system is the most rational in the case of high frequencies at the output and/or output of the CMC, e.g., in gas turbines.
- The content of higher harmonics in the voltage, generated using PWR and NVM algorithms, is not linearly dependent on the reference load voltage value, this can make application of the proposed solution problematic in a full range of load voltage amplitude changes. Therefore, the proposed type of amplitude control should be used and optimised preferably in systems with a fixed output frequency. Only the SVPWM method, based on the rotating vectors, can be utilised in a full range of the modulation index.
- In comparison with high-frequency methods such as PWM, both PWR regulation and NVM modulation are not precise methods generating output voltages. Therefore, the proposed solution will not find application even in electric drive with high requirements for dynamics. However, it can be assumed that apart from reducing switching losses, the EMI level will also decrease. Due to these properties, the presented modulation methods can be applied in converters for high-speed generators/motors and also the onboard power supply.

In the case of MMCCR control with NVM modulation, it is possible to achieve a reasonable compromise between low THD value and relatively low frequency of power switches. However, as shown in Figure 20, in case of NVM modulation, it is difficult to control the output current/voltage with reference amplitude changes. Special switchable algorithms are required. Much better control possibilities, albeit at the cost of increasing THD and about 2 times the switching frequency, can be achieved when implementing the PWR algorithm. A further increase in the precision of the generation and control range of the output current/voltage is possible by means of SVPWM modulation for two rotating spatial vectors. This results in higher switching frequency and control calculation problems for CMC systems, in particular for this 12-pulse MMCCR. In order to reduce the importance of these problems and the related requirements on the capabilities of processor controllers, the authors initially propose to use the barycentric coordinate method [19], which unifies and simplifies calculations.

The research of this method in relation to the MMCCR system, including the hybrid method [25], allowing to minimize the frequency of connections in the converter at fixed points will be presented in the next paper. This study article does not in any way pretend to present the full spectrum of problems associated with MMCCR systems. Its main objective was only to present the possibilities and basic properties of equalising typical CMC modules with chokes coupled with overall power of no more than

about 30% of the rated power of the whole system. The above objective also includes a general discussion of dedicated control algorithms. Considering the generality and the material's size, only the most important theoretical issues verified by simulation are presented. Experimental research on specific cases will be the subject of further publications in the near future.

Author Contributions: Conceptualisation: P.S. and N.S., investigation and simulation: P.S. and J.L., validation, formal analysis: A.U., final editing: P.S. and E.R.-C. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

CMC	Conventional Matrix Converter
CMCs	Conventional Matrix Converters
CRs	Coupled Reactors
EMI	Electromagnetic Intereference
MMCCR	Multipulse Matrix Converter with Coupled Reactors
NVM	Nearest Vector Modulation
PS	Phase Shifters
PWM	Pulse Width Modulation
PWR	Pulse Width Modulation
RMS	Root Mean Square
SVPWM	Space-Vector Pulse Width Modulation
THD	Total Harmonic Distortion
VFD	Variable Frequency Drive

Appendix A

Table A1. The $\mathbf{S}_{\mathrm{MC}n}$ Switch States.

	$s_{A1}\ldots s_{C3}$	$s_{A4}\ldots s_{C6}$	$s_{A7}\ldots s_{C9}$	$s_{A10}\ldots s_{C12}$
V0	001-100-010	001-100-010	001-100-010	001-100-010
V1	001-100-010	001-100-010	001-100-010	010-001-100
V2	001-100-010	001-100-010	001-100-010	100-010-001
V3	001-100-010	001-100-010	010-001-100	001-100-010
V4	001-100-010	001-100-010	010-001-100	010-001-100
V5	001-100-010	001-100-010	010-001-100	100-010-001
V6	001-100-010	001-100-010	100-010-001	001-100-010
V7	001-100-010	001-100-010	100-010-001	010-001-100
V8	001-100-010	001-100-010	100-010-001	100-010-001
V9	001-100-010	010-001-100	001-100-010	001-100-010
V10	001-100-010	010-001-100	001-100-010	010-001-100
V11	001-100-010	010-001-100	001-100-010	100-010-001
V12	001-100-010	010-001-100	010-001-100	001-100-010
V13	001-100-010	010-001-100	010-001-100	010-001-100
V14	001-100-010	010-001-100	010-001-100	100-010-001
V15	001-100-010	010-001-100	100-010-001	001-100-010
V16	001-100-010	010-001-100	100-010-001	010-001-100
V17	001-100-010	010-001-100	100-010-001	100-010-001
V18	001-100-010	100-010-001	001-100-010	001-100-010
V19	001-100-010	100-010-001	001-100-010	010-001-100
V20	001-100-010	100-010-001	001-100-010	100-010-001
V21	001-100-010	100-010-001	010-001-100	001-100-010
V22	001-100-010	100-010-001	010-001-100	010-001-100
V23	001-100-010	100-010-001	010-001-100	100-010-001
V24	001-100-010	100-010-001	100-010-001	001-100-010
V25	001-100-010	100-010-001	100-010-001	010-001-100
V26	001-100-010	100-010-001	100-010-001	100-010-001
V27	010-001-100	001-100-010	001-100-010	001-100-010
V28	010-001-100	001-100-010	001-100-010	010-001-100
V29	010-001-100	001-100-010	001-100-010	100-010-001

Table A1. *Cont.*

	$S_{A1} \ldots S_{C3}$	$S_{A4} \ldots S_{C6}$	$S_{A7} \ldots S_{C9}$	$S_{A10} \ldots S_{C12}$
V30	010-001-100	001-100-010	010-001-100	001-100-010
V31	010-001-100	001-100-010	010-001-100	010-001-100
V32	010-001-100	001-100-010	010-001-100	100-010-001
V33	010-001-100	001-100-010	100-010-001	001-100-010
V34	010-001-100	001-100-010	100-010-001	010-001-100
V35	010-001-100	001-100-010	100-010-001	100-010-001
V36	010-001-100	010-001-100	001-100-010	001-100-010
V37	010-001-100	010-001-100	001-100-010	010-001-100
V38	010-001-100	010-001-100	001-100-010	100-010-001
V39	010-001-100	010-001-100	010-001-100	001-100-010
V40	010-001-100	010-001-100	010-001-100	010-001-100
V41	010-001-100	010-001-100	010-001-100	100-010-001
V42	010-001-100	010-001-100	100-010-001	001-100-010
V43	010-001-100	010-001-100	100-010-001	010-001-100
V44	010-001-100	010-001-100	100-010-001	100-010-001
V45	010-001-100	100-010-001	001-100-010	001-100-010
V46	010-001-100	100-010-001	001-100-010	010-001-100
V47	010-001-100	100-010-001	001-100-010	100-010-001
V48	010-001-100	100-010-001	010-001-100	001-100-010
V49	010-001-100	100-010-001	010-001-100	010-001-100
V50	010-001-100	100-010-001	010-001-100	100-010-001
V51	010-001-100	100-010-001	100-010-001	001-100-010
V52	010-001-100	100-010-001	100-010-001	010-001-100
V53	010-001-100	100-010-001	100-010-001	100-010-001
V54	100-010-001	001-100-010	001-100-010	001-100-010
V55	100-010-001	001-100-010	001-100-010	010-001-100
V56	100-010-001	001-100-010	001-100-010	100-010-001
V57	100-010-001	001-100-010	010-001-100	001-100-010
V58	100-010-001	001-100-010	010-001-100	010-001-100
V59	100-010-001	001-100-010	010-001-100	100-010-001
V60	100-010-001	001-100-010	100-010-001	001-100-010
V61	100-010-001	001-100-010	100-010-001	010-001-100
V62	100-010-001	001-100-010	100-010-001	100-010-001
V63	100-010-001	010-001-100	001-100-010	001-100-010
V64	100-010-001	010-001-100	001-100-010	010-001-100
V65	100-010-001	010-001-100	001-100-010	100-010-001
V66	100-010-001	010-001-100	010-001-100	001-100-010
V67	100-010-001	010-001-100	010-001-100	010-001-100
V68	100-010-001	010-001-100	010-001-100	100-010-001
V69	100-010-001	010-001-100	100-010-001	001-100-010
V70	100-010-001	010-001-100	100-010-001	010-001-100
V71	100-010-001	010-001-100	100-010-001	100-010-001
V72	100-010-001	100-010-001	001-100-010	001-100-010
V73	100-010-001	100-010-001	001-100-010	010-001-100
V74	100-010-001	100-010-001	001-100-010	100-010-001
V75	100-010-001	100-010-001	010-001-100	001-100-010
V76	100-010-001	100-010-001	010-001-100	010-001-100
V77	100-010-001	100-010-001	010-001-100	100-010-001
V78	100-010-001	100-010-001	100-010-001	001-100-010
V79	100-010-001	100-010-001	100-010-001	010-001-100
V80	100-010-001	100-010-001	100-010-001	100-010-001

Table A2. The $\mathbf{S}_{MC_p}$ Switch States.

	$s_{A1} \ldots s_{C3}$	$s_{A4} \ldots s_{C6}$	$s_{A7} \ldots s_{C9}$	$s_{A10} \ldots s_{C12}$
V0	001-010-100	001-010-100	001-010-100	001-010-100
V1	001-010-100	001-010-100	001-010-100	010-100-001
V2	001-010-100	001-010-100	001-010-100	100-001-010
V3	001-010-100	001-010-100	010-100-001	001-010-100
V4	001-010-100	001-010-100	010-100-001	010-100-001
V5	001-010-100	001-010-100	010-100-001	100-001-010
V6	001-010-100	001-010-100	100-001-010	001-010-100
V7	001-010-100	001-010-100	100-001-010	010-100-001
V8	001-010-100	001-010-100	100-001-010	100-001-010
V9	001-010-100	010-100-001	001-010-100	001-010-100
V10	001-010-100	010-100-001	001-010-100	010-100-001
V11	001-010-100	010-100-001	001-010-100	100-001-010
V12	001-010-100	010-100-001	010-100-001	001-010-100
V13	001-010-100	010-100-001	010-100-001	010-100-001
V14	001-010-100	010-100-001	010-100-001	100-001-010
V15	001-010-100	010-100-001	100-001-010	001-010-100
V16	001-010-100	010-100-001	100-001-010	010-100-001
V17	001-010-100	010-100-001	100-001-010	100-001-010
V18	001-010-100	100-001-010	001-010-100	001-010-100
V19	001-010-100	100-001-010	001-010-100	010-100-001
V20	001-010-100	100-001-010	001-010-100	100-001-010
V21	001-010-100	100-001-010	010-100-001	001-010-100
V22	001-010-100	100-001-010	010-100-001	010-100-001
V23	001-010-100	100-001-010	010-100-001	100-001-010
V24	001-010-100	100-001-010	100-001-010	001-010-100
V25	001-010-100	100-001-010	100-001-010	010-100-001
V26	001-010-100	100-001-010	100-001-010	100-001-010
V27	010-100-001	001-010-100	001-010-100	001-010-100
V28	010-100-001	001-010-100	001-010-100	010-100-001
V29	010-100-001	001-010-100	001-010-100	100-001-010
V30	010-100-001	001-010-100	010-100-001	001-010-100
V31	010-100-001	001-010-100	010-100-001	010-100-001
V32	010-100-001	001-010-100	010-100-001	100-001-010
V33	010-100-001	001-010-100	100-001-010	001-010-100
V34	010-100-001	001-010-100	100-001-010	010-100-001
V35	010-100-001	001-010-100	100-001-010	100-001-010
V36	010-100-001	010-100-001	001-010-100	001-010-100
V37	010-100-001	010-100-001	001-010-100	010-100-001
V38	010-100-001	010-100-001	001-010-100	100-001-010
V39	010-100-001	010-100-001	010-100-001	001-010-100
V40	010-100-001	010-100-001	010-100-001	010-100-001
V41	010-100-001	010-100-001	010-100-001	100-001-010
V42	010-100-001	010-100-001	100-001-010	001-010-100
V43	010-100-001	010-100-001	100-001-010	010-100-001
V44	010-100-001	010-100-001	100-001-010	100-001-010
V45	010-100-001	100-001-010	001-010-100	001-010-100
V46	010-100-001	100-001-010	001-010-100	010-100-001
V47	010-100-001	100-001-010	001-010-100	100-001-010
V48	010-100-001	100-001-010	010-100-001	001-010-100
V49	010-100-001	100-001-010	010-100-001	010-100-001
V50	010-100-001	100-001-010	010-100-001	100-001-010

Table A2. *Cont.*

	$S_{A1} \ldots S_{C3}$	$S_{A4} \ldots S_{C6}$	$S_{A7} \ldots S_{C9}$	$S_{A10} \ldots S_{C12}$
V51	010-100-001	100-001-010	100-001-010	001-010-100
V52	010-100-001	100-001-010	100-001-010	010-100-001
V53	010-100-001	100-001-010	100-001-010	100-001-010
V54	100-001-010	001-010-100	001-010-100	001-010-100
V55	100-001-010	001-010-100	001-010-100	010-100-001
V56	100-001-010	001-010-100	001-010-100	100-001-010
V57	100-001-010	001-010-100	010-100-001	001-010-100
V58	100-001-010	001-010-100	010-100-001	010-100-001
V59	100-001-010	001-010-100	010-100-001	100-001-010
V60	100-001-010	001-010-100	100-001-010	001-010-100
V61	100-001-010	001-010-100	100-001-010	010-100-001
V62	100-001-010	001-010-100	100-001-010	100-001-010
V63	100-001-010	010-100-001	001-010-100	001-010-100
V64	100-001-010	010-100-001	001-010-100	010-100-001
V65	100-001-010	010-100-001	001-010-100	100-001-010
V66	100-001-010	010-100-001	010-100-001	001-010-100
V67	100-001-010	010-100-001	010-100-001	010-100-001
V68	100-001-010	010-100-001	010-100-001	100-001-010
V69	100-001-010	010-100-001	100-001-010	001-010-100
V70	100-001-010	010-100-001	100-001-010	010-100-001
V71	100-001-010	010-100-001	100-001-010	100-001-010
V72	100-001-010	100-001-010	001-010-100	001-010-100
V73	100-001-010	100-001-010	001-010-100	010-100-001
V74	100-001-010	100-001-010	001-010-100	100-001-010
V75	100-001-010	100-001-010	010-100-001	001-010-100
V76	100-001-010	100-001-010	010-100-001	010-100-001
V77	100-001-010	100-001-010	010-100-001	100-001-010
V78	100-001-010	100-001-010	100-001-010	001-010-100
V79	100-001-010	100-001-010	100-001-010	010-100-001
V80	100-001-010	100-001-010	100-001-010	100-001-010

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Unidirectional DC/DC Converter with Voltage Inverter for Fast Charging of Electric Vehicle Batteries

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Abstract: The paper proposes the adaptation of the industrial plant's power network to supply electric vehicle (EV) fast-charging converters (above 300 kW) using renewable energy sources (RESs). A 600 V DC microgrid was used to supply energy from RESs for the needs of variable speed motor drives and charging of EV batteries. It has been shown that it is possible to support the supply of drive voltage frequency converters (VFCs) and charging of EV batteries converters with renewable energy from a 600 V DC microgrid, which improves the power quality indicators in the power system. The possibility of implementing the fast EV batteries charging station to the industrial plant's power system in such a way that the system energy demand is not increased has also been shown. The EV battery charging station using the drive converter has been presented, as well as the results of simulation and laboratory tests of the proposed solution.

Keywords: EV battery; electric vehicles; fast battery charging; local transport; DC micro grid; drive voltage frequency converter; big power DC/DC converter

1. Introduction

The fast development of industrial power electronics gives the opportunity to replace traditional solutions not only in electric drives, but also contributes to the construction of scalable high-power modular charging stations for electric vehicles, e.g., 300 kW. The authors propose the use of low-voltage frequency converter modules, that are commonly used in electric drives, in fast-charging stations. This approach will significantly facilitate the construction of a fast vehicle charging station and should significantly reduce the cost of their manufacture.

The literature review shows that there are different methods and topologies for electric vehicle (EV) battery charging. In [1], the authors present simulation models of selected topologies of EV fast-charging systems and their research, where particularly interesting are the converter topologies with regulated rectified voltage using a thyristor half-bridge three-phase rectifier. This solution does not use galvanic separation between the charged battery and the converter. Other models shown use a single-phase inverter and a high-frequency isolation transformer. In [2], the authors focus on reviewing all the useful data available on EV configurations, battery energy sources, electrical machines, charging and optimization techniques, impacts, trends, and possible directions of future developments. In [3] various charging station topologies compared and evaluated based on microgrid support, power density, modularity and other factors. The authors use full-bridge single-phase

inverters to supply the individual phases of a three-phase high-frequency transformer that separates the output power stages of the DC/DC converter. In [4], mainly on-board converters for charging EV batteries powered from single- and three-phase grids are presented. Various power level chargers and infrastructure configurations are presented, compared, and evaluated based on amount of power, charging time and location, cost, equipment, and other factors. The paper [5] shows power electronics converters for EV fast charging stations, where a three-branch DC/DC converter is used that uses a half-bridge inverter structure to produce DC charging for EV batteries. The properties of the DC/DC converter model from [5] were described by the authors of this paper on the basis of simulation tests carried out.

The most popular charging method is constant current charging of EV battery to about 80% of its capacity [6,7]. Whereas the reference [8] shows off-board EV fast battery charger based on a dual-stage power converter (AC/DC and DC/DC) sharing the same DC link. Publications presenting the possibility of application of three-phase half-bridge voltage inverters as components for DC/DC converters in the EV charging stations are rarely seen. In particular, these three-phase Pulse Width Modulation (PWM) inverters are used in the induction motor drives [9]. The majority part of literature on the subject describes solutions with single-phase full-bridge PWM inverters [1,10]. Converters for charging EV batteries mainly use single-phase inverters. Three-phase converters are required for high charging powers. The proposals from the literature do not use the three-phase voltage frequency drives voltage frequency converters (VFCs) to obtain the charging voltage of an EV battery.

Particularly, paper [11] presents a comparison of a current-source converter and a voltage-source converter (VSC) for three-phase EV fast battery chargers, where it is possible to control the output voltage of VSCs in a wide range of values but no more than 560 V, which is the maximum instantaneous value of the phase-to-phase voltage.

An important aspect is that the power supply of the EV fast-charging station should come from renewable energy sources (RESs). The concept of powering from RES dedicated for EV fast-charging station is described in [12]. The use of an AC/DC converter to supply a three-phase diode rectifier, generating the charging voltage of an EV battery is presented. The elimination of distorted currents in three-phase networks was achieved by means of a resonant LC filter. The PWM inverter is connected to the rectifier via the differential-mode voltage filter, which additionally allows the voltage regulation on the rectifier. In [13] the methods of supporting DC power supply to drive converters from a PV source is presented. This solution reduces the harmonics of the current in the three-phase AC network. The main idea in [14] is to reduce the number of DC/DC converters in an off-board DC/AC charging station powered from a PV source. The vehicles are equipped with on-board AC/DC converters. The [15] presents calculations of the demand for renewable energy for the needs of EV battery charging, taking into account energy storages.

The combination of many different sources enables more efficient use of the production capacities of systems using RES, increases the reliability and quality of power supplied to consumers and ensures independence from the supply. This integration of different energy sources is ensured by a microgrid. The paper [16] presents the basic assumptions of the idea of connecting various generation units of distributed generation cooperating within the so-called "microgrids" on the example of DC microgrid, properties of renewable energy sources and economic aspects of energy production in the DC microgrid. The use of DC microgrids in the EV battery charging stations is described in detail in [17], as well as battery manufacturing technologies and charging strategies. In [18], the possibility of using a hybrid DC/AC microgrid to power an EV charging station is demonstrated.

It is also important to limit the harmonic content of low orders in the phase current caused by rectifiers located in EV chargers. In [19] the authors analyse the operating principle of charging current in a continuous and discontinuous mode in case of EV charger with three-phase uncontrolled rectifier with a passive method of power factor correction (current total harmonic distortion—THD). The use of a 12-pulse rectifier [20,21] or resonant filters [12] is justified by the low cost and significant reduction of current harmonics for demanding industry applications, typical above 250 kW.

The rest of the introduction contains two main sections. Section 1.1 presents a model of an exemplary Li-ion battery pack for an EVs and its basic parameters: nominal voltage, charging voltage, internal resistance. A proprietary method of determining the equivalent resistance of a cell and the entire set of batteries was proposed. The aim of the paper is to demonstrate the possibility of adapting high-power drive converters to generate a constant voltage with an adjustable value for fast-charging with a constant current of an EV battery set. Section 1.2 presents the described in the literature and already implemented for production of direct voltage–direct current (DC/DC) converters using the half-bridge structure of a three-phase inverter to generate direct current charging an EV battery pack by using appropriate PWM control and branch output chokes of the converter. The authors presented their own models for simulation tests of such converters to show the differences between PWM control of DC/DC converters and PWM control of a drive inverter (DC/AC converter).

Further parts present the possibilities of using DC microgrid with hybrid power supply using RES to supply clean energy, both for drive converters operating as converters to supply AC motors or as converters for charging EV batteries (e.g., internal transport). Simulation tests of a high-power converter model adapted for charging a battery set with DC current were carried out. The main circuit diagrams and the control of the converter models are given precisely to enable the reader to verify the obtained results and to further develop the presented research. The final section of the paper presents the results of laboratory tests in which an industrial low-power drive converter with a rectifier unit was used, where the energy supplied from the rectifier was lost on the power resistor. The aim of this study was to demonstrate that, according to simulation studies, it is possible to automatically maintain a constant current at a given value, regardless of the value of the load resistance. The industrial drive converter automatically adjusted the AC voltage of the inverter to the set rectifier load current value. The applied rectifier load power resistor with a given value replaced the EV battery set. The obtained experimental results confirm the possibility of using high power drive converters for fast-charging of EV batteries. Finally, in the Discussion section, the comparison of sinusoidal and triangular modulation was presented and the use of triangular modulation in the PWM inverter to EV battery charging was proposed for further research.

1.1. Charging of High Capacity, High Power Batteries

For the Li-ion type LFP100AHA battery cell [22] with the following parameters: V_{bn} = 3.2 V (from 20% to 100% State Of Charge—SOC) and Q_{no} = 100 Ah, it is possible to build a battery pack by connecting cells in series to determine the voltage of battery set and in parallel to increase the capacity of set.

With a series connection of 100 cells, a set of 100 cells multiplied by 3.2 V is obtained, giving the nominal voltage of the battery set equal to V_{zbn} = 320 V and a capacity Q_{zbn1} = 100 Ah. By connecting eight chains of 100 cells in parallel (100cx8ch), the final battery set 100cx8ch with the parameters 800 Ah/320 V is obtained, which corresponds to the capacity of 256 kWh. An equivalent diagram of an EV battery with a voltage DC/DC charging converter is shown in Figure 1.

According to Figure 1, it was assumed that a DC/DC converter with a minimum power of approx. $P_{(1C)}$ = 276 kW should be used to charge the battery set in 1 h with 1 C current or with a power of nearly 828 kW to charge the battery in about 20 min. with 3 C current. C rate is derived from Coulomb's Law. The value of the charging current resulting from the battery capacity specified in Ah, e.g., 100 Ah means 1 C = 100 A. The possibility to charge an EV battery with 3 C current depends on its cooling capability, as the losses during charging increase three times compared to 1 C current. For 1 C current is $P_s = R_{zb} \cdot I_{zb}^2 = 12.5\ \mathrm{m\Omega} \cdot (800\ \mathrm{A})^2 = 8$ kW and for 3 C current is 3×8 kW = 24 kW. During continuous operation and while charging the battery, its temperature may not exceed 65 °C [22]. For customer is better, when the charging this battery current is 3 C (2400 A). The EV battery in this case will be charge in 20 min, but it is associated with a shorter battery life.

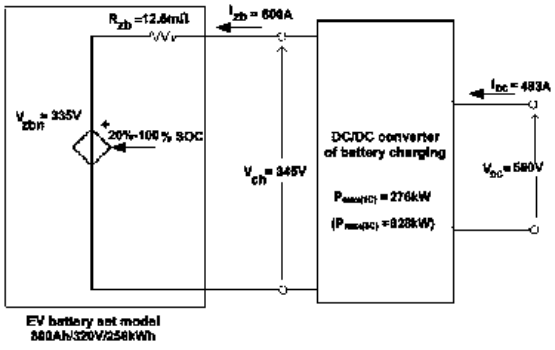


Figure 1. Model of 100cx8ch battery set made of Li-ion cells LPF100AHA-800 Ah/320 V/256 kWh with direct voltage–direct current (DC/DC) converter powered from 600 V DC microgrid [23,24].

Different strategies are used to charge EV batteries, e.g., Constant Current (CC) 3 C (20–80% SOC) and Constant Voltage (CV) 80–100% SOC or charging with 10 C current pulse (20–80% SOC). A compromise should be found between charging time and battery temperature.

The equivalent internal resistance R_{zb} of the battery pack intended to estimate charging power loses, can be determined based on the equivalent resistance of a single cell R_b. Several methods for determining R_b are known [25]. The authors of this paper propose a method based on reading the cell charging voltage value at 1 C ($U_{ch(1C)}$ = 3.45 V) and 3C ($U_{ch(3C)}$ = 3.65 V) charging currents, which is given in the catalogue card [26,27]. Charging voltages for the Li-ion cells of the LFP100AHA type are linearly approximated and presented in Figure 2. To the further simulation studies, an equivalent resistance was used, which reflects the power given to the battery by the converter.

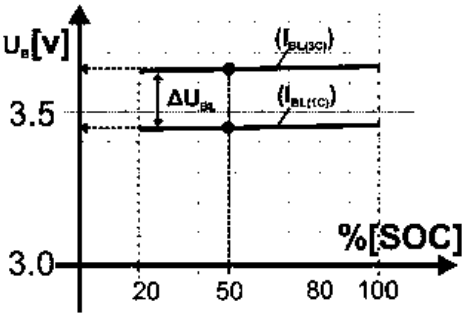


Figure 2. Linear approximated Li-ion cell voltages of the LFP100AHA type for the 20–100% State of Charge (SOC) range when charged at 1C and 3C [22].

Based on the reading of voltages for 50% SOC from Figure 2, the equivalent internal resistance R_b of the single cell can be calculated (1) as follows:

$$R_b = \frac{\triangle U_b}{\triangle I_b} = \frac{U_{b(3C)(50\%SOC)} - U_{b(1C)(50\%SOC)}}{I_{b(3C)(50\%SOC)} - I_{b(1C)(50\%SOC)}} = \frac{0.2V}{200A} = 1\ \mathrm{m\Omega} \quad (1)$$

where:

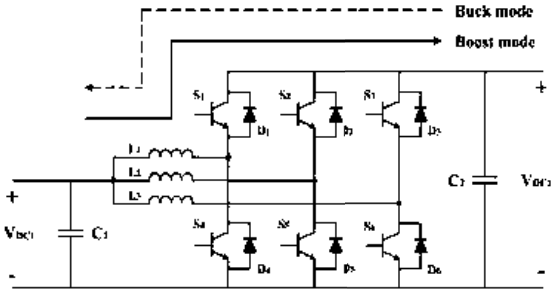
R_b—equivalent resistance of a single cell,
$\triangle U_b$—difference of cell voltages for 3 C and 1 C charging currents,
$\triangle I_b$—difference of cell charging currents 3 C (300 A) and 1C (100 A), respectively.

Then the equivalent resistance R_{zb} of the 100c8ch battery set is equal to:

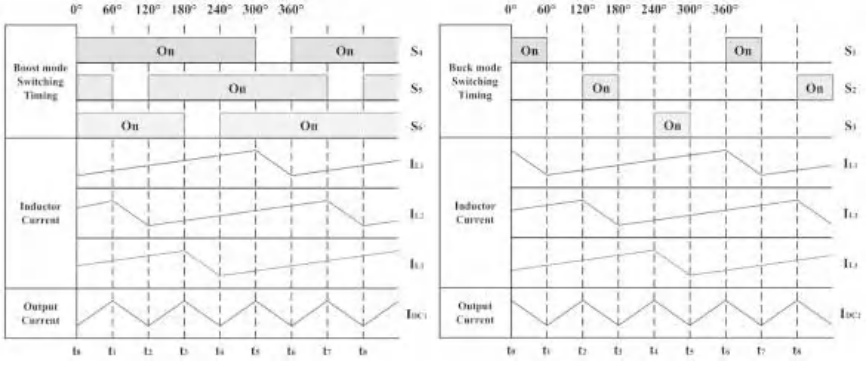
$$R_{zb} = \frac{R_b \cdot 100\ cells}{8\ chains} = 12.5\ \text{m}\Omega \tag{2}$$

1.2. Bidirectional DC/DC Converter

DC output power supplies, such as energy storages, uses a bidirectional DC/DC converter for direct connection to DC microgrid. The type of DC/DC converter, shown in Figure 3a, allows the converter current to be split into 3 branches, which are controlled with an 120° interleave method [28]. Figure 3b,c show switching states and waveforms of currents in operating states of boost and buck mode, respectively.



(**a**)



(**b**) (**c**)

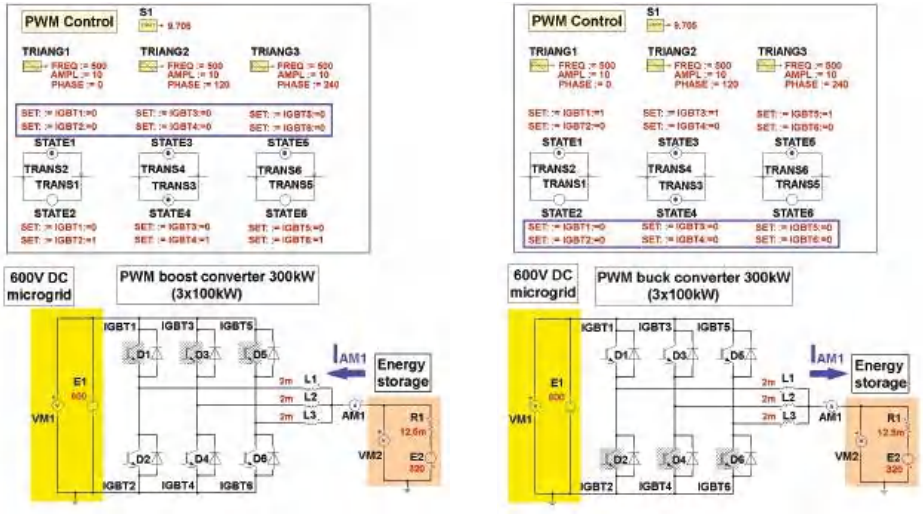
Figure 3. Three branches half-bridge bidirectional DC/DC converter: (**a**) diagram of the converter, (**b**) switching states and currents in boost mode, (**c**) switching states and currents in buck mode [28].

Bidirectional DC/DC converters can be basically divided into isolated [29,30] and non-isolated types. In general, an insulated bidirectional DC/DC converter has the advantage of easily controlling voltage step-up and step-down through a transformer inside the converter, but the transformer used in the insulated type has a large volume. It has a disadvantage that the size and weight of the transformer are increasing with the power of the converter. On the other hand, the non-isolated bidirectional DC/DC converter has the advantage of being relatively simple in structure, has high efficiency, and reduced weight in comparison to the insulated type [31]. In the non-isolated bidirectional DC/DC converter structure, various methods have been proposed to aim for higher efficiency, but among them, the interleaved method reduces the current stress of the power element because the magnitude of

the load current (battery storage, DC microgrid) is divided into multiple phases. It has a feature of reducing the power device size and its current rating [29,32].

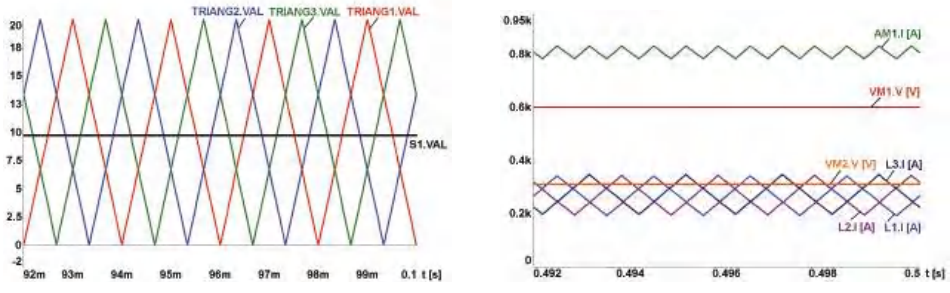
Tests of the battery (energy storage) charging current from the DC voltage line as a function of the converter control factor D (S1) are shown in Figure 4a,b. They present the models of boost type and buck type of DC/DC converter respectively, which are simulated in ANSYS Simplorer. The inverter of each one is controlled by means of a state graph. Triangular modulation is based on the analysis of waveforms controlling IGBT power transistors and is implemented for each phase separately (TRIANG1 to TRIANG3). A constant value S1 representing the control factor D is given. It is presented on Figure 5a.

Whereas, Figure 5b presents phase currents L1, L2, L3 and voltage waveforms at selected points of the models from Figure 4a. The DC/DC boost converter supplies energy to the 600 V DC voltage line (E1 source-VM1 voltmeter) from an energy storage with an initial voltage of 320 V (E2 source-VM2 voltmeter). To ensure constant charging current AM1 at different values of its voltage, the converter's control factor D should be changed accordingly. The operation of a buck converter is analogous (model from Figure 4b).



(**a**) (**b**)

Figure 4. Model of DC/DC converter: (**a**) boost type—energy is transferred from energy storage to DC microgrid, (**b**) buck type—energy is transferred from DC microgrid to energy storage.



(**a**) (**b**)

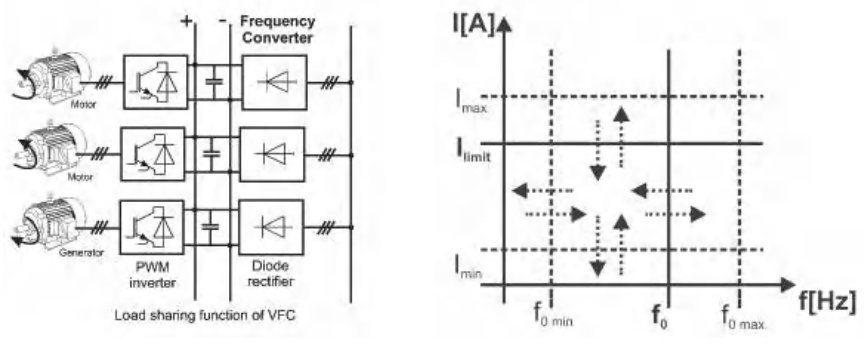
Figure 5. Waveforms in the boost mode (model from Figure 4a): (**a**) control, (**b**) currents and voltages.

The authors proposed an alternative solution. In the same power electronic structure as the bidirectional DC/DC converter, it was produced AC voltage instead of DC voltage, because the different control of converter is used. The unidirectional converter used in regulated industrial drives to control the speed and torque of induction motors was investigated. The maximum voltage of the EV battery charging converter constructed in this way is determined by the value of the DC link voltage.

2. Drive Voltage Frequency Converters Used in the EV Charging Stations

In a typical "load sharing" drive application, each VFC normally supplies power to a motor via the AC supply line. If one or more motors are driven in regenerative mode, they deliver power to the common DC bus. Then this power is used by other VFC and in this way the installation is more efficient, because in many situations the brake resistors can be omitted. In this situation the DC voltage (intermediate voltage) can be slightly different in each converter. This is due to minor differences in the rectifiers, different temperature, output power, etc. This small difference in DC voltage makes it necessary to use small line reactors in the AC main supply and fuses in the DC bus. The load sharing DC grid, which connect a few intermediate circuits of VFC, is presented in Figure 6a [33]. A large number of VFCs located in the various places of the local grid enables the location of EV battery charging points as close as possible to places of using the autonomous electric work machines and various types of EVs. Currently, all drives in which the engine speed is controlled, use indirect AC/DC/AC converters.

The I_{limit} battery charging current can be set between the minimum current I_{min} and the maximum current I_{max} of the inverter, Figure 6b. For the maximum frequency of sinusoidal voltage f_0, the condition is $f_c/f_0 = 10$ [21]. Increasing the frequency of the sinusoidal waveform f_0 to a value above 50 Hz ensures a reduction of the alternating component in the rectified DC.

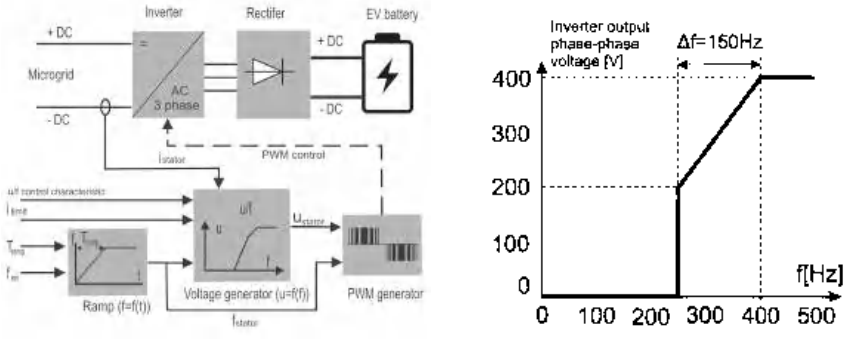


(**a**) (**b**)

Figure 6. Functions of drive voltage frequency converter (VFC): (**a**) load sharing in drive VFCs, (**b**) current limiter [21,33].

An example of basic drive VFC with scalar control, which is adapted to DC/DC converter, is shown in Figure 7a. The CC battery charging strategy can use the inverter output current limitation function. The control systems of these converters can ensure any voltage characteristic as a function of frequency, typically u/f^2 = const., or u/f = const. It enables to realise a special characteristic like the one shown in Figure 7b, which is used for battery charging. This shape of u/f characteristic limits the frequency changing when the current limiter is active, Figure 6b. The arrows indicate the possibility of setting any frequency and limit current values in the drive FC. When EV charger achieves the charging current I_{min}, it means that the battery is fully charged. The sinusoidal frequency of the inverter output voltage f_0 is limited by the carrier frequency f_c of PWM. Frequency changes of 150 Hz causes the voltage to change between 250 V and 400 V. It is possible to choose a battery charging characteristic

from four variable sets of VFC parameters, Figure 7a [21].



(**a**) (**b**)

Figure 7. Drive VFC implemented as an electric vehicle (EV) fast charger: (**a**) control of industrial Pulse Width Modulation (PWM) drive converter with output rectifier, (**b**) special characteristic of inverter phase-phase voltage.

Frequently the control of a complex voltage vector in the drive VFC is used in the recuperative DC/AC converter that transfers energy from a DC microgrid to a three-phase AC grid. Drive VFC commonly uses the inverter current limiting function to protect motors against overload. This function can be used to set charging current of an EV battery.

3. DC Microgrid

By connecting all DC links of the sources and loads, a DC microgrid is formed, Figure 8. The DC microgrid does not directly connect to the prevalent three-phase AC utility grid, like the AC microgrid, but via a bidirectional DC/AC converter for common integration. The use of this type of solution gives wide possibilities of cooperation of various generating units, such as RES. Functional microgrids focused on EV battery charging can become a basic element of charging infrastructure. The possibility of eliminating many stages of AC/DC and DC/AC conversion, could significantly reduce the cost of network components and power losses, and additionally increase the reliability of network systems. Moreover, the lack of reactive power, absence of harmonics and asymmetry of voltages and currents in the DC system, make the DC microgrid one of the key areas of application that contribute to significant benefits [16,17].

The own concept of hardware integration of the EV fast-charging station with the local LV DC microgrid (3) and the MV industrial power system (4) supplying the drive VFC (14) of the squirrel-cage induction motor (16) is presented in Figure 8. The local DC microgrid is powered from three sources: renewable energy (solar or wind) (1), energy storage (e.g., Li-ion battery) (9) and MV power system (4) via LV grid (5). The hybrid DC power supply is optional, however, the extension of the power supply system with additional RES provides "clean energy" to the production process and relieves the power system. Reducing the so-called carbon footprint in products is now a mandatory requirement due to the increased effort to protect the environment. The EV battery is attached to the output rectifier (11). Implementation of the battery charging strategy, e.g., CC charging in the range of 20–80% SOC is controlled by a PLC controller (17), which for this purpose communicates with the inverter (12) of drive VFC (14).

A parallel resonant filter (15) is connected to the power supply of the drive VFC, which reduces the harmonic current of the input rectifier (13). To limit the effect of capacitive reactive power of the filter, it is switched on, if the VFC load exceeds the set value, e.g., when the drive VFC (14) load current exceeds 50% of the nominal current. The ES (9) accumulates excess energy generated by RES and maintains power supply for devices connected to the local DC microgrid during interruptions in the

supply of energy from other sources. The ES is coupled to the DC microgrid via a bidirectional DC/DC converter (8). The task of this converter is to ensure charging of the ES according to the set strategy or supplying energy to the DC microgrid in accordance with the algorithm implemented in the PLC software (17).

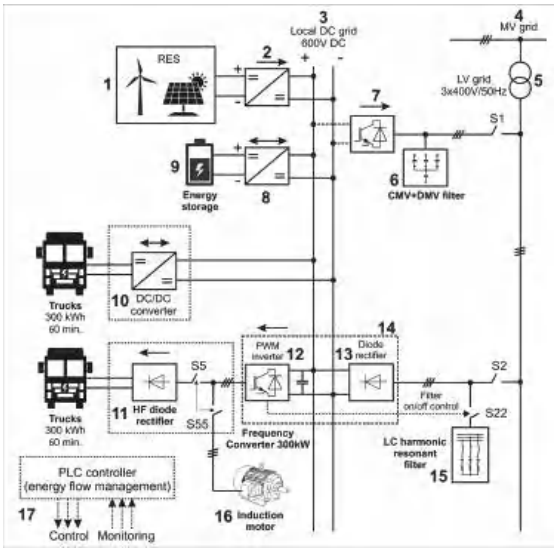


Figure 8. Hybrid 600 V DC microgrid for EV fast charging.

The local RES power plant (1) supplies DC voltage to the microgrid (3) via a unidirectional DC/DC converter (2). The task of this converter is to supply renewable energy to the DC grid and minimize the energy consumed from the power system (4). During a significant deterioration of power quality indicators in the power system or the occurrence of surplus renewable energy, it can be sent to the system via a DC/AC inverter (7), which cooperates with the LCL filter group (6) to limit the content of high-frequency differential-mode (DM) and common-mode (CM) voltage produced by the PWM Active Front End (AFE) recuperative inverter (7) [34,35].

The authors carried out research showing the possibility of using drive VFC as inverter components for fast charging of EV batteries, which is depicted in Figure 9.

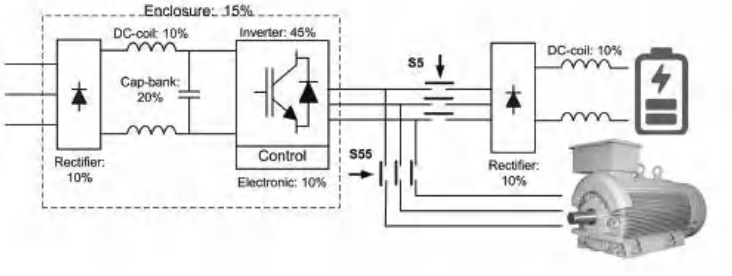


Figure 9. Use of drive VFC to charging EV batteries.

The mathematical model of the bipolar PWM inverter of the drive VFC connected with a six-pulse diode rectifier is presented in Figure 10. The model is written with electric symbols representing ideal energy sources, ideal passive elements and linearized models of controlled and non-controlled power electronics. The electrical differential equations of the DC/AC/DC converter are solved

using an ANSYS Simplorer. The obtained results of simulation tests of the presented model confirm the possibility of controlling the direct voltage value of the diode rectifier charging the EV battery. Experimental tests carried out on the laboratory stand confirmed the results of simulation tests. The battery constant voltage obtained here is characterized by stability and negligible ripple. A detailed description of the operation of the EV battery charging rectifier and the PWM inverter is not the subject of this study.

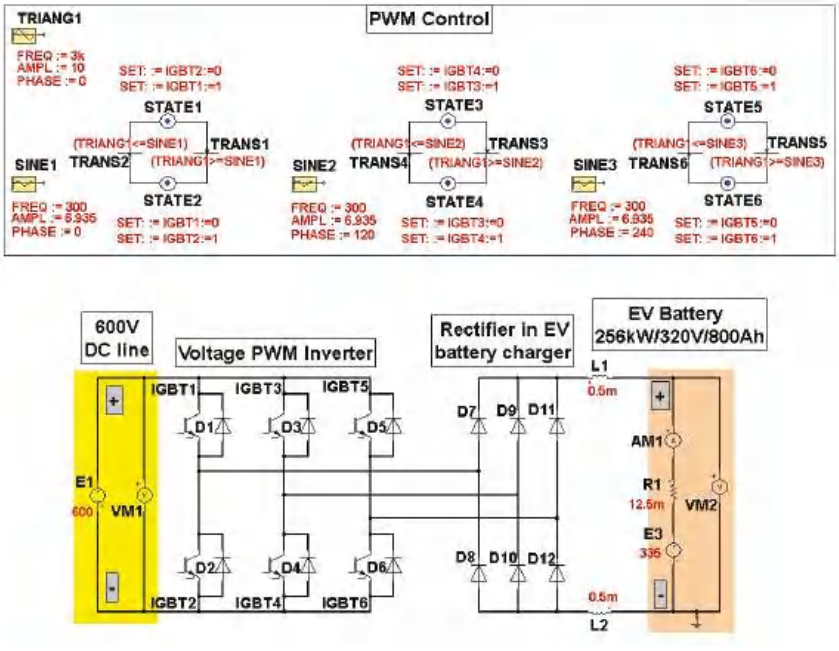


Figure 10. DC/AC/DC converter model with a two-level PWM voltage inverter and a six-pulse diode rectifier.

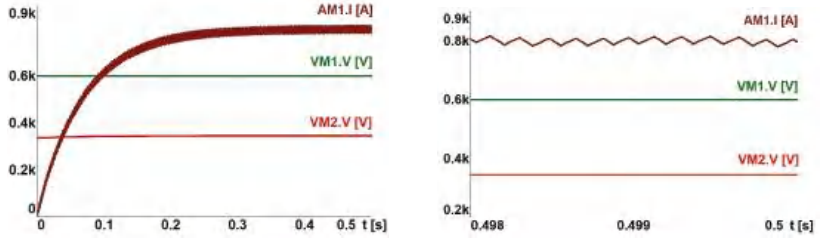
Drive VFCs with two-level voltage inverters are usually available with a six-pulse diode rectifier or less often with an AFE rectifier [21]. The basic types of drive converters used in LV grid are shown in Figure 9. The digital designations of the VFC components in Figure 9 refer to the hardware configuration of the hybrid EV fast-charging station shown in Figure 8. Proposed hardware combination of a hybrid EV charging station power supply system contains a significant part of the components used in industrial drive systems.

4. Simulation and Experimental Tests of Novel EV Charger

The electrical diagram of the simulation linear circuit model of a three-phase EV charger is depicted in the Figure 10. The EV battery is represented with a resistor R1 and voltage source E3. Using different values of sinusoids frequency and its amplitude in the inverter PWM control (SINE1, SINE2 and SINE3 PWM control-Figure 10), it was possible to test the EV charger properties for different values of the modulation factor M and the frequency of modulating voltages. The frequency of the triangular carrier waveform of PWM modulation was set in the TRIANG1 module and f_c = 3 kHz was used. It is a typical carrier frequency for inverters in the industrial high power drives. The frequency of SINE modules is 300 Hz, and it was the maximum output sinusoidal frequency of industry drive FC used in the laboratory stand. The modulation factor M can be changed between 0 and 1.25 to control output inverter voltage.

The use of the PWM modulator model described by the state graph made it easy to control the inverter IGBT transistors in relation to the sinusoidal PWM pattern. It was assumed that all model elements used in electrical circuits had linearized parameters.

To receive the constant charging current 800 A, the control of the modulation factor value M was used. Figure 11a,b show the obtained results of current and voltage waveforms, which are depended on the modulation factor's value (according to the model from Figure 10, M = 0.6935). The EV battery charging current 1 C was used in the test. The value of the charging current results from the technical specification of tested the Li-ion battery [22]. In the case of continuous modulation (the maximum value of modulation factor is M = 1), the EV battery voltage increased and the current exceeded the permissible charging value, which could destroy the EV battery. Therefore, it is important to choose the appropriate value of the modulation factor M, which allows battery charging with constant current for nominal pack voltages at the level to about 500 V [36].



(**a**) (**b**)

Figure 11. Constant-current battery charging measured in the time interval up to (**a**) 0.5 s, (**b**) 2 ms.

The tests of a diode rectifier powered by an inverter were performed under the following conditions:

1. without chokes of LC filters (3, 4) downstream of the inverter and in the rectifier,
2. with two types of LC filters of inverter DM voltage (3, 4),
3. without DM filter, but with DC chocks in the rectifier.

In case 1, it was not possible to adjust the value of the rectified voltage. In case 2, the impedance of the LC filter chokes caused an unfavourable significant drop in the rectifier supply voltage. Case 3 made it possible to control the rectified voltage in a wide range. Moreover, the elimination of the capacitors on the DC side of the rectifier did not significantly increase the AC component in the rectified voltage.

The specification of laboratory stand depicted in Figure 12a is presented in Table 1.

Table 1. Specification of the laboratory stand from Figure 12a.

No.	Name of Component	Parameters
1	Frequency converter VLT 3004	2.2 kW, 3 × 400 V/50 Hz, I_N = 5 A
2	RFI filter	I_N = 16 A
3	LC filter 1	16 A, 3 × L = 4 mH, 3 × C = 3 µF-Y
4	LC filter 2	16 A, 3 × L = 4 mH, 3 × C = 2 µF-△
5	Capacitors battery for CM voltage suppression	3 × C2 = 1 µF (connected to supply AC phases)
6	Drive frequency converter 5.5 kW	5.5 kW, 3 × 400 V/50 Hz, I_N = 12 A
7	Load resistors for drives VFC in rows 2 and 6	3 × (100 Ω–500 Ω)
8	Passive current harmonic filter for drives VFC (rows 2 and 6)	3 × 400 V/50 Hz, I_N = 10 A

When the negative pole of the load (EV battery) is grounded, the CM voltage is absent in the rectified voltage. Therefore, there is no need to filter the inverter CM voltage by using the capacitors (No. 5, Table 1) attached to the DM filter from one side and AC phase voltages from the second side.

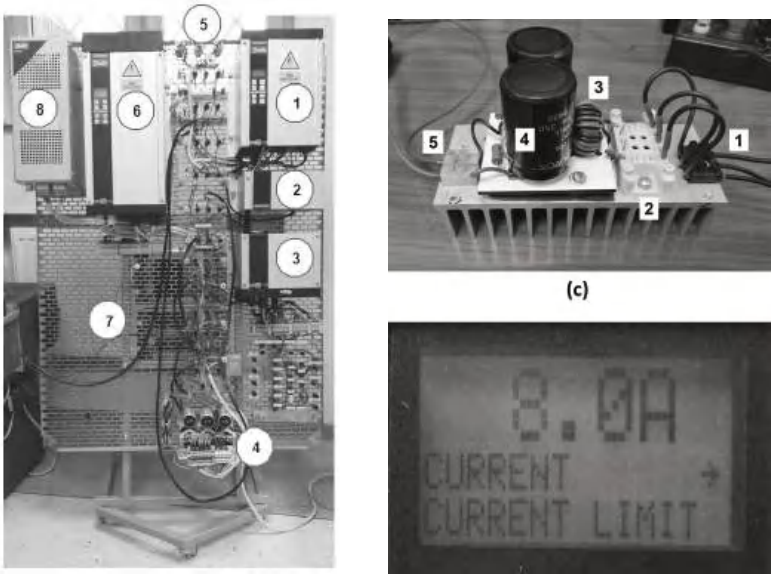
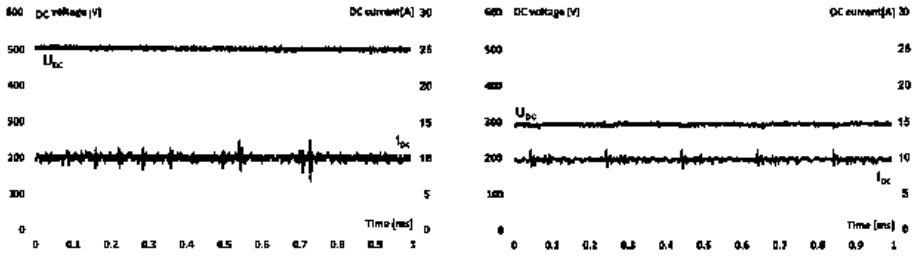


Figure 12. Laboratory stand: (**a**) equipped with two drive VFCs with built-in rectifying units attached to PWM inverters - the detailed specification is in Table 1, (**b**) with three-phase rectifier unit I_n = 15 A built into the drive VFC, (**c**) programmed value of the maximum output current in 5.5 kW drive VFC.

Given by the VFC drive current limitation, the rectifier load current maintained a constant value thanks to automatically lowering the rectifier supply voltage by the inverter control system. Figure 12b shows the programmed value of the maximum output current 8 A of low voltage (3 × 400 V/50 Hz) and small power (5.5 kW) industrial VFC drive (No. 6, Table 1). The maximum value of the rectified current did not exceed 10 A, which resulted from the power balance ($P_{AC} = P_{DC}$).

Figure 12c shows the six-pulse diode rectifier built for drive VFCs of the laboratory stand. Drive VFC outputs (1) were connected to a fast six-diode rectifier (2) with ferrite anti-distortion filter (3) and capacitor bank on the constant voltage side (4) of the rectifier, thus it was possible to charge EV batteries with DC current (5). The DC voltage fluctuations did not depend substantially from the value of the capacitor bank, because the inverter frequency of fundamental voltage harmonic was set to 300 Hz.

The received output DC voltages and DC currents are presented in Figure 13, for the capacitor bank equal to C = 16 μF. By comparing Figure 13a,b, the effective operation of the EV battery charging current stabilizer was visible. The rectifier voltage depends on the value of load resistance. A two-times decrease of the resistance resulted in a decrease of the charging voltage from 500 V to 300 V. In Figure 13a the DC voltage and charging current had a constant value and the output power was about 1 kW. When the rectifier was loaded with the resistance of 30 Ω (Figure 13b), the voltage supplying of the six-pulse diode rectifier automatically decreased. The load current was at the same value of 10 A in accordance with the set point of current limiter in the drive VFC.



(**a**) (**b**)

Figure 13. The DC output voltage and current of EV charger when current limiter in drive VFC is active at different value of rectifier load: (**a**) R = 50 Ω—the current limiter of the inverter is inactive, (**b**) R = 30 Ω—the current limiter of the inverter is active I_{limit} = 8.0 A.

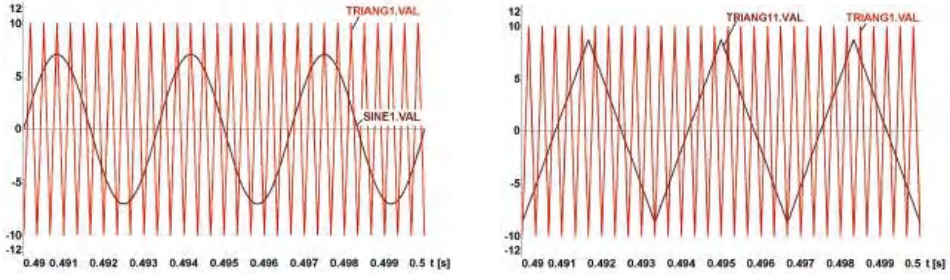
The operation of the drive VFC could be programmed to perform expected functions of an EV battery charger. The experimental tests done for low power setup confirmed the correctness of performed simulation tests and the possibility of using the drive VFC as the basic DC/DC converter component of EV fast chargers.

5. Discussion

When charging the EV battery, the voltage inverter does not use freewheeling diodes (they are inactive), because there is a unidirectional energy flow from the DC microgrid to the diode rectifier. Therefore, it should be assumed that the efficiency of charging system will be similar to the efficiency of a drive VFC. The rectifier diodes cause losses similar to those in the inverter freewheeling diodes when supplying an induction motor.

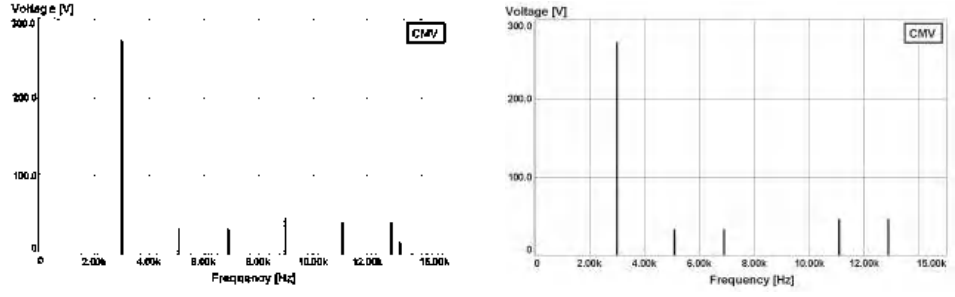
If the drive converter is powered only from the DC microgrid, then it is possible to use one integrated circuit with an inverter and a rectifier to build a DC/DC converter for charging EV batteries.

When building a new converter for battery charging purposes, it is possible to replace sinusoidal modulation, e.g., with triangular modulation. The advantage of using the triangular PWM Figure 14b instead of the sinusoidal PWM (Figure 14a) is the proportional dependence of the value of rectified voltage and modulation factor M. As the amplitude of the triangular of the modulating wave increases linearly (TRIANG11-Figure 14b), there is a directly proportional increase of width modulated pulse. Such proportionality does not occur if the modulating waveform is a sine wave and the modulated waveform is a triangular wave [34]. The spectral analysis of the inverter CM voltage for sinusoidal and triangular modulation shows that there are no significant differences in the CM voltages, in these both kind of PWM modulations as shown in the Figure 14c,d respectively.



(**a**) (**b**)

Figure 14. *Cont.*



(**c**) (**d**)

Figure 14. Comparison of using different modulations: (**a**) sinusoidal modulation, (**b**) triangular modulation, (**c**) harmonics spectrum in the common-mode (CM) voltage using the sinusoidal modulation, (**d**) harmonics spectrum in the CM voltage using the triangular modulation.

6. Conclusions

The authors proposed a DC 600 V microgrid, which is connected to the intermediate circuits of drive VFC used in the induction motor drives. Thanks to this solution, the efficiency of electric drives has increased, as energy losses on brake resistors for drive converters have been eliminated. The actual efficiency of the converter has not been experimentally tested. The efficiency can be estimated on the basis of the efficiency of the driving frequency converters (VFCs), which reaches values of 98% [21].

In the proposed solution, there are also losses in the rectifier, but the reactive component of the current does not flow via the freewheeling diodes of the inverter while charging the EV battery. The reactive component of the current flows via the freewheeling diodes of the inverter while supplying induction motors. Therefore, the authors conclude that the efficiency of the proposed converter for charging EV batteries will be similar to the efficiency of the drive converter.

The bidirectional converter is an adjustable current source for battery and it was used as an example of fast charging battery converter in this paper. The authors' solution is a converter with adjustable EV battery voltage source. Using of the drive frequency converter as an EV battery charging converter is a novel solution where EV battery is charged via a constant voltage source with regulated value.

The energy supplied by the generator is transferred to the energy storage or other converters connected to the microgrid (load sharing). RES and ES cooperate with the microgrid, which has a hybrid DC converter power supply system for fast charging of EV batteries. Scheduled EV battery charging was used, which is carried out in such a way that when the motor is powered by a frequency converter, it is used to charge an EV battery or a mobile electric work machine. The battery charging converter has been developed through the adaptation of drive VFC, consisting of the attachment of a diode rectifier. The VFC drive is used to set the rectifier DC voltage value. The phase voltage value and frequency are controlled by the PWM drive parameters of the drive VFC inverter.

The use of a microgrid provides the opportunity to integrate a hybrid power supply system for fast EV charging stations in such a way that the battery charging energy does not increase the load of the power system and in addition has an impact on worsening the power quality indicators in the power system.

7. Patents

There are three patent applications resulting from the work presented in this manuscript:

1. Power electronic converter with the conversion of alternating voltage into regulated direct voltage for fast charging of batteries in electric vehicles. Patent application no. P-434784 dated 24 July 2020.

2. Power electronic converter with inverter and rectifier for fast charging of electric vehicle batteries. Patent application no. P-434786 dated 24 July 2020.
3. Power electronic converter with a mobile rectifier set for fast charging of electric vehicle batteries. Patent application no. P-434787 dated 24 July 2020.

Author Contributions: Conceptualization, J.R.S., M.Z.-M., D.W. and N.P.; methodology and software, J.R.S. and M.Z.-M.; validation and formal analysis, D.W. and N.P.; investigation and resources, J.R.S., M.Z.-M.; data curation, D.W.; writing—original draft preparation, writing—review and editing, D.W. and M.Z.-M.; visualization, M.Z.-M.; supervision, J.R.S.; project administration, J.R.S., M.Z.-M., D.W. and N.P.; funding acquisition, D.W., N.P. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

AFE	Active Front End
CC	Constant Current
CV	Constant Voltage
CM	Common-mode Voltage
DM	Differential-mode Voltage
ES	Energy Storage
EV	Electric Vehicle
PLC	Programmable Logic Controller
PWM	Pulse Width Modulation
RES	Renewable Energy Sources
SOC	State of Charge
THD	Total Harmonic Distortion
VFC	Voltage Frequency Converter
VSC	Voltage Source Converter

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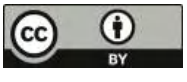

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Suppression of Supply Current Harmonics of 18-Pulse Diode Rectifier by Series Active Power Filter with LC Coupling

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Abstract: The reported research aims at improving the quality of three-phase rectifier supply currents. An effective method consists of adding properly formed booster voltages to the fundamental supply voltages using a series active filter. In the proposed solution, the booster voltages are generated by three single-phase systems consisting of inverters, LC filters, and single-phase transformers. The application of LC couplings ensures low emission of disturbances, but may provoke compensator stability problems. The article presents the current control system for a series active filter designed to suppress the dominant harmonics in the supply currents of an 18-pulse rectifier, without interference into fundamental current components. A proportional control is proposed in combination with integral terms implemented in the orthogonal coordinate systems, which synchronically rotate with frequencies equal to those of the harmonic components to be eliminated. The use of complex gains in integral terms allows a simple phase correction of the output signals. A description is given of the method to determine controller parameters based on the mathematical model of the control object. Sample results of experimental tests performed in steady-state and transient conditions are included to illustrate the quality of performance of the series active filter as compared to the results recorded for the rectifier alone, and for the rectifier with additional line reactor. The applied control method of active filter significantly reduces harmonic distortion of the grid current, which is particularly advantageous at nonideal supply voltage and low loads.

Keywords: series active power filters; multipulse converters; power conditioning; coupled reactors

1. Introduction

Diode rectifiers are frequently used in industry, because of their low cost, high reliability, and low-level emission of disturbances. Unfortunately, the simplest rectifier solutions usually draw a highly distorted current from the electrical grid. However, after many years of deploying them in the industry, effective methods have been developed to improve the quality of the input current. One of these methods is the use of multipulse rectifiers [1–4], whose supply line current has a multistep shape which is characterized by a lower content of higher harmonics. If the galvanic separation is not required and there is no need to adjust the voltage between the supply line and the load, then the multipulse diode rectifiers with coupled reactors are a good solution. The main advantage, in comparison to multipulse converters with transformers, is the much smaller limiting power of the required electromagnetic elements, resulting in the smaller dimensions and weight of the entire rectifying device [5,6]. The downside is that when the supply voltage is unsymmetrical with higher harmonics it results in distortions of the supply current [5]. In such cases, it is advisable to use

an additional smaller rated Series Active Power Filter (S-APF), which further improves the power quality [7].

Several control methods of the S-APF connected to the input of a multipulse rectifier are presented in the literature [8–12]. The first developed control algorithms were implemented using analogue control techniques [8,9]. The fundamental harmonic was removed from the supply currents, and the remaining signal was properly amplified and added to the rectifier supply voltages, thus reducing current distortion. However, in the case of digital control, due to unavoidable delays in the S-APF control system, this method did not bring satisfactory results [10]. That is why a DFT (discrete Fourier transform) based control algorithm [10] has been proposed, in which only dominating harmonics of the supply current are extracted and suppressed. Unfortunately, the authors did not use a switching-ripple filter in the S-APF system and provided only general guidelines for the selection of the regulator parameters.

Digital control of S-APF as a current source based on the hysteresis controller was proposed in [11] by the authors of this article. In [12] instead of current controllers with a large bandwidth, proportional-integral controllers in multiple reference frames were used for selective line current harmonic suppression. Both solutions ensure very good quality of rectifier supply currents, but insufficiently suppress current and voltage ripples caused by transistor switching. This article presents the research results of the S-APF system additionally equipped with the LC ripple filter, and the current controller with a simple structure, which enables additional phase correction of the outputs of integral terms.

2. Converter System Characteristic

A simplified schematic diagram of the analyzed ac/dc supply system is shown in Figure 1.

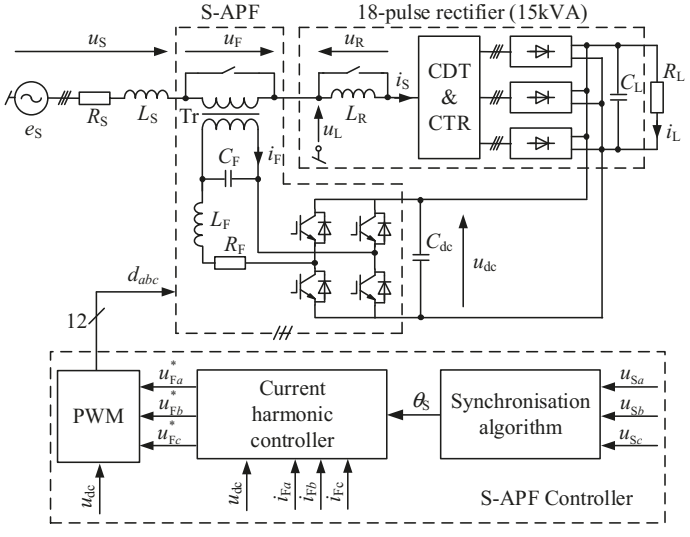


Figure 1. Schematic diagram of the proposed ac/dc supply system based on 18-pulse rectifier and series active power filter with LC output stage.

Three-phase supply is modeled by the voltage source e_S, resistance R_S, and inductance L_S, which also represents the leakage inductance of a rectifier's magnetic circuits. The system is composed of two separate modules: an 18-pulse rectifier, and a series active filter. Three system configurations are possible: (1) only 18-pulse rectifier, (2) rectifier with additional series reactor, and (3) rectifier with the series active filter. The main element of the system is the 18-pulse rectifier based on current

dividing transformer (CDT) for preliminary current division, and the set of coupled three-phase reactors (CTR) [5]. The above magnetic elements compose three 3-phase voltage systems, shifted by 20° in relation to each other. Six-pulse rectifiers with a shared output capacitor are connected to CTR outputs. The 18-pulse rectifier enables reduction of undesired higher harmonics from the supply network currents, mainly of the order of 5, 7, 11, and 13.

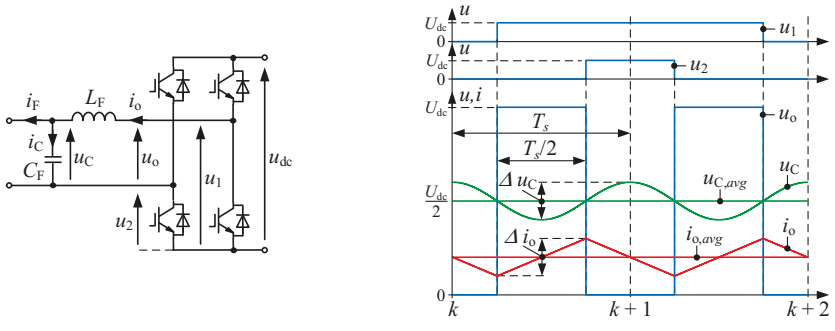
The series active filter consists of three single-phase circuits, each composed of a voltage source inverter (VSI) with IGBTs transistors. The dc circuits of these inverters are connected to the output of the 18-pulse rectifier. The ac sides of the inverters are series-connected to the supply voltage via LC filters and step-up transformers (Tr) with voltage ratio 1:12. During system start-up and operation only with the rectifier, the S-APF is bypassed by a contactor.

The parameters of the converter system are given in Table 1. The supply resistance and inductance were measured using the loop impedance meter. The series injection transformer (Tr) was selected through simulation research, based on the results presented in [8,13]. The transformer is represented by its classical circuit model, excluding a magnetizing branch. The transformer parameters listed in Table 1 were determined on the basis of a short-circuit test.

Table 1. Parameters of the proposed ac/dc supply system.

Symbol	Description	Value
E_S	Phase voltage of the supply (50 Hz)	230 V
L_{Sp}	Supply inductance referred to the primary side of the transformer	7.2 mH
R_{Sp}	Supply resistance referred to the primary side of the transformer	57.6 Ω
P_{REC}	Nominal output power of the 18-pulse rectifier	15 kW
C_L	Rectifier output capacitance	10 mF
S_T	Nominal power of the series injection transformer (Tr)	800 VA
U_{Tp}	Nominal primary voltage of the transformer Tr	300 V
I_{Tp}	Nominal primary current of the transformer Tr	2.9 A
N_T	Turns-ratio of the series injection transformer Tr	12
L_T	Leakage inductance of the windings of the transformer referred to the primary side	3.46 mH
R_T	Resistance of the windings of the transformer referred to the primary side	3.7 Ω
L_{TS}	Equivalent inductance, sum of L_T and L_{Sp}	10.66 mH
R_{TS}	Equivalent resistance, sum of R_T and R_{Sp}	61.3 Ω
L_F	Inductance of the switching ripple filter inductor	20 mH
R_F	Resistance of the switching ripple filter inductor	0.5 Ω
C_F	Capacitance of the switching ripple filter	0.56 µF
T_d	Delay introduced by control system and VSI	75 µs
f_s	Sampling and PWM switching frequency	20 kHz

The inductance (L_F) and capacitance (C_F) of the switching ripple filter were selected assuming the maximum ripple of the inductor current and the capacitor voltage. Figure 2a shows a simplified circuit diagram of the VSI and its output filter to define the signals, the waveforms of which are presented on Figure 2b. It shows the branch voltages u_1, u_2 and the output voltage u_o of the VSI, as well as the capacitor voltage u_C and its averaged value over the sampling period $u_{C,avg}$. In addition to the voltages, the figure also shows, in an idealized way, the VSI output current i_o and its averaged value over the sampling period $i_{o,avg}$. In the case of unipolar modulation with the double update mode the largest ripples of inductor current occur when the duty cycle $m = u_o/u_{dc}$ is equal to 0.5. The simplified waveforms in Figure 2b apply to this case.



(**a**) (**b**)

Figure 2. Simplified circuit diagram of the VSI and switching ripple filter (**a**) and waveforms of the characteristic signals in the case of maximum ripples of capacitor voltage and inductor current (**b**).

Taking into account the time interval of length $T_s/2$ (Figure 2b), in which the current i_o increases from the minimum value to the maximum, the peak-to-peak value of the current ripple Δi_o can be calculated from the formula [14]:

$$\Delta i_o = \frac{U_{dc}}{4L_F f_s}, \tag{1}$$

where U_{dc} is the maximum *dc* link voltage equal to 500 V.

Lower current ripple reduces inductor high frequency losses and for this reason a choke with a relatively high inductance L_F = 20 mH was selected. The maximum current ripple is at 11% of the peak nominal input current of the 18-pulse rectifier current, referred to the primary side of the transformer Tr.

Considering the time interval $T_s/2$, in which the capacitor voltage u_C varies from the minimum to the maximum value (Figure 2b), the maximum capacitor voltage ripple Δu_C can be estimated by the equation [14]:

$$\Delta u_C = \frac{\Delta i_o}{8C_F f_s} = \frac{U_{dc}}{32L_F C_F f_s^2}, \tag{2}$$

It was assumed that the capacitor voltage ripple should not exceed 1% of the peak output voltage of the VSI, which is equal to U_{dc} in the worst case. Finally, the value of C_F = 560 nF was selected, for which maximum Δu_C equals 3.5 V (0.7% of the U_{dc}).

The control algorithm was implemented in the microprocessor controller based on the digital signal processor TMS320C6713 and the programmable system FPGA Cyclone IV. To execute the control algorithm, measurements were performed of the supply network phase voltages (u_{Sa}, u_{Sb}, u_{Sc}), transformer phase currents (i_{Fa}, i_{Fb}, i_{Fc}) on the inverter side, and the rectifier output voltage u_{dc}.

3. The Structure of Multiple Reference Frame Current Controller

The task of the series active filter is to improve the quality of the supply current by suppressing higher harmonics and compensating the asymmetry of the fundamental components. A simplified schematic diagram of the S-APF control system is shown in the lower part of Figure 1. Three functional blocks are singled out in this part: pulse width modulator (PWM), synchronization algorithm [12,15], and the current controller, which will be described in detail further in the article. It was developed on the basis of the research results reported in [12,16–18].

In order to implement the control system, the three-phase quantities x_a, x_b, and x_c were converted using the space vector defined as:

$$\underline{x}_{\alpha\beta} = x_{\alpha\beta} + \mathrm{j}x_{\alpha\beta} = \frac{2}{3}\left(x_a + x_b e^{\mathrm{j}2\pi/3} + x_c e^{-\mathrm{j}2\pi/3}\right). \tag{3}$$

In steady state, the current space vector $\underline{i}_{F\alpha\beta}$ can be approximated by a complex Fourier series given by the formula:

$$\underline{i}_{F\alpha\beta} = \sum_{m=-\infty}^{\infty} \underline{I}_{\mathrm{F}\alpha\beta m} e^{\mathrm{j}m\omega_1 t} \cong \sum_{m\in M} \underline{I}_{\mathrm{F}\alpha\beta m} e^{\mathrm{j}m\theta_1}. \tag{4}$$

where $\underline{I}_{\mathrm{F}\alpha\beta m} = \left|I_{\mathrm{F}\alpha\beta m}\right| e^{\mathrm{j}\varphi_m}$ is the complex-valued amplitude of m-th current harmonic belonging to the set of M dominant harmonics to be suppressed; ω_1 is the frequency of the fundamental component, and θ_1 is its instantaneous phase.

The 18-pulse rectifier draws the distorted current from the supply source. The dominating frequencies in this current are of the order of $m = -17, 19, -35, 37, \ldots$ while the harmonics of the space vector of supply network voltage are usually of the order of $m = -1, -5, 7, -11, 13, \ldots$, where the component $m = -1$ represents the asymmetry of fundamental components of phase voltages. Suppressing the harmonics of the above orders is the basic task of the proposed current controller. Additional S-APF functions, requiring the adjustment of the fundamental harmonic of the rectifier supply voltage, such as the power factor compensation or stabilization of the rectifier's output voltage are not implemented in considered system. They require the use of a series transformer with a higher rated power and an appropriate voltage ratio and also increase the S-APF power losses [13].

The block diagram of the current controller is shown in Figure 3. To limit the S-APF power losses related to the first harmonic, the proposed current controller should not affect the fundamental component of the current taken from the supply network. Consequently, this harmonic was removed from the space current vector $\underline{i}_{F\alpha\beta}$ using the fundamental component filter [12] based on recursive discrete Fourier transform. The signal $\underline{e}_{F\alpha\beta}$ created in the above way is the control error, assuming that the reference value for all compensated current harmonics is zero.

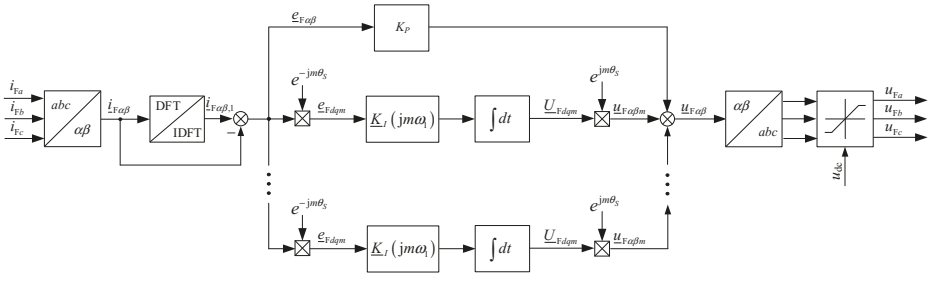


Figure 3. Simplified block diagram of the current harmonic controller.

The error signal is given to the input of the proportional term of the current controller, and to the inputs of the integral terms implemented in the synchronous coordinate systems dq_m, the number of which is equal to the number of compensated current harmonics. The error signal is converted to m synchronous coordinate systems by multiple Park transformations defined by the formula:

$$\underline{e}_{\mathrm{F}dqm} = \underline{e}_{\mathrm{F}\alpha\beta} e^{-\mathrm{j}m\theta_S}, \tag{5}$$

where $\underline{e}_{\mathrm{F}dqm}$ is the error signal converted to the coordinate system dq_m rotating with frequency $m\omega_S$, ω_S is the estimated frequency of fundamental component, and $\theta_S = \omega_S t$ is the estimated instantaneous phase. After transformation, the control error harmonic of the order m becomes a constant component in dq_m

frame and is amplified by the integral term of current controller which corresponds to this harmonic. Simultaneously, the remaining harmonic components in the output signal $\underline{U}_{\mathrm{F}dqm}$ are suppressed:

$$\underline{U}_{\mathrm{F}dqm}[k] = \sum_{n=k_0}^{k} \underline{K}_i(\mathrm{j}m\omega_1)\underline{e}_{\mathrm{F}dqm}[n], \tag{6}$$

where k_0 is the time of control algorithm activation, and $\underline{K}_i(\mathrm{j}m\omega_1)$ is the complex-value gain of the frequency-dependent integral term of the controller.

In the proposed controller implementation, the integral gain is a complex number which also determines relevant phase shift of the output signal of this block after its reconversion to the coordinate system $\alpha\beta$ using the inverse Park transform:

$$\underline{u}_{\mathrm{F}\alpha\beta m} = \underline{U}_{\mathrm{F}dqm}e^{-\mathrm{j}m\theta_S}. \tag{7}$$

The sum of output signals from particular integral terms and from the proportional part is the controller output signal in the coordinate system $\alpha\beta$.

$$\underline{u}_{\mathrm{F}\alpha\beta} = K_p\underline{e}_{\mathrm{F}\alpha\beta} + \sum_{m\in M} \underline{u}_{\mathrm{F}\alpha\beta m}. \tag{8}$$

when it is too large, the modulus of the output voltage space vector $\underline{u}_{\mathrm{F}\alpha\beta}$ is limited to the voltage in the *dc* circuit. The calculated output signal from the current controller is passed to the input of pulse width modulator.

4. Selection of Controller Settings

When selecting controller settings, the magnetizing branch in the transformer model was omitted. Then, the transfer function of the circuit coupling the inverter with the supply network takes the form:

$$G_o(s) = \frac{1}{s^3L_FL_{TS}C_F + s^2C_F(L_FR_{TS} + L_{TS}R_F) + s(L_F + L_{TS} + C_FR_FR_{TS}) + R_F + R_{TS}}e^{-sT_d}. \tag{9}$$

Selection of controller settings started with determining the gain of the proportional part of the controller. This setting was calculated based on the assumed gain margin for the open-loop system working only with the proportional controller. For the assumed gain margin of 10 dB, the calculated proportional coefficient was equal to K_p = 44.

To select the integral gains, the current control system was treated as a multiloop scheme, the inner feedback loop of which consists only of a proportional term [18]. Then, the integral gains were selected in such a way as to compensate the remaining errors for the frequencies of dominant harmonics. The error which should be compensated by the integral terms is given by the following transfer function:

$$G_e(s) = \frac{E_{F\alpha\beta}(s)}{U_I(s)} = \frac{G_o(s)}{1 + K_pG_o(s)} = \frac{1}{K_p}G_{cp}(s), \tag{10}$$

where $E_{F\alpha\beta}(s)$ is the Laplace transform of the control system error, $U_\mathrm{I}(s)$ is the Laplace transform of the output signal of the integral part (corresponding to the sum of output signals from individual integral terms), and $G_\mathrm{cp}(s)$ is the transfer function of the closed-loop system when only the proportional controller is used:

$$G_{cp}(s) = \frac{K_pG_o(s)}{1 + K_pG_o(s)}. \tag{11}$$

Figure 4 shows the Bode plots of the open and closed-loop control system with only the proportional term. The proportional controller with fixed setting is not able to suppress harmonics effectively. The task of the integral terms is to increase controller gain for selected frequencies. Considering the

formula (8), the transfer function of the integral term of the proposed controller in the stationary coordinate system $\alpha\beta$ is as follows:

$$G_{im}(s) = \frac{U_{F\alpha\beta m}(s)}{E_{F\alpha\beta}(s)} = \underline{K}_i(jm\omega_1)\frac{1}{s - jm\omega_1}, \tag{12}$$

in which the complex-value integral gain, shown in the scheme in Figure 3, is given by:

$$\underline{K}_i(jm\omega_1) = \frac{K_p}{T_i\underline{G}_{cp}(jm\omega_1)}. \tag{13}$$

where the controller integration time was assumed equal to $T_i = 0.5/f_1 = 10$ ms.

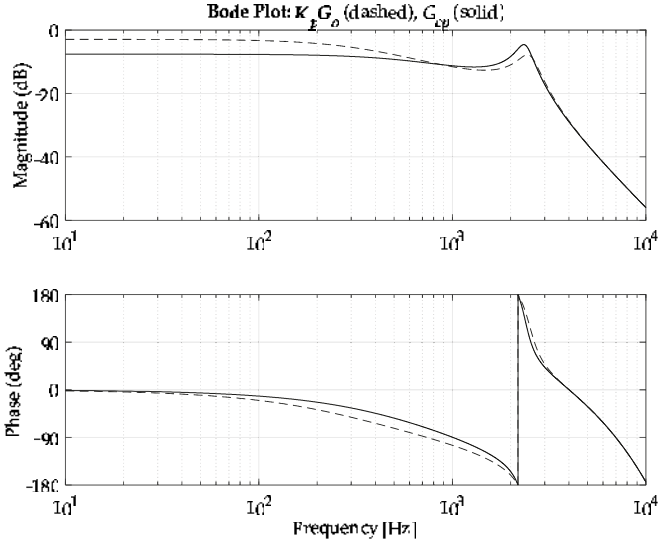


Figure 4. Bode plots of open-loop and closed-loop control systems with proportional controller.

The gains of the integral terms have complex values and ensure proper phase correction of particular output signals $u_{F\alpha\beta m}$, without additional trigonometric function calculations.

5. Laboratory Results

To verify the operation of the S-APF control algorithm, a series of experimental tests were performed. The task of the current controller was to suppress current harmonics of the following orders: -1, ± 3, $\pm(6n \pm 1)$ for $n = 1, 2, \ldots, 6$. Firstly, the steady-state operation of the current control system was tested. The obtained results were compared with the data recorded for two remaining configurations of the converter system. Figure 5 shows sample oscillograms of supply currents and their amplitude spectra recorded at nominal load: (1) for only 18-pulse rectifier (Figure 5a,b), (2) for rectifier with additional series reactor L_R (Figure 5c,d), and (3) for rectifier with series active filter (S-APF) (Figure 5e,f). The waveforms of the phase currents with their amplitude spectra and THD (total harmonic distortion) values were recorded and calculated using the Precision Power Analyzer LMG670 made by Zes Zimmer. The amplitude spectra of the supply currents are given in logarithmic scale.

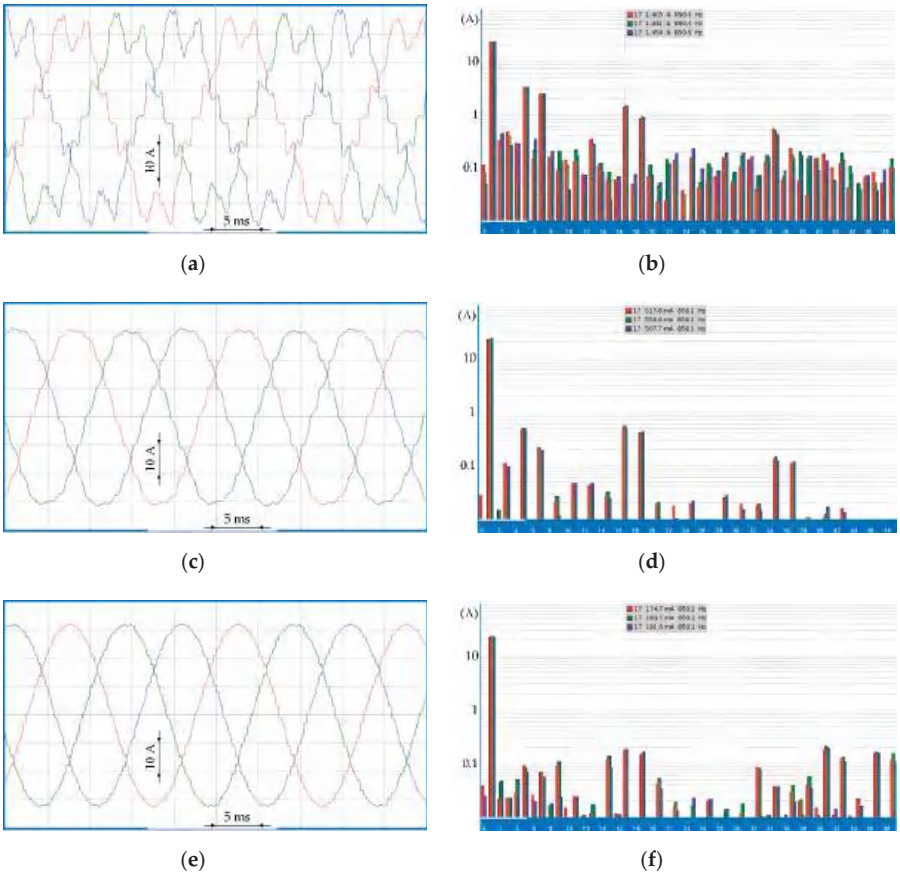


Figure 5. Oscillograms and spectra of converter supply currents at nominal load: (**a**,**b**) system without reactor L_R and S-APF; (**c**,**d**) system with reactor L_R and without S-APF; (**e**,**f**) system without reactor L_R and with S-APF.

The amplitudes of the dominant harmonics are the lowest when using S-APF. In each spectrum shown in Figure 5, the amplitudes of the 17-th harmonic (about 850 Hz) are marked for three phase currents. The application of the series reactor reduced the values of this harmonic from the level of 1.433 A to 0.525 A, while the use of S-APF to the level of 0.180 A. In general, all dominating harmonics considered in the current controller with S-APF were reduced, as compared to the remaining configurations.

Figure 6 shows the results of measurements of supply current THD and output voltage for three system configurations. The introduction of a series reactor alone has already reduced significantly the harmonic distortion of supply currents as compared to the autonomous operation of the 18-pulse rectifier. Replacing the reactor L_S with the S-APF system improves the quality of supply currents within the entire output power range. For the configuration with S-APF operating at nominal load, the THD of supply currents remains at the approximate level of 2%. Significant improvement in quality of supply currents can be observed during converter system operation at low load. Compared to the configuration with additional series reactor, the system with S-APF also ensures slightly higher output voltage.

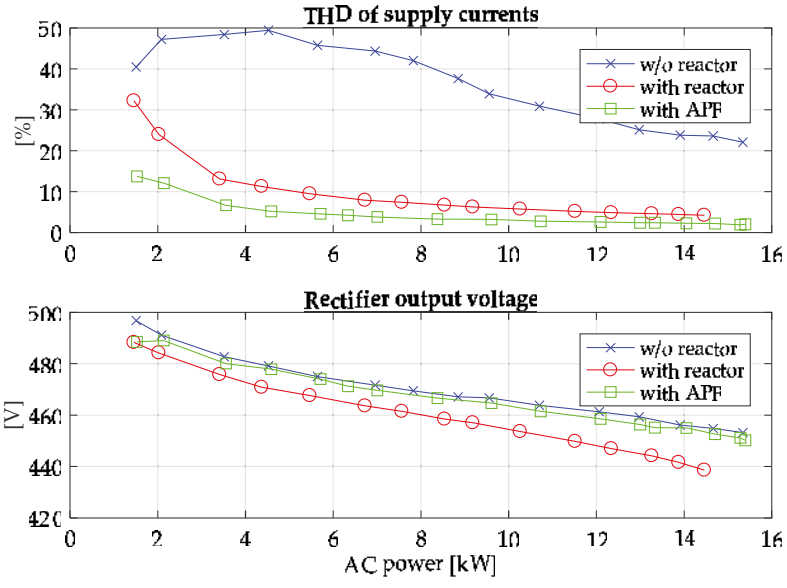


Figure 6. THD of supply currents (**top**) and rectifier output voltage (**bottom**) as functions of input power for three converter system configurations.

Figures 7–9 show sample results of converter system examination in dynamic states. The values of supply network currents were measured and recorded in the converter control system unit. To illustrate the quality of the controller's performance, THD values of the supply current are shown, which were obtained from harmonic values calculated in moving window with fixed width corresponding to frequency 50 Hz:

$$THD[k] = \frac{\sqrt{\sum_{m=-40}^{-1} \left|\underline{I}_{S\alpha\beta m}[k]\right|^2 + \sum_{m=2}^{40} \left|\underline{I}_{S\alpha\beta m}[k]\right|^2}}{\left|\underline{I}_{S\alpha\beta 1}[k]\right|}, \tag{14}$$

where $\underline{I}_{S\alpha\beta m}[k]$ is the amplitude of m-th harmonic of the supply current converted to the coordinate system $\alpha\beta$, calculated in the moving window, and $\underline{I}_{S\alpha\beta 1}[k]$ is amplitude of fundamental harmonic of the supply current.

Figure 7 shows the waveforms of supply network currents and THD values after control algorithm activation when the system is loaded with half of the nominal power. During two supply network voltage periods, significant reduction in the level of harmonic distortion is observed, from about 36% to 14.5%, with further slower reduction to the approximate level of 3.7%.

Figures 8 and 9 show sample transient states related with load change at converter system output. Figure 8 presents the step increase of load from 33% to 100%, while Figure 9 shows the reverse situation, i.e., rapid load drop.

In both situations, the converter system operation is stable and leads to the reduction of supply current harmonic distortions after the transient state. Unfortunately, during transients the THD values are not a meaningful indicator and reach disproportionately high values in relation to the level of distortion visible in the current waveforms.

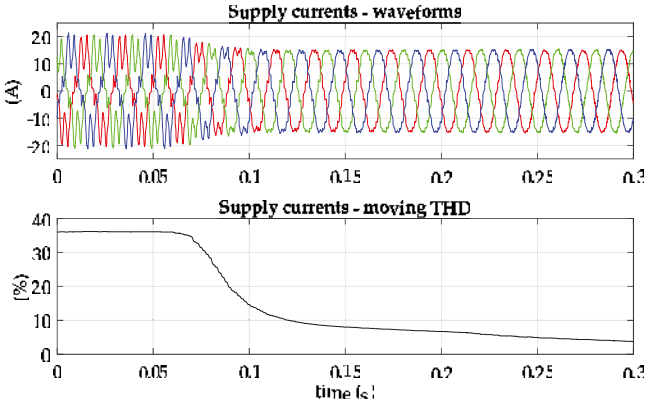


Figure 7. Supply current waveforms and THD values recorded after initiating the current control algorithm.

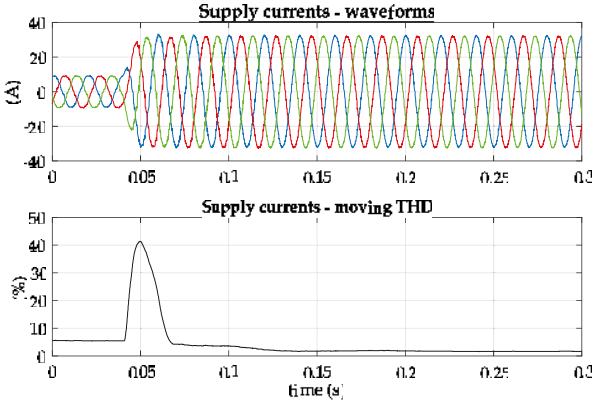


Figure 8. Supply current waveforms and THD values recorded after load increase from 33% to 100%.

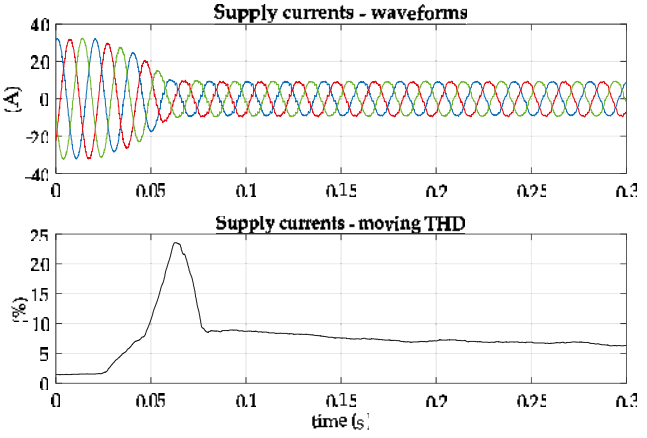


Figure 9. Supply current waveforms and THD values recorded after load decrease from 100% to 33%.

6. Conclusions

The article proposed a current harmonic controller for a series active filter integrated with 18-pulse diode rectifier with coupled reactors. The ac sides of S-APF inverters were coupled with booster transformers via LC filters, which enables significant reduction of booster voltage ripples, but may lead to unstable operation of the converter system.

To suppress undesired harmonics in supply currents, a proportional controller was used with integral terms implemented in multiple coordinate systems, rotating synchronously with angular frequencies of the dominant harmonics. The use of integral gains with complex values, ensures proper phase correction of integral's output signals and stable operation of the converter system.

The proposed current controller suppresses dominating harmonics up to the order of 37. For nominal load, the controller can reduce the THD coefficient from 22% to about 2%.

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The Unified Power Quality Conditioner Control Method Based on the Equivalent Conductance Signals of the Compensated Load

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Abstract: This paper proposes a new control method for a Unified Power Quality Conditioner (UPQC). This method is based on the load equivalent conductance approach, originally proposed by Fryze. It can be useful not only for compensation for nonactive current and for improving voltage quality, but it also allows one to perform some unconventional functions. This control method can be performed by extending the orthodox notion of 'static' load equivalent conductance into a time-variable signal. It may be used to characterize energy changes in the whole UPQC-and-load circuitry. The UPQC can regulate energy flow between all sources and loads being under compensation. They may be located as well for UPQC's AC-side as DC-side. System works properly even if they switch their activity to work either as loads or generators. The UPQC can operate also as a buffer, which can store/share the in-load generated energy amongst other loads, or it can transmit this energy to the source. Therefore, in addition to performing the UPQC's conventional compensation tasks, it can also serve as a local energy distribution center.

Keywords: power quality; power distribution; reverse power flow; compensation for nonactive current; voltage regulation; UPQC

1. Introduction

It is well known that distortions of supply voltage and load current cause power quality degradation, diminish the power factor of the supply system and may result in disruption of sensitive loads [1]. Shunt and series active power filters can alleviate these problems. Shunt filters are intended to compensate for load non-active current whereas series ones can improve supply voltage quality. The Unified Power Quality Conditioner (UPQC) can integrate advantages of both shunt and series active filters in order to achieve control over load voltage and source (line) current [2,3].

A wide review on UPQC configurations can be found in [3]. According to this classification the discussed UPQC can be classified as intended for a single-phase supply system that is based on a two-H-bridge converters employing the same DC-link capacitor. Depending on the point of injecting the compensating current with respect to the injecting transformer (Figure 1), the UPQC under study can be implemented as well in the UPQC-R (right-side shunt) as UPQC-L (left-side shunt) configuration. It is also classified as UPQC-P—It compensates source voltage sags using active power of supply sources. UPQCs can obtain reference signals on the base of frequency or time domain detection methods. Some researchers argue that "Harmonic current estimation is the key technology of power electronics systems to generate a harmonics reference current for harmonic control" and propose extensive and flexible solutions in this field [4]. Other researchers develop time-domain techniques [5,6]. Since the considered UPQC calculates references for load voltage and line current directly on the base of time variable quantities it can be classified as operating using time-domain signal analysis. In particular, this method refers to Fryze's concept of the load equivalent conductance [7].

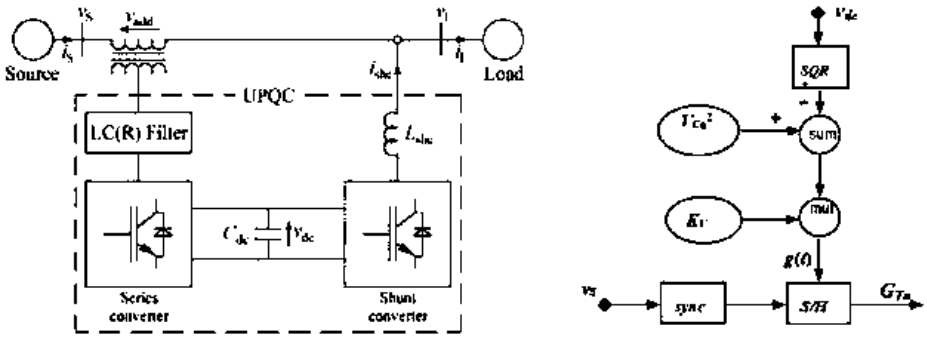

Figure 1. UPQC power circuitry diagram and scheme of obtaining conductance signal on the base of DC-link capacitor voltage v_{dc}, according to Equation (6). The S/H block is an sample-and-hold module that is synchronized with source voltage waveform using *sync* block.

Commonly used control methods of UPQC involves continuous measurement of source voltage and load voltage and current in order to calculate reference signals for UPQC action. Such control methods are known as direct control techniques. However, UPQC can be steered using a somewhat different scenario, which may be classified as the indirect control method [8–12]. A type of the indirect method, which has been dubbed the conductance signal control method, has been successfully implemented to control the shunt active power filter (SAPF) action [9]. However, there is no implementation of this technique for UPQC so far. Applying the conductance signal control method references required to control the UPQC operation are obtained on the base of measuring the voltage across the UPQC's DC-link capacitor. Since for this method the capacitor is employed as "a sensor" of load active power its voltage must not be controlled to be constant. On the contrary, the "freewheeling" capacitor voltage is measured and processed in order to obtain an equivalent (or hypothetical) conductance element that characterizes the consumption of the total active power taken from the source [8]. Since the load active power may vary in time, this conductance element should also be considered as time-dependent one. The ongoing information on conductance of this element may be referred to as the conductance signal. The first part of this paper shows that the conductance signal can be used to control the UPQC action.

As it turns out, if the conductance signal method is used some noteworthy additional functionalities of UPQC can be obtained. In particular, the UPQC can also be used to control the flow of energy between the supply source and the AC or DC passive or active elements of the network being connected with the particular UPQC. It can be said that in addition to perform the UPQC's conventional tasks, it can also serve as a local energy distribution center operating with high power factor. This center may serve as a spot improving grid's energetic efficiency. The second part of this paper describes these extra UPQC's functionalities.

There are many other technical problems related to UPQC extended operation in smart grids. From this perspective problems of UPQC real-time control [13–16] and their optimal sizing and siting are considered very important [13–19].

2. Control of UPQC with the Use of Signal of Load Equivalent Conductance

2.1. Basic Scheme of UPQC

From the point of view of the studied control method the UPQC can be considered as composed of: (1) the shunt converter, which shapes source current i_S to be active and of amplitude required to supply the load with the required active power and maintains the UPQC's DC-link capacitor voltage in the assumed range, and (2) of the series converter, which tracks the supply voltage v_S and—If needed—injects suitable voltage corrections v_{add} (Figure 1). As the result load voltage v_L is shaped to be sinusoidal and of nominal amplitude. In the vast majority of cases the control circuitry

of the UPQC's shunt converter steers also the operation of the entire UPQC filter. The same rule is applied in this paper. A comprehensive review on the possible shunt converter control techniques can be found in [20,21].

2.2. Principle of UPQC's Shunt Converter Control

The control unit of the shunt converter processes the voltage signal of the UPQC's DC-link capacitor C_{dc}, Figure 1, in order to obtain the conductance signal. This signal gives crucial information needed to produce the reference for the source current. The conductance signal can be used to obtain the current reference signal as well for the shunt active power filter (SAPF) as for UPQC's shunt converter.

In general, the compensated load may be nonlinear, time variable, passive or active, of single or polyphase structure with or without the neutral conductor, unbalanced, etc. From this perspective applying an universal method for obtaining the signal of equivalent conductance would be beneficial. Such an universal method, which allows this signal calculation as a function of amount of energy stored in the active filter's reactance elements, has been proposed in [8]:

$$g(t) = \frac{(W_{APF0} - w_{APF}(t))(N_{SF} + 1)}{T_{st} V_S^2} \tag{1}$$

where: $g(t)$ is the instantaneous load equivalent conductance signal; W_{APF0} is initial amount of energy, which has been stored in all UPQC's reactance elements during UPQC initialization procedure; $w_{APF}(t)$ is amount of energy stored in these elements at instant t; N_{SF} is the ratio of amount of energy delivered to the load from the supply source with respect to energy that is simultaneously delivered to the load from UPQC's reactance elements—After each instant of change of load active power until the moment of achieving a new stead state by UPQC; T_{st} is a user dependent parameter that may be utilized to define UPQC time response on change of load active power; V_S is source voltage rms.

The Equation (1) can be simplified to the form that only information on a part of total amount of energy stored in the UPQC is taken into account: namely that is stored in its DC-link capacitor:

$$g(t) = \frac{C_{dc}\left(V_{C0}^2 - v_{dc}^2(t)\right)(N_{SF} + 1)}{2T_{st} V_S^2} = K_V\left(V_{C0}^2 - v_{dc}^2(t)\right)(N_{SF} + 1) \tag{2}$$

where C_{dc} is capacity of DC-link capacitor, V_{C0} is its initial (i.e., after UPQC initialization procedure, see also W_{APF0} in Equation (1)) voltage and $v_{dc}(t)$ is its voltage at instant t, and where:

$$K_V = \frac{C_{dc}}{2T_{st} V_S^2} \tag{3}$$

It is characteristic for the discussed control technique that the DC-link capacitor voltage is not controlled to be constant. On the contrary, the "freewheeling" capacitor voltage is an input signal for obtaining the conductance signal. The K_V factor gives a proportion between a signal related to the DC-link capacitor voltage and the conductance signal. The K_V factor has a practical meaning: it may be used as the gain coefficient of a simple P-type regulator in the active filter's control unit. No other signal converters of DC-link capacitor voltage are needed to obtain the conductance signal (Equation (2)).

There is a parameter T_{st} in the denominator of Equation (3). By changing this parameter the user can control the UPQC's shunt converter inertial response on any change of load active power. By increasing/decreasing magnitude of this parameter more/less energy of each change of load active power can be buffered by DC-link capacitor. In other words, the T_{st} parameter can be used to regulate the energy flow between the source and the load in order to stabilize (or average) the source active power.

Having the conductance signal the reference for source current can be determined by the relationship:

$$i_S^*(t) = g(t)v_{1S}(t) \tag{4}$$

where $v_{1S}(t)$ is fundamental component signal of source voltage. This component can be obtained in many ways (e.g., using filtration or PLL based techniques).

A variable component may appear in conductance signal (Equation (2)) if the load current contains a non-active component. Since UPQC compensates such component with the use of energy stored in its reactance elements (Equation (1)) this cause an oscillating component in DC-link capacitor voltage (Equation (2)). This component can distort the reference (Equation (4)). In order to eliminate impact of this component on the reference (Equation (4)) the continuous signal (Equation (2)) should be transformed into the stepwise waveform. To do this the signal (Equation (2)) is sampled at the very end of each subsequent period T_m of source voltage cycle. Then each sample is hold for the next period T_{m+1}, [8]. Application of such sample-and-hold procedure causes a "step-by-step" UPQC's shunt converter action in that every change in load active power is practically entirely buffered with energy stored in the DC-link capacitor. For such method of full-buffering of energy flow the N_{SF} parameter, see Equations (1) and (2), should be set to zero. As the result the source-to-load flow of energy is delayed for one period T and the stepwise form of the conductance signal applied for a T_m period is given by:

$$G_{T_m} = \frac{C_{dc}\left(V_{C0}^2 - v_{dc}^2(T_{m-1})\right)}{2T_{st}V_S^2} \tag{5}$$

where: $v_{dc}(T_{m\text{-}1})$ is capacitor C_{dc} voltage at the end of (m-1)th period T.

Finally, on the base of Equations (4) and (5) the source current reference signal $i_S{}^*$ for period T_m is:

$$i_{S,T_m}^*(t) = G_{T_m}v_{1S}(t) \tag{6}$$

It should be emphasized that during compensation the following inequality has to be satisfied:

$$v_{dc}(t) >> v_S(t) \tag{7}$$

If this condition is not satisfied the UPQC dynamics can be insufficient. In an extreme case, when $v_{dc}(t) < v_S(t)$, the UPQC action may become even harmful.

2.3. Principle of UPQC's Series Converter Control

Source voltage waveform may deviate from its fundamental component due to wide range of physical phenomena existing in the grid. They may be considered as voltage harmonics, flicker, swell or sag, or pulse transients. There are specialized devices to overcome power quality problems that are related to voltage disturbances. The dynamic voltage restorer (DVR) seems to be the most economical solution in this field, [22]. However, UPQC's series converter can maintain the load voltage v_L to be close to the fundamental component v_{1S} of the source voltage v_S.

Independently of the reason of voltage distortion its shape bettering can be performed with the use of the same conductance signal-based control method considered. In other words, there is no need to identify the reason or spectrum of the source voltage distortion. In any case it is sufficient to inject the adequate voltage correction v_{add} in series with the source voltage v_S (Figure 1). To produce appropriate voltage correction v_{add} the series converter generates (using energy stored in the DC-link capacitor) the current flow through the converter's side winding of the injecting transformer. The hysteresis controller compares load voltage to its reference, i.e., the source voltage fundamental component, and steer switches action of the series converter in order to keep this voltage near this reference. As the result the required voltage v_{add} appears across the grid side winding of the injecting transformer.

Voltage and current distortion components may be considered as nonactive ones. Therefore, while compensating and being in the steady state, both UPQC converters impact the compensated voltage/current runs using nonactive power only, i.e., without change of mean magnitude of DC-link capacitor energy (if skip energy loss in the UPQC circuitry). In such situation the load conductance signal is still constant and, consequently, source current amplitude is constant as well. This observation is important from the perspective of the considered control method.

However, for the control method considered each change of load active power cause change of the conductance signal. Also energy losses in UPQC circuitry influence the total load-and-UPQC active power, so they impact the conductance signal (Equation (5)). It can be then said that there are no changes of signals (Equations (5) and (6)) when load active power is constant and the UPQC's series converter compensates only for higher harmonics of source voltage. On the contrary, the signals (Equations (5) and (6)) get new magnitude when the series converter counteracts change of source voltage rms, or if there is a change in source voltage harmonic content. As a result the source is loaded higher/lower in order to maintain constant voltage rms across load terminals.

Finally, as an important conclusion it can be said, that all energy relations between the UPQC's series converter and the rest of the system considered can be supervised by the control unit of the UPQC's shunt converter and there is no operational incompatibility between both converters.

3. Studies for UPQC Standard Operation

The considered control method has been extensively verified by means of computer simulation. The IsSpice software (Intusoft, San Pedro, CA, USA) has been used. During some analyses performed the deformation of source voltage and load current often went beyond the voltage and current runs encountered in practice. They caused strong overload of UPQC circuitry. This approach, attractive in simulation studies, allows to assess the usability area of the considered UPQC control method.

In this paper simulation studies are divided into two parts. The first one, Section 3, considers UPQC standard operations, i.e., compensation for nonactive current and improving the voltage waveform on load terminals. The second part, Section 4, describes additional UPQC functionalities that arise if the conductance signal control method is used. In particular, this section considers the possibility of using UPQC as a distribution center for locally generated power.

For all analyses performed the same supply source characteristic and UPQC circuitry were used:

(1) Supply source. Supply voltage waveform, v_S in Figure 1, is composed of fundamental harmonic of rms 230 V/50 Hz and of two higher harmonics: rms 32 V/250 Hz and rms 32 V/350 Hz. Internal resistance and inductance of the supply voltage source is 2 mΩ and 100 μH, respectively.

(2) UPQC's shunt converter. Energy phenomena related to DC-link capacitor are essential for obtaining the UPQC reference signal. The capacity of UPQC's DC-link capacitor C_{dc} is rated with respect to the maximal magnitude P_{Lmax} of the load active power and the C_{dc} capacitor maximal-to-minimal voltage ratio (compare Equation (7)). Thus, on the base of Equation (5) the needed capacity can be estimated as $C_{dc} = 2P_{Lmax}/({V_{C0}}^2 - {v_{dcT1}}^2)$. Finally, the initial voltage V_{C0} of 600 V and the C_{dc} capacity of 8 mF were used. A band-bang regulator operating with ΔI loop equal to 1 A has been used to force the reference current (Equation (6)). The inductance of shunt converter series inductor is set to 5 mH in order to limit the converter's switching frequency to about 40 kHz. Switching elements of the converter are modeled to work similarly to IGBT transistors.

(3) UPQC's series converter. A hysteresis bang-bang regulator operating with ΔV equal to 5 V has been used to shape the load voltage waveforms near its reference signal: The fundamental harmonic component of source voltage. The inductance and capacity of the series converter's LC(R) smoothing filter are designed so that the switching frequency of the serial converter is about 15 kHz.

(4) Switching elements of the shunt converter are modeled in such a way that they work similarly to IGBT transistors.

(5) A high-pass passive LC(R) filter has been added in parallel to the UPQC's shunt converter in order to diminish flow of high-frequency component of the compensating current into the supply source branch.

3.1. Basic Examination of the Control Method. Turning UPQC and Load On and Off

Achieving the steady state after turning the UPQC or load on and off is considered in this Subsection. Analyses of selected signals of the network after switching the load on and off gives information on correctness of source-and-load energy balancing performed by UPQC. This energy balancing is crucial for the studied UPQC control method.

For all analyses carried out in this subsection the load is a thyristor power controller. It is composed of a 10 Ω resistor in series with two thyristors in antiparallel connection. Both thyristors are fired symmetrically with phase angle of $\pi/2$. This load brings in abrupt load power changes and wide harmonic spectrum for load current that can be difficult to compensate by SAPF and UPQC devices.

3.1.1. Turning UPQC's Shunt Converter On

Since the shunt converter controls the source current it is also responsible for the total power delivered to the whole UPQC-and-load network. In particular, it controls also the source current component that is related to energy dissipated in all UPQC's circuitry. For this reason the shunt converter should be turned on no later than the series one. The process of turning the shunt converter on is shown in Figures 2 and 3, and then characterized with the use of basic electrical load and UPQC parameters collected in Tables 1 and 2.

In Figure 2 source voltage $v_S(t)$, source current $i_S(t)$ and the conductance signal $G(T_n)$—According to Equation (5), are shown as waveforms 1, 2 and 3, respectively. Before the time instant t = 400 ms the source-and-load circuit acts in the steady state. The UPQC is inactive yet and does not impact the source-load energy transmission. Then the shunt converter is turned on at instant t = 400 ms. Until this moment the DC-link capacitor voltage is of its initial magnitude V_{C0}, so the conductance signal (Equation (6)) is null. For that reason for the whole period T starting at this moment the load is powered using energy stored in UPQC reactance elements, practically solely from its DC-link capacitor. Therefore the source current is practically null. At the end of this period T, i.e., at t = 420 ms, the load equivalent conductance related to this period can be calculated and then used to produce the reference signal (Equation (6)) for the next period T, i.e., for time period 420 ms–440 ms.

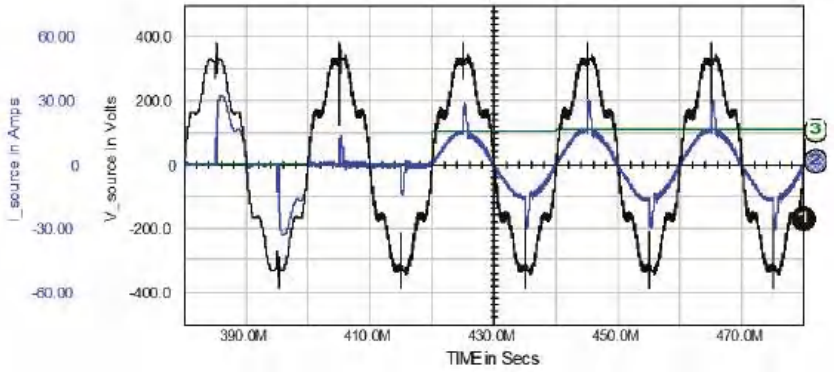

Figure 2. Shunt converter turning on. Source voltage: run 1, source current: 2, conductance signal: 3. Y scale for conductance signal is 45 mS/div.

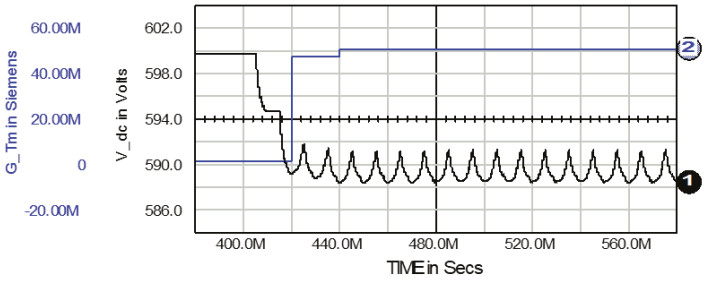

Figure 3. Shunt converter turning on process. DC-link capacitor voltage: waveform 1, and load equivalent conductance signal: waveform 2.

Table 1. Compensated load basic electrical parameters just before (for 380 ms–400 ms) and after (for 400 ms–460 ms) the instant (at 400 ms) of turning the shunt converter on.

Time (ms) / **Parameter**	**380–400**	**400–420**	**420–440**	**440–460**
V_{Load} (V)	229	234	234	234
I_{Load} (A)	15.6	16.6	17.0	17.0
S_{Load} (VA)	3572	3884	3978	3978
P_{Load} (W)	2439	2743	2885	2879
PF_{Load}	0.68	0.71	0.73	0.73
W_{Load} (J)	48.8	54.9	57.7	57.6
G_{Load} (mS)	46.6	50.1	52.7	52.6

V_{Load} and I_{Load} are voltage and current rms on load terminals, S_{Load} and P_{Load} are load apparent and active powers, PF_{Load} is load power factor, W_{Load} is energy consumed by load, G_{Load} is load equivalent conductance equal to $P_{Load}/(V_{Load})^2$.

Table 2. UPQC-and-load subcircuit basic electrical parameters before (380 ms–400 ms) and after (400 ms–460 ms) the instant (at 400 ms) of turning the shunt converter on.

Time (ms) / **Parameter**	**380–400**	**400–420**	**420–440**	**440–460**
V_{Source} (V)	232	232	232	232
I_{Source} (A)	15.5	2.8	12.1	12.9
I_{Source} THD (%)	59	146	17	14
$S_{UPQC+Load}$ (VA)	596	650	2807	2993
$P_{UPQC+Load}$ (W)	449	277	2717	2899
$PF_{UPQC+Load}$	0.68	0.42	0.97	0.97
$W_{UPQC+Load}$ (J)	49.0	5.5	54.3	58.0
ΔW_{DCCap} (J)	0.0	−49.5	−4.2	0.0
G_{Signal} (mS)	1.2	1.2	42.3	59.0

V_{Source} and I_{Source} are voltage and current rms on UPQC terminals, I_{Source} THD is source current THD factor, $S_{UPQC+Load}$ and $P_{UPQC+Load}$ are UPQC-and-load apparent and active powers seen on UPQC terminals, $PF_{UPQC+Load}$ is UPQC-and-load subcircuit power factor, $W_{UPQC+Load}$ is energy delivered to UPQC-and-load subcircuit from source, ΔW_{DCCap} is change of energy stored in DC-link capacitor, G_{Signal} is signal of load equivalent conductance calculated accordingly to Equation (5).

The whole "static" change of the capacitor voltage takes place in two steps: the first step from 599.7 V (sample taken at time t = 400 ms), down to 589.3 V (sample taken at t = 420 ms) and then the

second step from 589.3 V for sample taken at t = 420 ms down to 588.4 V at t = 440 ms. There are two main reasons of this two-step process of energy balancing:

- the first reason is due to intentional increasing the T_{st} parameter, see Equation (5). Setting this parameter to be longer then the period T introduces some inertia to the UPQC response on a change of source voltage or load power, making the UPQC action more stable. Here T_{st} has been fixed as increased by 2.2% with respect to the period T = 20 ms.
- the second reason is that energy stored only in the DC-link capacitor has been taking into account when calculating the conductance signal. In such case a comparatively small amount of non-considered energy, which is stored in other UPQC's reactance elements, affects the conductance signal making it a little oscillating. This effect can be neglected because of possible load power changes for time-variable loads as well as possible random variations in source voltage.

Finally, after the two-step updating of the conductance signal magnitude the whole network achieves the steady state.

There are basic electrical parameters characterizing load and UPQC action, related to waveforms shown in Figures 2 and 3, collected in Tables 1 and 2. They characterize the load and source work, respectively.

The load work is buffered through the UPQC. Therefore, variations in load action are "seen modified" from the perspective of the supply source. In particular, there are two major changes, which are seen from this perspective, that occur in whole load-and-UPQC circuitry action at t = 400 ms and then 20 ms later. These changes are related to the periodical updating of the conductance signal, see Equation (5) and comments to Figures 2 and 3.

It is noteworthy, that there is no difference in UPQC operation if the order of turning on the load and UPQC is reversed, that is, when UPQC is already active at the moment when the load begins its work. Similarly, at this moment the DC-link capacitor voltage equals its initial magnitude and the going magnitude of the conductance signal is zero. Consequently, the energy flow is buffered by UPQC with all consequences on UPQC action already described above.

3.1.2. Turning UPQC's Series Converter On

The series converter starts its action at t = 800 ms (Figure 4), when the network operates in the steady state and the shunt converter is already active. Since for the control method considered no time is needed for analysis of source voltage spectrum its distortion can be compensated immediately. This compensation cause change in harmonic components of DC-link capacitor voltage, waveform 2 in Figure 4. Although compensation for harmonics does not require the use of active power an increase of mean magnitude of the capacitor voltage can be observed. This is due to change of load active power being result of elimination of higher harmonics power from the total active power of the load.

Change in mean value of capacitor voltage causes change in magnitude of conductance signal (Equation (5)). Therefore, appropriate change of source current amplitude can be also observed. Changes of source-UPQC-load system parameters, related to Figures 4 and 5, are collected in Tables 3 and 4.

Just after turning the series converter on, at t = 800 ms, there is a drop of load active power resulting from eliminating load voltage distortion. As a consequence a part of source current turns out to be "excessive" with respect to going load and UPQC energy demand. Energy of this excessive current is stored in the DC-link capacitor increasing its voltage/energy. Therefore, on the base of Equation (5) the conductance signal is recalculated to a new magnitude at the beginning of the next T period. From this instant, i.e., for t = 820 ms, possibly delayed by the corrections described in the commentary next to Figure 2, the whole network reaches a new steady state.

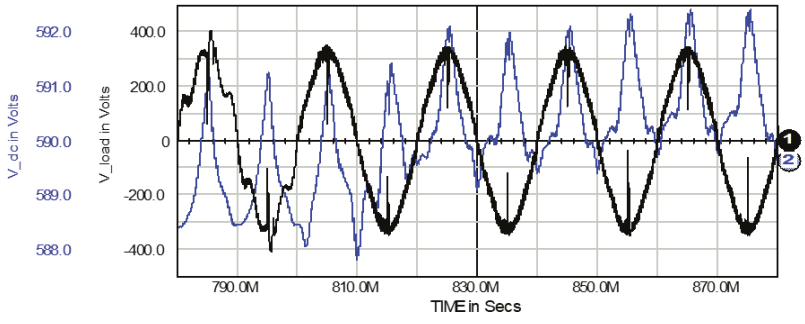

Figure 4. Series converter turning on. Load voltage: waveform 1, and DC-link capacitor voltage: waveform 2.

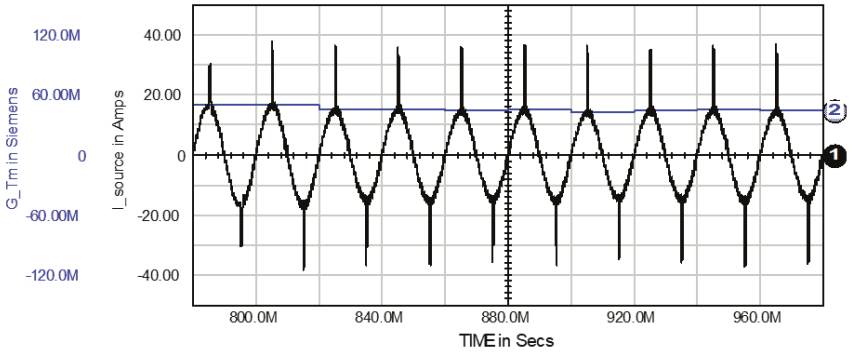

Figure 5. Series converter turning on process. Source current: waveform 1, and conductance signal: waveform 2.

Table 3. Basic parameters describing load action before (780 ms–800 ms) and after (800 ms–860 ms) the instant (800 ms) of turning the series converter on.

Time (ms) / Parameter	780–800	800–820	820–840	840–860
V_{Load} (V)	234	229	229	229
V_{Load} THD (%)	15	3.3	3.1	3.5
I_{Load} (A)	16.9	16.1	16.1	16.0
S_{Load} (VA)	3955	3687	3686	3664
P_{Load} (W)	2873	2589	2608	2563
PF_{Load}	0.73	0.86	0.71	0.70
W_{Load} (J)	57.5	51.8	52.2	51.3
G_{Load} (mS)	52.4	49.5	49.9	49.0

V_{Load} THD [%] is load voltage THD factor and other parameters are defined as for Table 1.

Table 4. Basic parameters describing load action before, (780 ms–800 ms) and after (800 ms–860 ms) the instant (800 ms) of turning the series converter on. All parameters are defined as for Table 2.

Time (ms) / Parameter	780–800	800–820	820–840	840–860
V_{Source} (V)	232	232	232	232
I_{Source} (A)	12.9	13.1	12.0	12.1
I_{Source} THD (%)	14	13	14	14
$S_{UPQC+Load}$ (VA)	2993	3039	2784	2807
$P_{UPQC+Load}$ (W)	2908	2919	2659	2692
$PF_{UPQC+Load}$	0.97	0.96	0.96	0.96
$W_{UPQC+Load}$ (J)	58.2	58.4	53.2	53.8
ΔW_{DCCap} (J)	0.5	5.2	−0.9	1.9
G_{Signal} (mS)	51.0	50.8	45.8	46.3

3.1.3. Turning the Load Off

Before the load is turned off the whole network operates in the steady state. Then, at the moment t = 1400 s, the load is turned off (Figure 6).

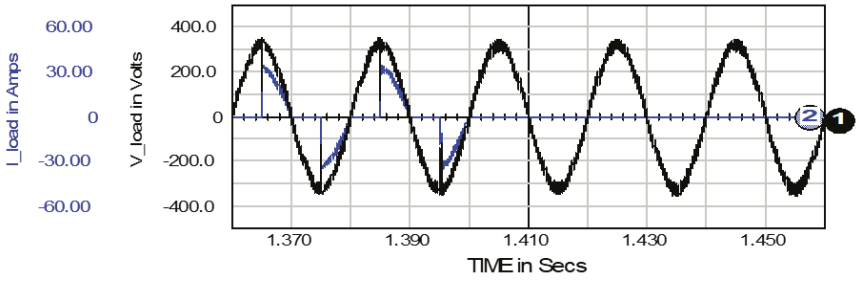

Figure 6. Load turning off process. Load voltage: waveform 1, and load current: waveform 2.

Just after the load turning off moment the load current stops immediately. However, because of the energy flow buffering the flow of source current has been extended for the next period T, i.e., for the time 1400 s–1420 s (Figures 7 and 8). As the result the whole circuit achieves zero steady state, i.e., with no load current/power, and UPQC is ready to the next compensation if load is turned on again.

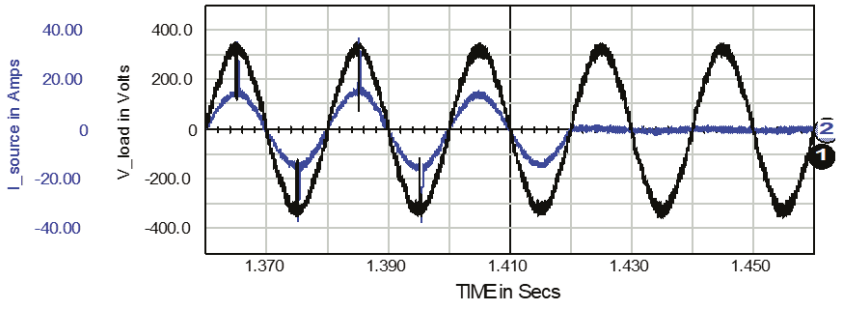

Figure 7. Load turning off process. Load voltage: waveform 1, and source current: waveform 2.

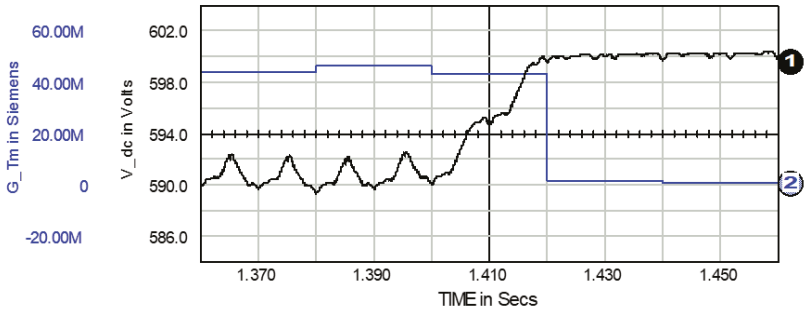

Figure 8. Load turning off process. DC-link capacitor voltage: waveform 1, and load conductance signal: waveform 2.

3.2. Compensation for Source Voltage and Current Distortions

Beside compensation for voltage deformation from higher harmonics the UPQC should maintain sinusoidal load voltage even if source voltage is influenced by irregular or unexpected distortions. Source voltage swells and sags, flicker, and pulse-type distortions can be enumerated in this context.

In Section 3.2. the load consists of two branches in parallel. The first one contains a thyristor power controller, consists of a 15 Ω resistor in series with two thyristors in antiparallel connection operating with phase angle equal to $\pi/4$. The second one consists of 15 Ω resistor in series with 32 mH inductor. This load branch introduces reactive power into the network.

3.2.1. Compensation for Source Voltage Swell

The source voltage is composed initially of fundamental frequency component of rms 230 V and also of two harmonics: 32 V/250 Hz and 32 V/350 Hz. Then, beginning from t = 120 ms there is a swell of the source voltage fundamental component by 50%. The most important waveforms and electrical quantities are shown in Figures 9–11, and then in Tables 5 and 6.

The load operates in the steady state when at instant t = 80 ms UPQC's shunt and series converters are activated simultaneously. For the first period T of UPQC operation, i.e., for time period 80 ms–100 ms, the load is powered practically solely with the use of energy stored in the DC-link capacitor, i.e., without drawing energy from the supply source. This cause decrease of DC-link capacitor voltage. Then, the first non-zero magnitude of conductance signal (Equation (5)) can be obtained at the very end of this time period, i.e., at instant t = 100 ms, waveform 3 in Figure 10.

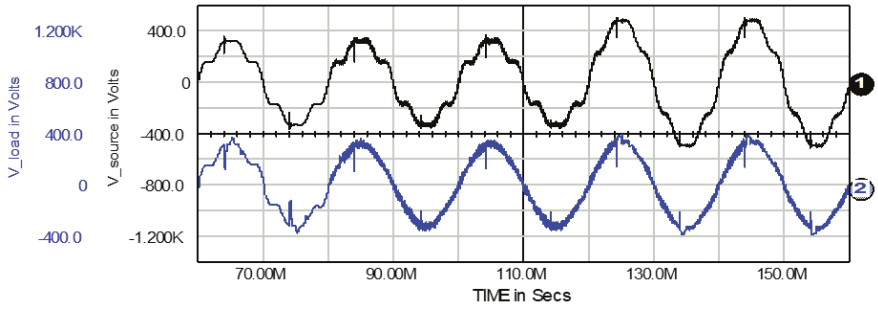

Figure 9. Source voltage swell compensation. Source voltage: waveform 1, and load voltage: waveform 2.

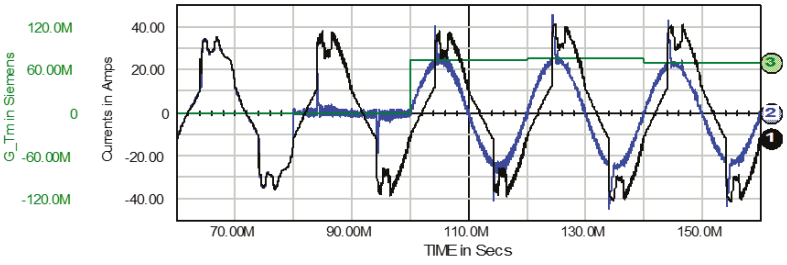

Figure 10. Source voltage swell. Load current, source current and conductance signal: waveforms 1, 2 and 3.

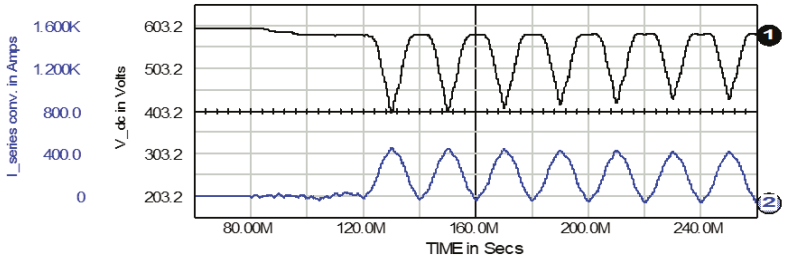

Figure 11. Source voltage swell. DC-link capacitor voltage and series converter current: waveforms 1 and 2.

Table 5. Basic parameters characterizing load work before and during source voltage swell. The parameter definitions are the same as for Table 3.

Time (ms) / Parameter	0–80	80–100	100–120	120–140	180–200	240–260
V_{Load} (V)	225	229	228	247	248	247
I_{Load} (A)	22.3	22.4	22.3	24.6	24.6	24.8
S_{Load} (VA)	5018	5130	5084	6076	6101	6126
P_{Load} (W)	4203	4278	4241	5145	5147	5214
PF_{Load}	0.84	0.83	0.83	0.85	0.84	0.85
W_{Load} (J)	84.0	85.6	84.8	102.9	102.9	104.3
G_{Load} (mS)	83.0	81.6	81.6	84.3	83.7	85.5

Table 6. Basic parameters characterizing UPQC-and-load subcircuit operation for the voltage swell. The parameter describing is the same as for Table 2.

Time (ms) / Parameter	60–80	80–100	100–120	120–140	180–200	240–260
V_{Source} (V)	231	232	232	346	346	346
I_{Source} (A)	22.2	2.6	18.2	19.0	17.7	17.7
$S_{UPQC+Load}$ (VA)	5128	603	4222	6574	6124	6124
$P_{UPQC+Load}$ (W)	4210	254	4146	6458	6014	6009
$PF_{UPQC+Load}$	0.82	0.42	0.98	0.98	0.98	0.98
$W_{UPQC+Load}$ (J)	84.2	5.1	82.9	129.2	120.3	120.2
ΔW_{DCCap} (J)	−1.0	−81.8	−2.8	7.0	−0.5	0.0
G_{Signal} (mS)	0.2	0.3	74.4	76.8	71.1	71.4

At t = 120 ms the amplitude of source voltage fundamental component rises from 325 V up to 487 V, Figure 9. Since for the control method considered there is no time needed for analysis of source voltage spectrum this source voltage increase can be compensated immediately. The load voltage amplitude rises, but only to 349 V, Figure 9 and Table 5.

In order to compensate for this voltage increase a voltage correction is generated using energy stored in the DC-link capacitor. Depending on the voltage swell magnitude the current of the converter side of the series converter can reach significant values. This can result in significant increase of energy loss in this converter (Figure 11) and compare P_{Load} and $P_{UPQC+Load}$ in Tables 5 and 6.

3.2.2. Compensation for Source Voltage Sag

The load operates in the steady state when the UPQC is turning on at t = 80 ms. At t = 120 ms the amplitude of source voltage fundamental frequency component decreases to 163 V. Due to the UPQC action the load voltage can be maintained on the amplitude about 295 V, Table 7 and Figure 12.

Table 7. Basic parameters characterizing load work before and during source voltage sag. The parameter describing is the same as for Table 3.

Time (ms) / Parameter	60–80	80–100	100–120	120–140	200–220	380–400
V_{Load} (V)	225	229	228	214	209	208
I_{Load} (A)	22.3	22.4	22.3	20.9	20.7	20.2
S_{Load} (VA)	5018	5130	5084	4473	4326	4121
P_{Load} (W)	4203	4278	4241	3735	3653	3487
PF_{Load}	0.84	0.83	0.83	0.84	0.84	0.85
W_{Load} (J)	84.1	85.6	84.8	74.7	73.1	69.7
G_{Load} (mS)	83.0	81.6	81.6	81.6	83.6	83.4

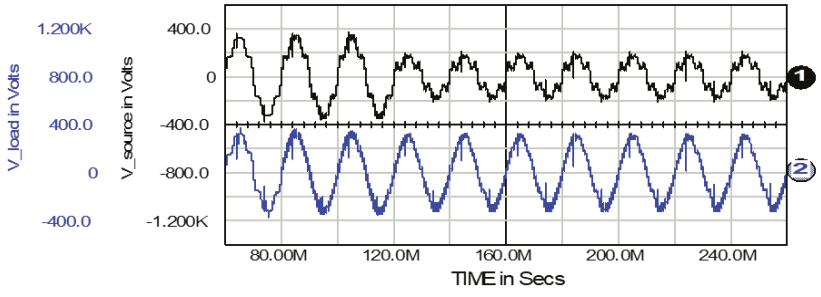

Figure 12. Source voltage sag compensation. Source voltage: waveform 1 and load voltage: waveform 2.

The source voltage drop is compensated with the use of energy drown from the supply source. This is performed as follows. The deficiency of source energy, caused by voltage sag, is balanced using of energy stored in the DC-link capacitor. As the result its voltage decreases. It causes an increase in the conductance signal (Equation (5)) and an increase in amplitude of the source current reference (Equation (6)). Source current rises increasing source active power (Figure 13). This "additional" source power is utilized to increase load voltage to be near its nominal magnitude.

Similarly to the case of voltage swell the compensation for voltage sag may require large current of the series converter. This imply a high magnitude of variable component of the DC-link capacitor voltage. If the instantaneous capacitor voltage falls close to the source instantaneous voltage, then UPQC

may lose the possibility of correct operation. Therefore it can be said that in the analyzed case UPQC operates at the limit of its capabilities. This is illustrated in Figure 14, waveform 1.

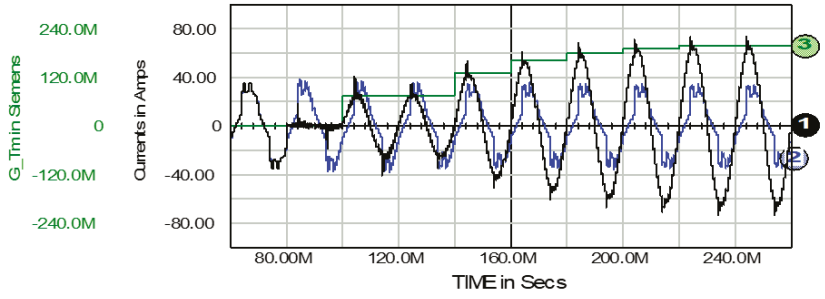

Figure 13. Source voltage sag compensation. Source current: waveform 1, load current: waveform 2, and conductance signal: waveform 3.

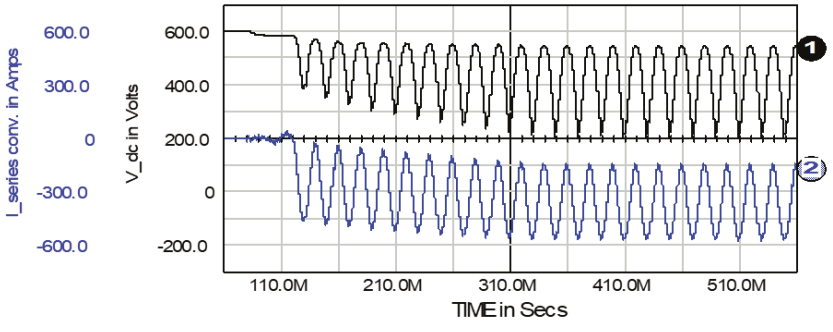

Figure 14. Source voltage sag compensation. DC-link capacitor voltage and load series converter current: waveform 1 and 2, respectively.

It should be also noticed a problem of energetic cost of compensation for the source voltage sag. During compensation high current of the series converter causes a large dissipation of energy in its power circuitry. Such power loss can be estimated on the basis of a comparison of the active power at the load terminals against the active power at the UPQC's input terminals: compare the parameter P_{load} in Table 7 with the parameter $P_{UPQC+Load}$ in Table 8.

Table 8. Basic parameters describing UPQC-and-load subcircuit action before and during the source voltage sag. The parameters shown were defined in Table 2.

Time (ms) / **Parameter**	**60–80**	**80–100**	**100–120**	**120–140**	**140–160**	**200–220**	**280–300**	**380–400**
V_{Source} (V)	231	232	232	120	120	120	120	120
I_{Source} (A)	22.2	2.6	18.2	18.1	30.3	44.7	46.5	46.6
$S_{UPQC+Load}$ (VA)	5128	603	4222	2172	3636	5364	5580	5592
$P_{UPQC+Load}$ (W)	4210	254	4146	2086	3492	5123	5364	5369
$PF_{UPQC+Load}$	0.82	0.42	0.98	0.96	0.96	0.96	0.96	0.96
$W_{UPQC+Load}$ (J)	84.2	5.1	82.9	41.7	69.8	102.5	107.3	107.4
ΔW_{DCCap} (J)	−0.48	−82.8	−2.3	−57.6	−33.0	−7.1	−10.5	−0.4
G_{Signal} (mS)	0.2	0.3	74.4	76.8	129.6	192.6	200.0	200.0

3.2.3. Compensation for Source Voltage Fluctuations

Compensation for source voltage fluctuations within the range of magnitude of 0.9 to 1.1 of its nominal value and at frequency of 8 Hz is considered in this section. Such voltage fluctuation may be classified as flicker. Flickers cause a number of adverse effects in electrical circuits operation, for example for electric motors action electronic devices operation or lighting installations.

For the discussed UPQC control method, the way and effect of reducing flicker-type of source voltage fluctuations is identical with the method of compensating for source voltage swells and sags. In addition, because of smaller disturbances in source voltage amplitude they are easier for compensation. However, the flicker-type voltage oscillations can be considered as repetitive run in a narrow range of low frequencies. Therefore, it seems to be convenient to present here a distinctive way of the UPQC action which can be useful for such periodical-like voltage or current disturbances. In particular, the option of choosing a convenient value for the T_{st} parameter, see Equations (1) and (5), is utilized here. This possibility has been used to increase the inertia in UPQC operation against changes in load active power. Voltage fluctuations cause changes in this power. In general, the greater the magnitude of the T_{st} parameter the closer the conductance signal (Equation (5)) run with respect to its multi-period mean. As a result the source current (and load voltage) can be stabilized, so that flicker is easier to be reduced in the whole grid.

It should be noted, that if increase the T_{st} time the DC-link capacitor operates with lowered voltage. For this reason the condition (Equation (7)) may not be met. This can reduce UPQC dynamics or even cause UPQC operation to failure.

The UPQC operation when the time T_{st} is set to be equal to the source voltage period T, and then when it has been increased to $3T$ is analyzed. The conductance signal (Equation (5)) and DC-link capacitor voltage are shown in the same scale in Figure 15, respectively. It can be observed that for the T_{st} parameter increased to $3T$ fluctuation of conductance signal is reduced: Waveform 3 in contrast with waveform 1. Simultaneously the UPQC operates with lowered DC-link capacitor voltage: waveform 4 with respect to waveform 2.

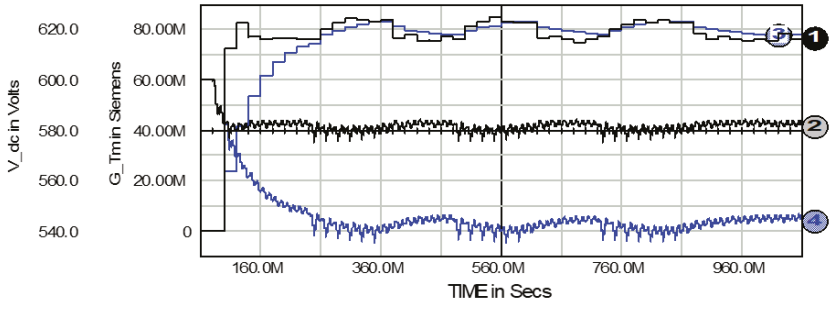

Figure 15. Source voltage flicker compensation. DC-link capacitor voltage for $T_{st} = T$ and for $T_{st} = 3T$: waveforms 2 and 4, respectively, and conductance signal for $T_{st} = T$ and for $T_{st} = 3T$: waveforms 1 and 3, respectively.

The effect of flicker (and still existing harmonics) compensation for $T_{st} = 3T$ is shown in Figure 16. The compensation can be considered sufficient. Taking into account that the load voltage amplitude is maintained to be constant, it can be concluded that the flicker compensation is sufficient.

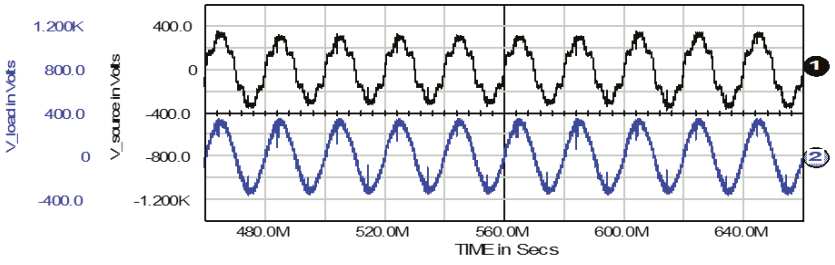

Figure 16. Source voltage flicker compensation. Source voltage: waveform 1, and harmonics-compensated and amplitude-levelled load voltage: waveform 2.

4. Studies for UPQC Extended Operation

The extended functionality of UPQC is understood here as the possibility of using it also to control the energy exchange between all—Being influenced by given UPQC device action—Elements of the network. These elements may be of passive or active type or may be changeable from this point of view. There is no restriction on location in the network of these elements. They may be covered by UPQC extended action as well being located on the AC-side as on the DC-side of UPQC device. Therefore, beside compensating for undesirable components of grid voltage and current runs the UPQC can also serve as a local energy distribution center that can operate with high power factor. There is no change in UPQC circuitry parameters and in source voltage waveform components with respect to those introduced in Section 3. However, in order to highlight UPQC's extended capabilities the load is composed to be nonlinear, time variable and of changeable passive or active kind.

4.1. UPQC Operation with Switched Passive/Active Work of AC-Side Load Elements

In general, there are two main possibilities of energy flow management when some nominally passive elements of load become generators and the amount of energy being generated in the load exceeds energy being consumed there:

(a) the "excessive" amount of energy is transmitted up stream to the supply source or
(b) the "excessive" amount of energy is stored in the DC-link capacitor.

The case (a) may be realized in a full form, when all amount of the "excessive" energy is transmitted up stream to the source, or in a partial form, when some portion of the "excessive" energy is accumulated in the DC-link capacitor. Waveforms related to the (a) strategy are shown in a general outlook in Figures 17–19, and then, in more precise look and with detailed comments, are presented in Figures 20–22. Then, waveforms related to the (b) strategy are shown in general outlook in Figures 23 and 24, and then are detailed in Figures 25–29.

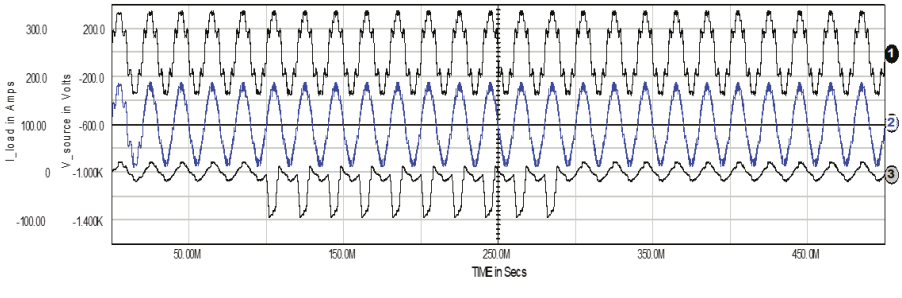

Figure 17. Source voltage: waveform 1, load voltage: waveform 2 and load current: waveform 3. Whole network action, general view.

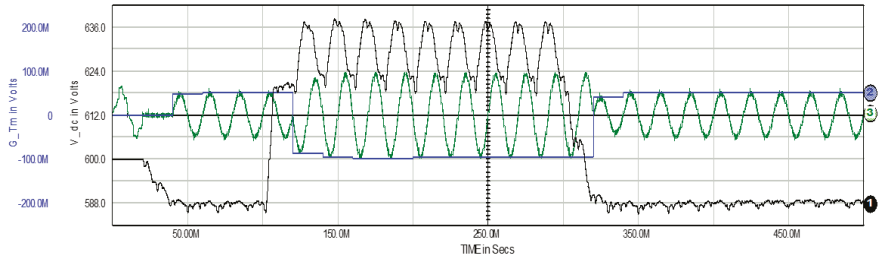

Figure 18. DC-link capacitor voltage: waveform 1, conductance signal: waveform 2 and source current: waveform 3 with Y scale of 54 mS/div. Whole network action, case 4.1 (a).

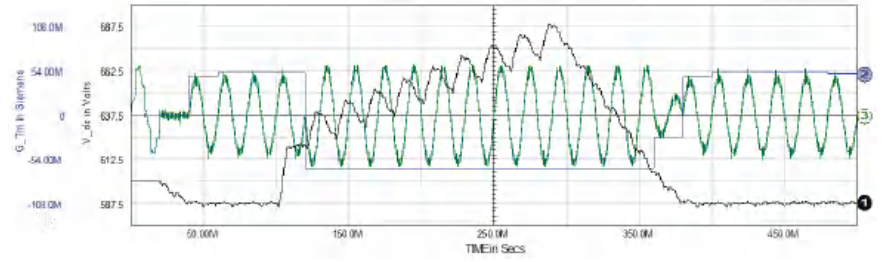

Figure 19. DC-link capacitor voltage: waveform 1, conductance signal: waveform 2 and source current: waveform 3 with Y scale of 10 A/div. Whole network action, case 4.1 (b).

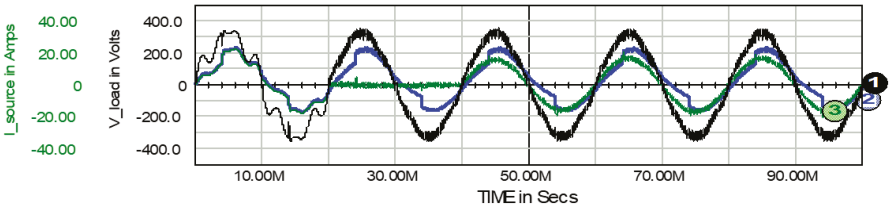

Figure 20. Load voltage: waveform 1, load current: waveform 2 and source current: waveform 3.

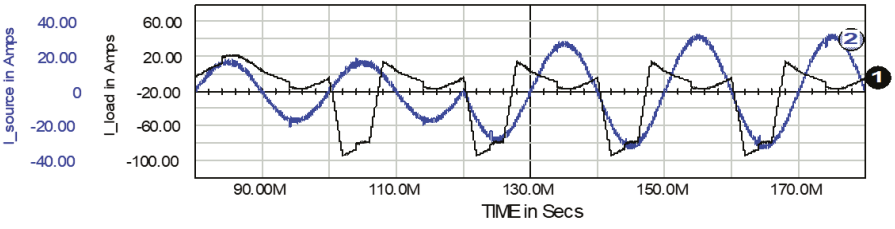

Figure 21. Load current: waveform 1 and source current: waveform 2.

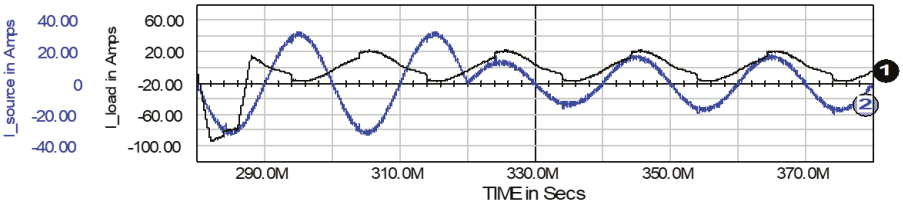

Figure 22. Load current: waveform 1 and source current: waveform 2.

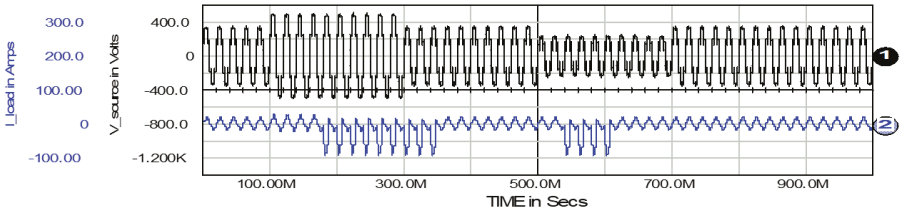

Figure 23. Source voltage: waveform 1 and load current: waveform 2.

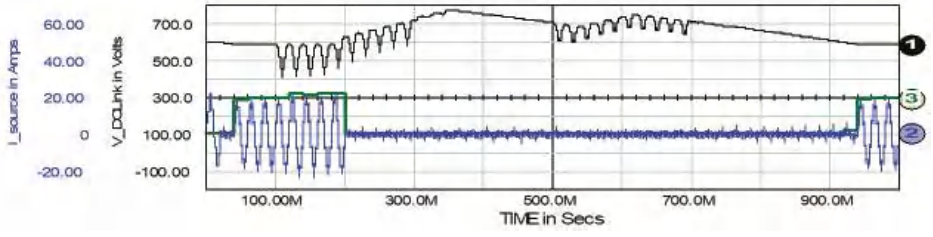

Figure 24. DC-link capacitor voltage: waveform 1, source current: 2 and conductance signal: 3 with Y scale of 27 mS/div.

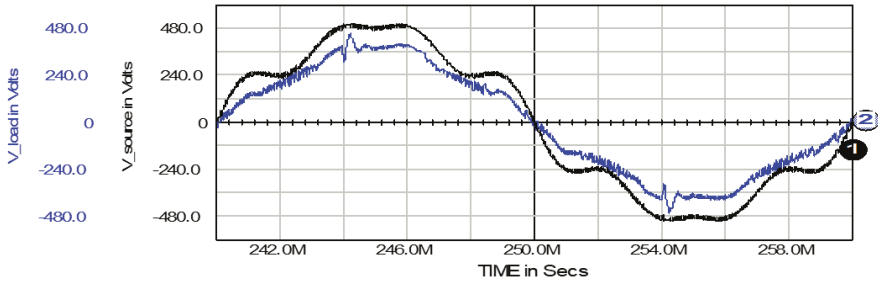

Figure 25. Source and load voltages: waveform 1 and 2. Theirs RMS and THD parameters are 348 V and 14.7%, and then 268 V and 7.7%, respectively.

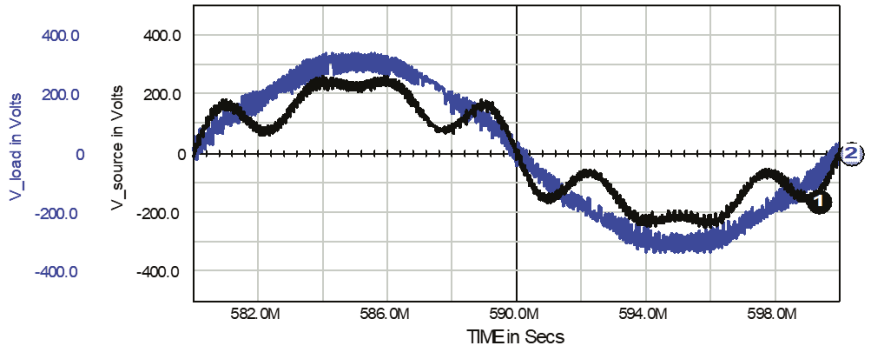

Figure 26. Source and load voltages: waveform 1 and 2. Theirs RMS and THD parameters are 162 V and 32.7%, and then 219 V and 4.1%, respectively.

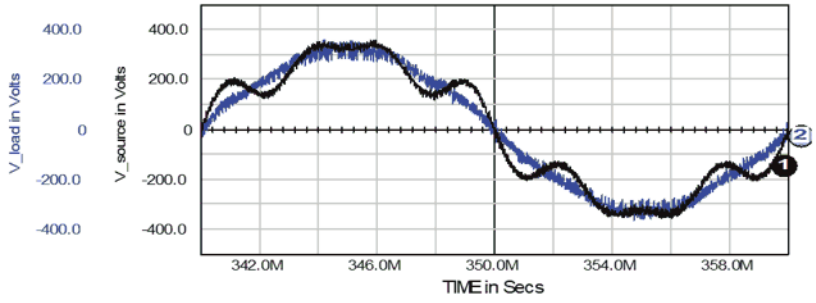

Figure 27. Source and load voltages: waveform 1 and 2. Theirs RMS and THD parameters are 235 V and 21.4%, and then 231 V and 4.3%, respectively.

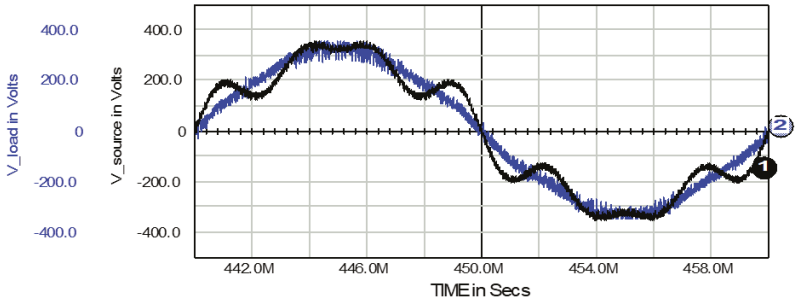

Figure 28. Source and load voltages: waveform 1 and 2. Theirs RMS and THD parameters are 235 V and 21.7%, and then 231 V and 4.7%, respectively.

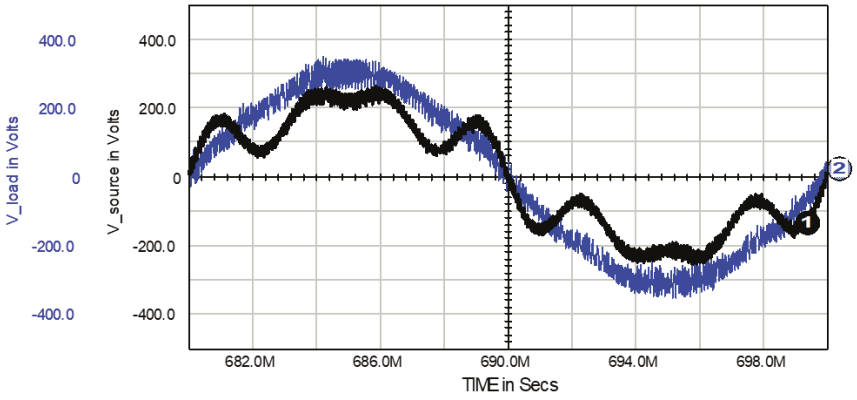

Figure 29. Source and load voltages: waveform 1 and 2. Theirs RMS and THD parameters are 162 V and 32.6%, and then 219 V and 4.2%, respectively.

Figure 20 shows load voltage and current, and then source current during the first 100 ms of whole network action. This time period corresponds with the same time interval in Figures 17–19, and then in Figures 23 and 24.

The waveform 2 in Figure 20 is formed to represent total current of several loads, where some of them are nonlinear and time variable. The current is highly distorted, having also an inductive and DC components. Initially, in the time period T of 0 ms–20 ms the load active and apparent powers are

2.8 kW and 3.0 kVA, respectively, and 2.7 kW and 2.9 kVA during time period T of 20 ms–40 ms when UPQC starts its action.

Then, during the time interval 100 ms–300 ms, a new load-sided element was activated and therefore the load current run changes, see waveform 1 in Figure 21 (and waveform 3 in Figure 17). The load current is now composed to be almost unrealistically strongly distorted in order to show high and extended performance of UPQC. In particular a relatively large negative constant component of 17–28 A appears in the load current spectrum, so the fundamental frequency component is inverted relative to the fundamental component of the source voltage. Thus, the load, taken as a whole, works now as a source of energy. Because the in-load generated power exceeds both the power consumed in the load and dissipated in the UPQC the instantaneous DC-link capacitor voltage rises above its initial magnitude. As a result, the conductance signal changes its sign to negative, see waveform 3 in Figure 18. Consequently, the source current, still being purely active, begins to be controlled by the UPQC's shunt converter in order to carry some amount of the in-load generated power to the source, waveform 2 in Figure 21.

Estimation of energy balance in the network when it is practically in the steady state (here in the time period 200 ms–220 ms, when there is no change in the load power and in the static DC-link capacitor voltage, see Figures 17 and 18) is as follows: in-load generated power: 7.85 kW, in-load consumed power: 2.72 kV, power transmitted from the load to the source: 5.07 kW, power dissipated in UPQC's shunt converter: 43 W and power dissipated in UPQC's series converter: 226 W. From this energy balance results that the in-load generated power feeds passive elements of the compensated load and covers UPQC's energy loss. The remaining "excessive" amount of in-load generated power is transmitted to the source.

After switching off the in-load generating element the DC-link capacitor voltage diminishes below its initial magnitude. For this reason the conductance signal becomes positive, consequently source current polarity has been inverted and load draws energy from the source again. This is shown in Figures 18 and 22.

During the time period about 100 ms–350 ms the UPQC operates as a compensator as well as an energy distributor. Note, during this time load voltage and source current were maintained to be sinusoidal, irrespective of energy flow direction (Figures 17 and 18).

4.1.1. Split Storing/Distributing of the In-Load Generated Energy

As it was already stated the energy generated in the active part of load may be decomposed into the portion consumed immediately and into the "excessive" portion. In turn this "excessive" portion may be split into a piece to be transmitted immediately to the grid and a piece to be stored in the DC-link capacitor. In other words, a power limit may be imposed on energy transmission to the grid (or, if needed, a voltage limit may be imposed on maximal DC-link capacitor voltage).

Such possibility of limited back-transmission is illustrated in Figure 19. In this example the maximal back-transmission power is bounded to 2.7 kW. Because the in-load generated power is greater than the allowed power limit of the back-transmission the DC-link capacitor voltage (energy) rises. It lasts till the moment of switching-off the generating element that is located in the load. Then the "excessive" energy portion, which were stored in the capacitor, is discharging partially to the source and partially to UPQC—Being dissipated in its power circuitry. After achieving the balance between load and source active powers, what can be seen in Figure 19 about t = 380 ms, the source takes over powering the load.

4.1.2. Full Storing of the In-Load Generated Energy

Characteristic waveforms of currents and voltages for the case of the full energy-storing mode (without upstream energy transmission) are shown in general outlook in Figures 23 and 24, and then some critical time areas are zoomed in Figures 25–29.

The waveform 1 in Figure 24 demonstrates the process of accumulating/discharging the in-load generated "excessive" energy in the DC-link capacitor. The energy accumulation process takes place in time periods 180 ms–340 ms and then 540 ms–620 ms, whereas the energy discharging can be seen during time periods 340 ms–520 ms and 620 ms–940 ms. These time intervals fall within the wider 180 ms–940 ms range in which UPQC's shunt converter blocks any current flow to-or-from the supply source. In other words, during the time 180 ms–940 ms the load works in an energetically autonomous way, that means without any energy drawing from or giving to the supply source. Power fluctuations of all elements of the network are buffered by UPQC. Simultaneously all UPQC's conventional compensation tasks are fully fulfilled.

The most critical areas occurs about 200 ms–300 ms and then about 550 ms–600 ms. There is a cumulation of strong source voltage harmonics distortions with voltage swell and later with voltage sag. There are also large load current deformations, including high energy negative pulses that generates "asymmetrical" active power, occurring only during positive half-waves of source voltage.

The 240 ms–260 ms T period was chosen to show the effect of UPQC action (Figure 25).

For this period the RMS and THD parameters of source voltage run have been reduced at load terminals from the "swelled" magnitude of 348 V down to 268 V and from 14.7% to 7.7%, respectively. Unfortunately, it can be said that despite a significant improvement of load voltage parameters, the voltage quality requirements have not been met.

Within the second critical area the 580 ms–600 ms T period was chosen to show the effect of UPQC action (Figure 26). For this period the RMS and THD parameters of source voltage waveform have been improved at load terminals from the "sagged" magnitude of 162 V up to 219 V and from 32.7% down to 4.1%, respectively. It can be said that these parameters may be considered satisfactory.

The source and load voltages for non-critical areas are presented in next three figures. The 340 ms–360 ms, 440 ms–460 ms and 680 ms–700 ms T periods were chosen to show these waveforms in Figures 27–29, respectively. The load voltage RMS and THD parameters can be accepted as sufficient from the voltage quality point of view. In particular, there is no significant difference in the content of harmonics when working with or without compensation for source voltage sag.

4.1.3. A Side Effect of Conductance Signal Control Method: Alleviating and Catching Energy of Source Voltage Spike Distortion

From time to time an impulsive voltage transient (voltage spike) can appear in the grid, e.g., as a result of lighting stroke. Lighting arresters can be used to stop the transient. Fortunately, it follows from the principle of the considered control method that UPQC can alleviate, or even store and then utilize some amount of energy of such voltage distortion.

The network operates in the steady state when a voltage spike appears at t = 105 ms, Figure 30. Parameters characterizing this spike are 3.3 kV in magnitude, 1.2 μs rise time, 10 μs peak voltage duration and 200 μs fall time.

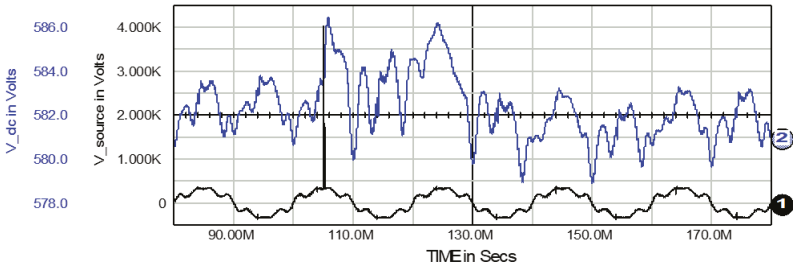

Figure 30. Source voltage with spike distortion: waveform 1 and DC-link capacitor voltage: waveform 2.

Energy of this source spike increases amount of energy, which flows through UPQC input terminals, from 89.9 J during the stead state T period 80 ms–100 ms, up to 141.6 J for the next (i.e., hit by the spike) 100 ms–120 ms T period. Some amount of energy of the spike impacts the load immediately, what can be seen as load voltage distortion shown in waveform 2 in Figure 31. As the result, the energy consumed by the load rises from 88.2 J for the 80 ms–100 ms time period up to 125.4 J for the next one. However, some portion of energy of the spike has been caught by UPQC. This energy portion increases energy stored in the DC-link capacitor: note the difference in capacitor voltage between instants t = 120 ms and t = 100 ms in waveform 2 in Figure 30.

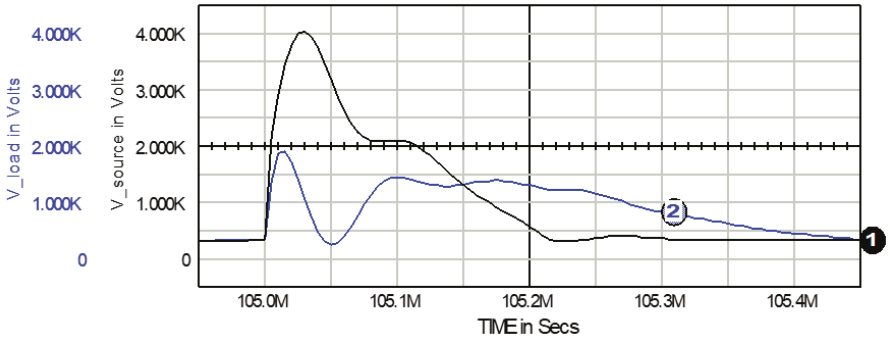

Figure 31. Source voltage: waveform 1 and load voltage: waveform 2.

Because UPQC buffers energy variations between the supply source and the load the energy of the pulse distortion, which reaches load terminals, is lower than the distortion of energy that appears on UPQC input terminals. This is 125.4 J with respect to 141.6 J, respectively. This energy difference increases electric charge stored in the DC-link capacitor and, at the same time, increases its static voltage from 581 V at t = 100 ms up to 584 V at t = 120 ms, waveform 2 in Figure 30. This "additional" voltage (or energy) decreases the conductance signal (Equation (1)) from 82.3 mS for T period 100 ms–120 ms down to 65.7 mS for the next T period 120 ms–140 ms, waveform 1 in Figure 32. This fall of conductance signal (Equation (1)) causes decreasing in source current amplitude from 26.6 A down to 21.3 A, waveform 2 in Figure 32 during the T period 120 ms–140 ms. In other words, during this T period UPQC uses the from-the-distortion energy to power both itself and the load.

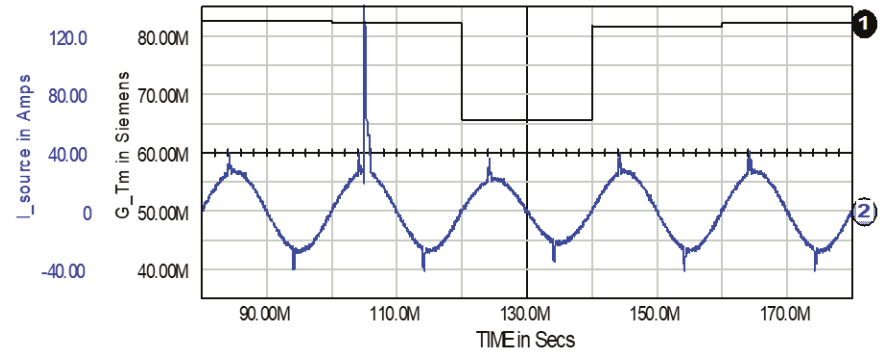

Figure 32. Conductance signal: waveform 1 and source current: waveform 2.

Just after the moment at which energy of the pulse distortion stored in the DC-link capacitor is discharged, the network returns to the steady state, waveform 2 in Figure 30 and both waveforms in Figure 32.

4.1.4. UPQC Operation During Switched Passive/Active Work of DC-Side Load

In order to extend the UPQC usefulness a load as well as a source of energy may be connected to the UPQC's DC-link capacitor. In such a case UPQC can perform some extra tasks. In particular, depending on direction of energy flow, UPQC can act as a high power factor rectifier, which can power DC-side loads with the use of AC-side generated energy, or as an inverter, which can supply AC-side loads with the use of energy generated by DC-side sources. Therefore, UPQC may also serve as an energy bridge and buffer that can control energy flow between all UPQC's AC-side and DC-side loads and sources. Figures 33 and 34 illustrate such extended mode of UPQC operation.

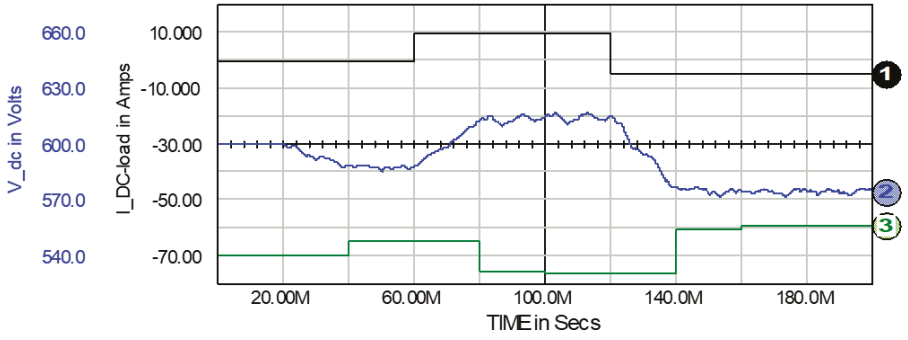

Figure 33. DC-side load current: waveform 1, DC-link capacitor voltage: waveform 2 and conductance signal: waveform 3 (Y scale for this signal is 25 mS/div).

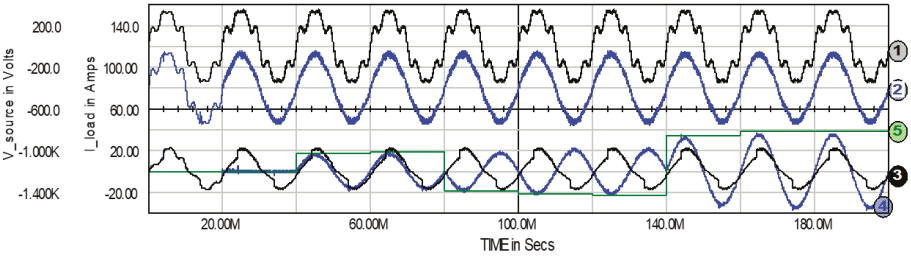

Figure 34. AC-side source voltage: waveform 1, AC-side load voltage: waveform 2, AC-side load current: waveform 3, AC-side source current: waveform 4 and conductance signal: waveform 5, where Y scale for the conductance signal is 57 mS/div.

In Figure 33 UPQC operates in the steady state when a DC-side current of 10 A magnitude begins to charge the DC-link capacitor at the moment t = 60 ms, waveform 1 in Figure 33. Due to the increase in DC-link capacitor voltage, the conductance signal changes both its magnitude and sign to be negative, waveform 3 in Figure 33 and waveform 5 in Figure 34.

As a result energy of this charging DC-side current is transferring to the AC-side network. This energy can power AC-side loads and, concurrently, its surplus may be transmitted upstream to the grid. This to-the-grid energy transferring process starts at t = 80 ms, waveform 4 in Figure 34.

Then, at time instant t = 120 ms, the DC-side current begins to discharge the DC-link capacitor. The conductance signal is recalculated into a new magnitude that depends on sum of AC-side and DC-side active powers. As a result the UPQC, still compensating for voltage and current disturbances, operates concurrently as a high power factor rectifier, i.e., a rectifier with sinusoidal input current, waveform 4 in Figure 34.

Figures 35–39 characterize the UPFC work for when voltage/current runs to be compensated are highly and variously distorted. An additional element, which can operate either as a load or a

source of energy and which power can vary in time both in magnitude and in sign, is connected on the DC-link capacitor. Such a network can be considered as generating a kind of worst case of voltage and current runs to be improved. Parameters of these voltage/current runs are specified in the comment that follows Figure 36.

The distorted AC-side source voltage and then the compensated AC-side load voltage are shown in Figure 35. The AC source voltage is distorted by the same higher harmonics and swell/sag disturbances compared to that shown in Figure 23, but this time the whole system is also influenced by energy consumption/generation by the DC-side circuitry. The current run of the DC-side load/source element is shown in Figure 36. Positive polarity of this current means that this element generates energy and vice versa.

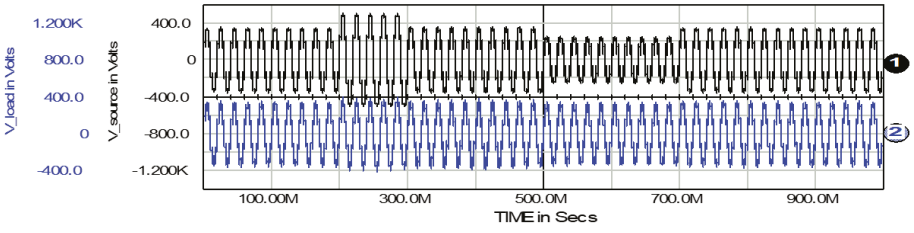

Figure 35. Global view on AC-side source voltage: waveform 1 and on AC-side load voltage: waveform 2.

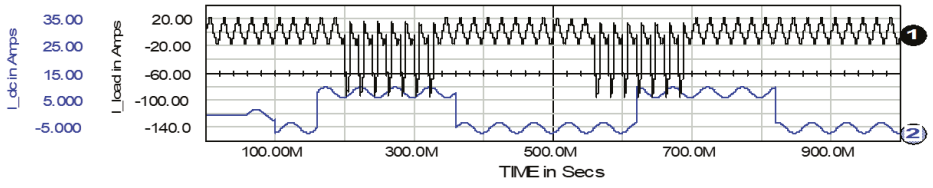

Figure 36. Global view on AC-side load current: waveform 1 and on DC-side load current: waveform 2.

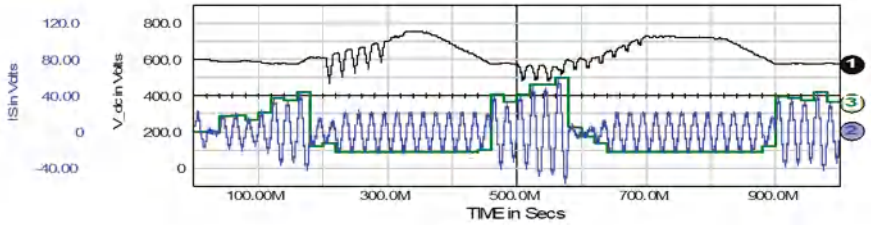

Figure 37. Global view on DC-link capacitor voltage: waveform 1, AC-side source current: waveform 2 and conductance signal: waveform 3 with Y scale of 56 mS/div.

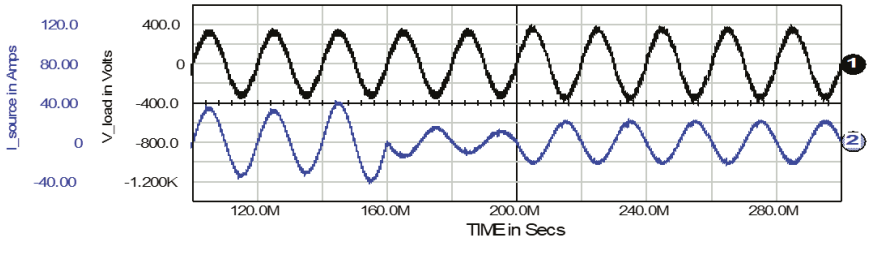

Figure 38. Critical time period 100 ms–300 ms. AC-load voltage: waveform 1 and AC-source current: waveform 2.

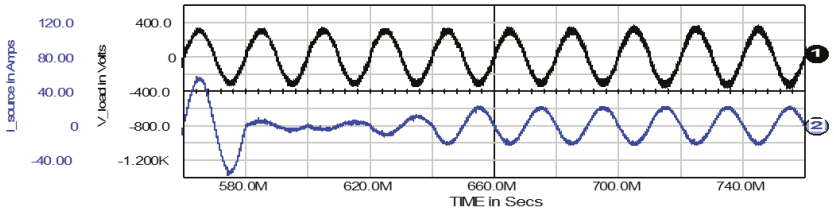

Figure 39. Critical time period 560 ms–760 ms. AC-load voltage: waveform 1 and AC-source current: waveform 2.

DC-link capacitor voltage, AC-side source current and conductance signal (shown as the envelope of source current) are presented in Figure 37. These signals are essential for discussing the UPQC extended operation. In particular, energy balancing between all sources and loads of the network as well as UPQC's "internal energy effort" in order to compensate for nonactive voltage and current components can be identified when analyzing the waveform of DC-link capacitor voltage. This voltage run contains the in-T-period oscillations that relate to compensation for nonactive components of AC-side current and voltage. In the same time the DC-link capacitor voltage increases or decreases statically, i.e., from T_n period to T_{n+1} one, when UPQC balances active powers of all loads and energy sources of the network.

The most critical conditions for UPQC action appear around 200 ms–300 ms and 500 ms–700 ms. They may be treated as a base for a general assessment of UPQC performance.

(a) The first critical time period 200 ms–300 ms: There exist a 50% increase in the amplitude of fundamental component of AC source voltage, a large harmonic deformation with heavy DC-component in AC-side load current and successive energy generation/consumption with variable power on UPQC's DC-side circuitry. The related UPQC's output runs, i.e., AC-side load voltage and AC-side source current, are shown in Figure 38. For the steady state of the grid waveforms, T period 220 ms–240 ms, parameters of UPQC's input and output runs are:

- source voltage RMS/THD of 348 V/14.5% have been transformed into load voltage 247 V/3.8%, respectively;
- load current THD of 82.3% and its DC component of magnitude −28.2 A have been transformed into source current THD and DC component of 1.9% and 0.0 A, respectively.

(b) The second critical time period 500 ms–700 ms. There is a 33% decrease in the amplitude source voltage fundamental component, other parameters are the same as in (a). The UPQC output signals are shown in Figure 39. For the steady state of grid runs within this region, T period 660 ms–680 ms, parameters of UPQC's input and output signals are as follows:

- source voltage RMS of 162 V and THD of 33.2% have been transformed into load voltage RMS and THD of 218 V and 4.6%, respectively;
- load current THD and DC component of 79.5% and −28.5 A has been transformed into source current THD and DC component of 2.6% and 0.1 A, respectively.

It can be stated that in both critical areas of the UPQC operation the disturbed input voltage and current runs have been compensated satisfactory.

5. Conclusions

The paper presents the possibility of compensation for nonactive voltage/current components with the use of compensators that are controlled using a conductance signal. In general, the conductance signal results from the active power of the compensated load. This signal can be calculated based on two variables to be measured:

(a) signal of load power—But obtained indirectly, by measuring energy stored in the reactive elements of the compensator;
(b) signal of supply voltage.

By using the conductance signal as the reference for the compensator action it is possible to omit the technically complicated methods of analysis of voltage/current waveforms by their decomposition into plurality of components. The same idea of avoiding the harmonic analysis is visible here if one compares the considered method to the p-q instantaneous power theory and its use to compensators control. Depending on planned purpose of compensation, such a solution may well be an advantage or a disadvantage.

The conductance signal is obtained based on observation of energy balance in the circuit consisting of the source, the UPQC compensator and the load. Any energy imbalance between the power required by the load and supplied by the source is buffered by the UPQC. In other words the network aims the steady state under control of the UPQC.

Using the conductance signal control method extends the functionality of UPQC. There is the possibility of controlling the flow of energy between all active and passive components of the network. This can help to increase the efficiency of the network.

The use of conductance signal in order to control the UPQC action enables bi-directional energy transmission with unity power factor both from the source to the load and in the opposite direction when the load can also generate energy. Both UPQC's AC- and DC-side generated or consumed energy may be handled and exchanged in such bi-directional way. This opens the possibility of using UPQC also as a local energy buffering-and-distribution center that can be useful for smart microgrids, increasing their energy efficiency.

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Effective Permeability of Multi Air Gap Ferrite Core 3-Phase Medium Frequency Transformer in Isolated DC-DC Converters

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Abstract: The magnetizing inductance of the medium frequency transformer (MFT) impacts the performance of the isolated dc-dc power converters. The ferrite material is considered for high power transformers but it requires an assembly of type "I" cores resulting in a multi air gap structure of the magnetic core. The authors claim that the multiple air gaps are randomly distributed and that the average air gap length is unpredictable at the industrial design stage. As a consequence, the required effective magnetic permeability and the magnetizing inductance are difficult to achieve within reasonable error margins. This article presents the measurements of the equivalent $B(H)$ and the equivalent magnetic permeability of two three-phase MFT prototypes. The measured equivalent $B(H)$ is used in an FEM simulation and compared against a no load test of a 100 kW isolated dc-dc converter showing a good fit within a 10% error. Further analysis leads to the demonstration that the equivalent magnetic permeability and the average air gap length are nonlinear functions of the number of air gaps. The proposed exponential scaling function enables rapid estimation of the magnetizing inductance based on the ferrite material datasheet only.

Keywords: average air gap length; dc-dc power converters; gapped magnetic core; magnetic permeability; magnetizing inductance; medium frequency transformer

1. Introduction

The medium frequency transformer (MFT) is one of the key components in the isolated dc-dc converters [1–4] related to: smart grids [5], photovoltaic power plants [6], wind power plants [7], and electric vehicle charging [8,9]. The three-phase topology is considered for high power applications where the high power density and high efficiency are required. In [10,11], an analytical approach was proposed to compare multi-phase dc-dc topologies. In [12], the single-phase and three-phase topologies were compared. A 10 kVA 1 kHz three-phase MFT prototype was reported in [13], and a 2 kVA 100 kHz three-phase MFT was reported in [14]. A 5 MW three-phase converter was presented in [15] but using three single-phase MFTs. The general circuit diagram of the three-phase isolated dc-dc converter is composed of two voltage source converters (VSC), and an MFT is presented in Figure 1.

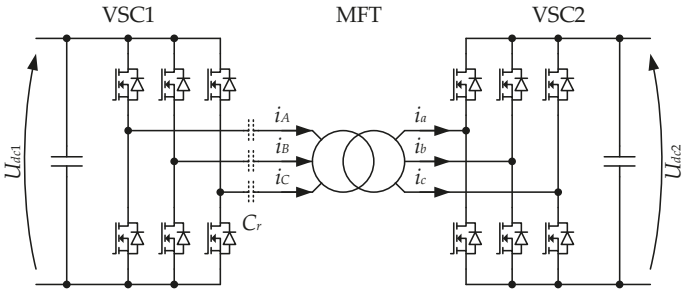


Figure 1. Three-phase isolated dc-dc converter circuit diagram; C_r is the optional resonant capacitor.

The performance of the converter highly depends on the MFT and its equivalent circuit parameters. The leakage inductance has a significant influence on the operation of the converter and the specified value is usually well achieved in the MFT development process. In the LLC resonant dc-dc (LLC) converter [1,16,17], the magnetizing inductance has a significant effect on the zero voltage switching (ZVS) [18–20], but it may be difficult to achieve within reasonable error margins [21]. The maximum value of the magnetizing inductance should take into account the drain-source capacitance C_{ds} of the MOSFET (or other power semiconductor switch). It should ensure the magnetizing current sufficient to charge and discharge the C_{ds} during the dead time of a VSC leg. In the dual active bridge (DAB) converter [2,22], the magnetizing inductance should not increase the VSC current and it should be considered at low operating power.

The operating frequency of the 100 kilowatt class isolated dc-dc converters is considered in the range from few kilohertz to tens of kilohertz [23–25]. The voltage and current fundamentals and harmonics influence the design of the MFT magnetic core and windings. The choice of MFT magnetic core material should be done according to the material properties and cost. The performance factor, which is defined as a product of the frequency and flux density at a specified core loss density, is used to compare different types of core materials [26,27]. The amorphous and especially nanocrystalline materials are preferred in the low and medium frequencies due to the high flux density [28,29]. On the other hand, the main advantage of ferrite cores is their low power loss, which makes them an attractive material for the construction of medium and high frequency transformers [30,31]. The ferrite also offers low cost in terms of material and transformer assembly. In [32], the ferrite core MFT was considered for an optimized dc-dc converter operating at a few kHz. Finally, the ferrite seems as a good candidate for the short term industrialization of the high power three-phase MFT. However, the construction of a ferrite magnetic core for high power MFT requires an assembly of type "I" cores since the C-cores or E-cores do not exist for large transformers. This results in a multi air gap structure of the magnetic core.

The influence of the air gap on the transformer magnetic properties in LLC converters was analysed in [33,34]. It was assumed that the air gap length was known and controlled in the MFT design process. The considered air gaps had relatively large size in order to reduce the slope of the $B(H)$ curve and to minimize the influence of magnetic saturation on the magnetizing inductance value. The influence of the air gap length on the equivalent magnetic permeability, magnetic reluctance and magnetizing inductance in ferrite core transformers was analysed in [35–38]. The influence on the core and winding power loss was studied in [39–41]. All the analysed cases considered a single and uniform air gap of a known length. The analysis of a single but non-uniform air gap in toroidal cores was presented in [42,43]. The influence of the number of uniform air gaps with a controlled size on the magnetic properties and transients in a current transducer was considered in [44].

In the transformer core structure characterized by a construction periodicity (ferromagnetic material—air gap, ferromagnetic material—diamagnetic material, etc.), it is possible to utilize the homogenization technique or multiscale methods in the description of magnetic properties (reluctance

of homogenized core, equivalent magnetic permeability, equivalent $B(H)$, etc.). The use of the homogenization technique in the finite element method (FEM) analysis of step-lap joints in steel sheet transformers was proposed in [45]. The homogenization technique was further developed in 2D FEM of steel sheet cores [46–48] and amorphous cores [49]. The multiscale methods were proposed in the analysis of the magnetic properties of transformer cores in [50]. In order to increase the accuracy of magnetic computations, a higher order FEM [51] and a step-wise method were proposed [52].

In all the presented references, it was assumed that the air gap length or the diamagnetic material dimensions were known. However, during the core assembly, the core experiences different mechanical constraints, which are required to ensure its integrity. This impacts the magnetic properties [53] and changes the core structure near the air gaps. In many cases, these changes are difficult to determine, especially once the core is assembled.

According to the authors' knowledge, a study of multiple air gaps in the ferrite core transformers, enabling an efficient MFT design for the isolated dc-dc converters, has not been reported. In this article, it is proposed the analysis of the number of air gaps on the equivalent $B(H)$ and the equivalent magnetic permeability. It is considered that different MFTs have a similar probability distribution of the average air gap length. The authors propose an experimental approach to the determination of the equivalent $B(H)$, implying that the physical phenomena as: nonlinearity, fringing effect, structure dissymmetry, technological aspects, etc. are taken into account.

The novel aspects of this work includes:

- Determination of the equivalent $B(H)$ and the equivalent magnetic permeability in a three-phase multi air gap ferrite core MFT.
- Demonstration that the equivalent magnetic permeability and the average air gap length of the multi air gap ferrite core MFT are nonlinear functions of the number of air gaps.
- Proposal of an exponential scaling function, enabling a rapid estimation of the magnetizing inductance based on the ferrite material datasheet only.

The multi air gap medium frequency transformer prototype is presented in Section 2. The measurement of the magnetic flux in the function of the magnetizing current and the calculation of the equivalent $B(H)$ and the equivalent magnetic permeability are presented in Section 3. The finite element simulation of the MFT no load test, using the measured equivalent $B(H)$, is presented in Section 4. The FEM simulation result is compared with an experimental measurement on a 100 kW 1.2 kV 20 kHz dc-dc converter in Section 5. The results are analysed and discussed in Section 6, where the influence of the number of air gaps on the equivalent permeability and the average air gap length are presented. A scaling function enabling a rapid estimation of the magnetizing inductance is proposed.

2. High Power Medium Frequency Transformer

2.1. MFT Prototypes

The authors have developed two three-phase MFT prototypes for a 100 kW 1.2 kV 20 kHz dc-dc converter. The dc-dc converter is presented in details in [54]. The three-phase structure is still novel in the MFT applications with very little demonstrators. The specifications of two MFT prototypes T1 and T2 are presented in Table 1. The MFT T1 can operate in delta and star vector groups whereas the T2 in star only. The winding of both transformers is made of the same litz wire composed of 3870 strands of 0.1 mm diameter.

Table 1. Specification of the medium frequency transformer prototypes for the nominal operating conditions.

Parameter	T1 Dd	T1 Yy	T2 Yy
Phase voltage (V)	980	566	566
Phase current (A)	36	65	65
Core flux density (T)	0.22	0.15	0.27
Winding current density (A/mm^2)	1.2	2.1	2.1
Dimensions of active parts (cm)	67 × 20 × 35		45 × 20 × 30
Total weight (kg)	57		36

The MFT T2 is presented in Figure 2 and its design is detailed in [55]. In particular, a significant difference between the calculated and measured magnetizing inductance is highlighted. This shows the important influence of the parasitic air gaps on the magnetizing inductance.

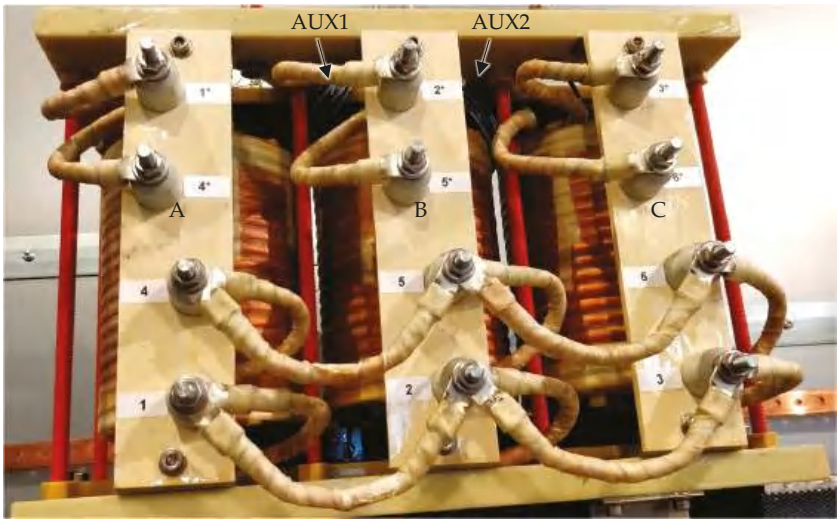


Figure 2. Medium frequency transformer prototype T2 showing primary winding terminals: 1*-1, 2*-2, 3*-3, secondary winding terminals: 4*-4, 5*-5, 6*-6, three columns A, B, C, and additional auxiliary coils AUX1 and AUX2 for flux measurement (blue wire around the yoke).

2.2. Magnetic Core

The magnetic core of the MFT prototypes is made of MnZn ferrite 3C90 from Ferroxcube. The core is assembled with I-cores measuring 25 mm × 25 mm × 100 mm each. The core assembly is presented in Figure 3. In this core design, the I-cores are not interleaved. It can be seen that the core involves multiple parasitic air gaps. Moreover, due to manufacturing tolerances, the I-core is not an ideal rectangular cuboid and its dimensions vary from one sample to another. This causes the non-uniform parasitic air gaps in the core. There are at least two types of parasitic air gaps: perpendicular and longitudinal to the axis of the magnetic flux path. The authors claim that the parasitic air gap size is unpredictable at the industrial design stage and that it cannot be modelled precisely. In Appendix A, some example views of the ferrite core assembly are presented. It can be seen that the air gap length varies from almost zero to about 0.5 mm. Consequently, the use of material datasheet in the calculation of effective magnetizing inductance leads to significant errors. However, the magnetizing inductance or the equivalent $B(H)$ can be measured on the transformer prototype. Such a measurement can be helpful in a new transformer design with a similar core assembly.

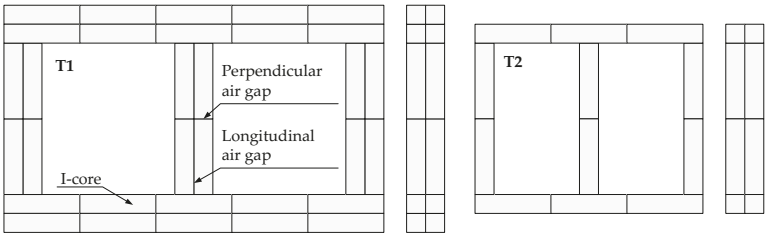


Figure 3. Medium frequency transformer core assembly composed of elementary I-cores: T1 (**left**) and T2 (**right**).

3. Equivalent B(H) Measurement

3.1. Measurement Setup

The nonlinear magnetic properties of core material are represented by the magnetic permeability, which relates the magnetic flux density B with the magnetic field strength H. The nonlinear magnetic properties of a transformer core can be described by the current-dependent flux linkage characteristics $\Psi(i)$ using the experimental approach. From the flux linkage characteristics, the $B(H)$ curve can be determined under certain simplifying assumptions. The measurement of $\Psi(i)$ hysteretic characteristics for inherently asymmetric three-phase transformer with three columns was proposed in [56]. In this approach to determine $\Psi(i)$ characteristics for each winding, only two phases are excited in a special manner.

A dedicated static $B(H)$ measurement setup was developed as presented in Figure 4. It is composed of a high current AC power supply, oscilloscope and probes. The primary and secondary windings of each phase were connected in series in order to achieve a high magnetomotive force (MMF). The windings of two columns were connected in anti-parallel so that their MMFs add together. Two additional auxiliary coils (AUX1 and AUX2) were placed on the yoke allowing the measurement of the magnetic flux in the core (see the blue wire in Figure 2) and minimizing the magnetic coupling in the air. The voltage of the remaining winding (so-called zero-coil) is measured in order to verify that the magnetic flux coupled with this winding is close to zero.

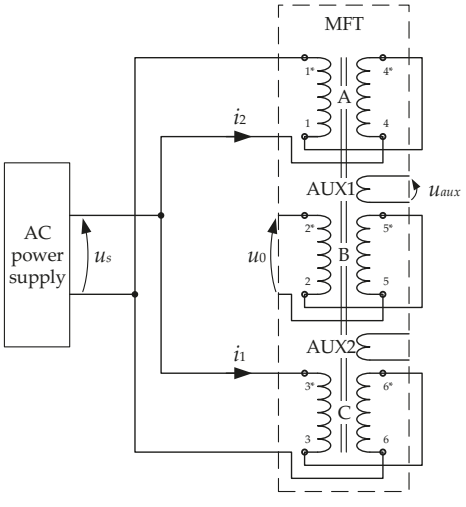
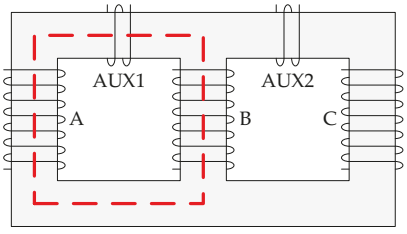
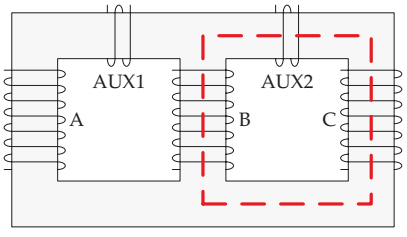
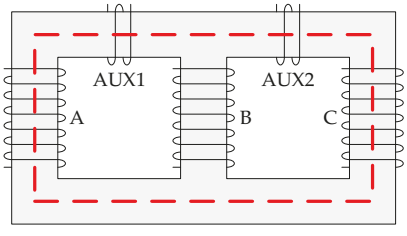


Figure 4. Circuit diagram of the equivalent $B(H)$ measurement setup where the windings C and A are supplied.

For each MFT prototype, three measurements were performed according to the winding configurations presented in Table 2. The frequency of the power supply in the static $B(H)$ measurement setup was set to 100 Hz. This value was considered in order to minimize the effect of eddy currents (considering a high frequency material as ferrite) and to achieve good performance of the available power supply.

Table 2. Winding configurations of the equivalent $B(H)$ mearement circuits.

u_s	u_{aux}	u_0	Magnetic Flux Path
A + B	AUX1	C	
B + C	AUX2	A	
C + A	AUX1 or AUX2	B	

The waveforms of the magnetic flux density $B(t)$ and the magnetic field strength $H(t)$ were calculated with:

$$H(t) = \frac{N_{exc}[i_1(t) + i_2(t)]}{l_m} \quad (1)$$

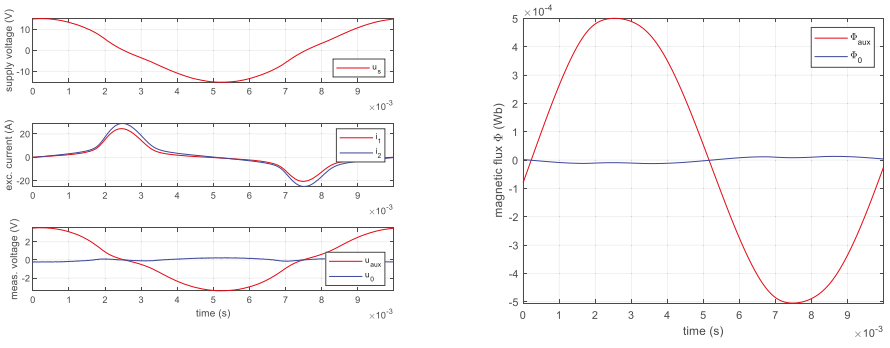
$$\Phi(t) = \int_0^T u_{aux}(t)dt \quad (2)$$

$$B(t) = \frac{\Phi(t)}{N_{aux}A_c}. \quad (3)$$

where i_1 and i_2 are the current of the first and second excitation winding respectively, N_{exc} is the number of turns of each excitation winding, l_m is the average magnetic circuit length (visualized in Table 2), u_{aux} is the voltage of the auxiliary coil placed on the yoke, T is the period of the excitation voltage, Φ is the core magnetic flux, N_{aux} is the number of turns of the auxiliary coil, and A_c is the average cross-section of the core.

3.2. Measurement Results

The measured waveforms for the example case where the C and A windings of T2 are supplied are presented in Figure 5a. The measurement was performed with the transformer temperature equal to ambient at 25 °C. It can be observed that the supply voltage is close to sinusoidal. The currents in two excitation windings show the core saturation. Their amplitudes are slightly different due to a difference in winding impedance. The amplitude of the zero-coil voltage is relatively low.



(**a**) (**b**)

Figure 5. Waveforms of the T2 supplied with C and A windings: (**a**) measured supply voltage u_s, excitation currents i_1 (C) and i_2 (A), auxiliary coil voltage u_{aux} (AUX1) and zero coil voltage u_0 (B); (**b**) magnetic flux of the auxiliary coil Φ_{aux} (AUX1) and magnetic flux of the zero coil Φ_0 (B).

Figure 5b presents the waveforms of the magnetic flux calculated according to (2). The Φ_{aux} correspond to the main magnetic flux in two side columns and two yokes. The Φ_0 corresponds to the magnetic flux in the central column. It is observed that the magnetic flux in the central column is below 5% of the main flux so it seems fair to neglect it.

Thanks to (1) and (3), the magnetic field strength H and the magnetic flux density B are calculated. In Figure 6, the resulting $B(H)$ is plotted for the positive values of H. The $B(H)$ is separated into the upward and downward curves, which are then interpolated with piecewise linear functions in order to facilitate the data analysis. The anhysteretic $B(H)$ curve is calculated as the average of the interpolated upward and downward curves and further filtered to achieve a smooth curve adequate for further processing. Moreover, the coercive field H_c and remanent flux density B_r can be captured.

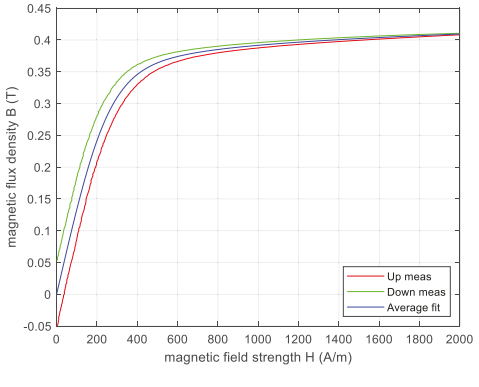
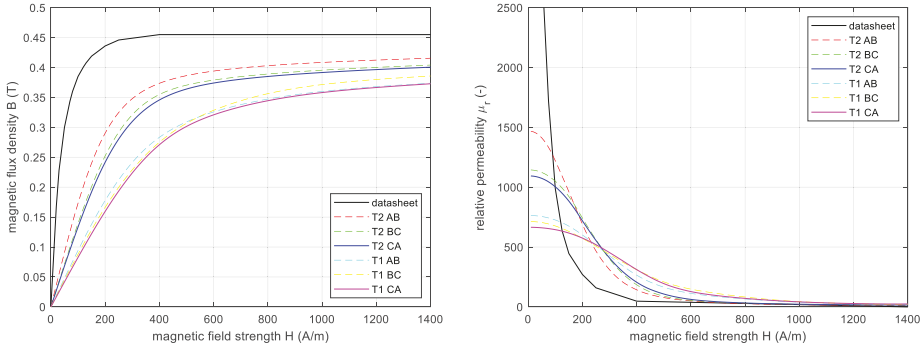


Figure 6. Measured equivalent $B(H)$ of the T2 supplied with C and A windings: upward curve (red), downward curve (green) and interpolated anhysteretic curve (blue).

3.3. Synthesis of Equivalent B(H) Measurement

The measurement process presented in the previous section was repeated for the MFT T1 and T2 for the cases with the supply of windings: A and B, B and C, and C and A, according to Table 2. The measured equivalent anhysteretic $B(H)$ and relative permeability $\mu_r(H)$ are presented in Figure 7. The 3C90 datasheet curves [57] are plotted for comparison. As expected, a significant difference between the datasheet and the measurement is observed. There is a difference between T1 and T2 since they have a different core assembly, T1 having more parasitic air gaps than T2 (see Figure 3). For each MFT, the equivalent $B(H)$ differs slightly for different measurement circuits. This proves that the parasitic air gaps are randomly distributed in the core assembly. For each transformer, the authors arbitrarily select the solid line curve (CA) as the reference $B(H)$ for the whole core.



(**a**) (**b**)

Figure 7. Synthesis of equivalent $B(H)$ measurement: (**a**) equivalent anhysteretic $B(H)$; (**b**) equivalent relative permeability μ_r; curves based on 3C90 datasheet (black) and measurement: T2 supply of A and B windings (red), T2 supply of B and C windings (green), T2 supply of C and A windings (blue)—the same as in Figure 6, T1 supply of A and B windings (cyan), T1 supply of B and C windings (yellow), T1 supply of C and A windings (magenta).

4. Finite Element Simulation

4.1. Finite Element Model

A 3D MFT T2 model was developed in Ansys Maxwell. A simplified transformer geometry was considered. The model was divided into three computational domains as shown in Figure 8. The Ω_1 domain is the volume of the windings, the Ω_2 domain is the volume of the core, and the Ω_3 domain consists of the air surrounding the MFT. In this model, it is assumed that the magnetic core is homogenized. It means that the core components: ferrite, air gaps and also glue, impregnation resin, etc. form a homogenous material. In a similar manner, the winding is also homogenized.

The Maxwell's equations for the defined domains have the form:

$$\nabla \times \mathbf{H} = \begin{cases} \mathbf{j} \text{ in } \Omega_1 \\ \overleftrightarrow{\boldsymbol{\sigma}}\mathbf{E} \text{ in } \Omega_2 \\ 0 \text{ in } \Omega_3 \end{cases} \tag{4}$$

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}; \nabla \bullet \mathbf{B} = 0; \mathbf{B} = \nabla \times \mathbf{A} \tag{5}$$

where $\overleftrightarrow{\boldsymbol{\sigma}}$ is the electrical conductivity tensor:

$$\overleftrightarrow{\boldsymbol{\sigma}} = \begin{bmatrix} \sigma_{xx}(x,y,z) & 0 & 0 \\ 0 & \sigma_{yy}(x,y,z) & 0 \\ 0 & 0 & \sigma_{zz}(x,y,z) \end{bmatrix} \tag{6}$$

The permeability tensor, which for nonlinear properties describes the relation between dB and dH in the constitutive equation, can be expressed as:

$$\overleftrightarrow{\boldsymbol{\mu}} = \begin{cases} \mu_0 \text{ in } \Omega_1 \\ \overleftrightarrow{\boldsymbol{\mu}}_{core} \text{ in } \Omega_2 \\ \mu_0 \text{ in } \Omega_3 \end{cases} \tag{7}$$

where $\overleftrightarrow{\boldsymbol{\mu}}_{core}$ is the magnetic permeability tensor:

$$\overleftrightarrow{\boldsymbol{\mu}}_{core} = \begin{bmatrix} \mu_{xx}(x,y,z) & 0 & 0 \\ 0 & \mu_{yy}(x,y,z) & 0 \\ 0 & 0 & \mu_{zz}(x,y,z) \end{bmatrix} \tag{8}$$

It was assumed that the ferrite core has isotropic electrical and magnetic properties. Hence, the electrical conductivity and magnetic permeability tensors have the form:

$$\overleftrightarrow{\boldsymbol{\sigma}} = \begin{bmatrix} \sigma_c & 0 & 0 \\ 0 & \sigma_c & 0 \\ 0 & 0 & \sigma_c \end{bmatrix}; \overleftrightarrow{\boldsymbol{\mu}}_{core} = \begin{bmatrix} \mu_c & 0 & 0 \\ 0 & \mu_c & 0 \\ 0 & 0 & \mu_c \end{bmatrix} \tag{9}$$

where σ_c = 0.25 S/m (at 25 °C) and μ_c = dB/dH are defined in the previous section (Figure 7b, curve T2 CA). In Ansys Maxwell, the material conductivity enables the calculation of eddy current effects. However, it can be noticed that the ferrite conductivity is low so the eddy current effects do not have a significant impact on the magnetic field and core power loss.

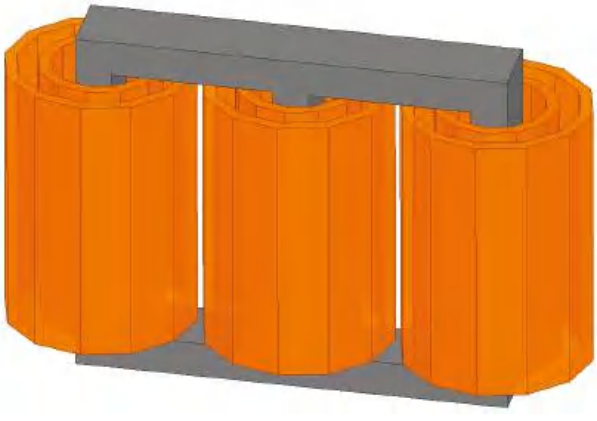


Figure 8. 3D MFT model divided into three computational domains: Ω_1 volume of the windings (orange), Ω_2 volume of the homogenized core (grey) and Ω_3 air surrounding the MFT (white).

4.2. Magnetic Simulations

In order to perform a magnetic transient simulation, the finite element model was coupled with an equivalent circuit model. A no load test was considered, as presented in Figure 9. The coupling

between the finite element model and the equivalent circuit model is done through the nonlinear inductances L_1, L_2 and L_3, which correspond to the primary winding. The voltage sources model the VSC square output voltage, and R_p is the primary winding resistance.

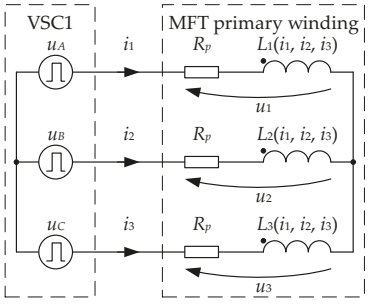


Figure 9. MFT no load test equivalent circuit model coupled with the finite element model through the nonlinear inductances L_1, L_2 and L_3.

The magnetic transient simulation result is presented in Figure 10. The MFT phase voltage is presented, being a typical VSC output voltage waveform. The MFT primary current is presented in steady-state. This result will be further used to validate the measured equivalent $B(H)$.

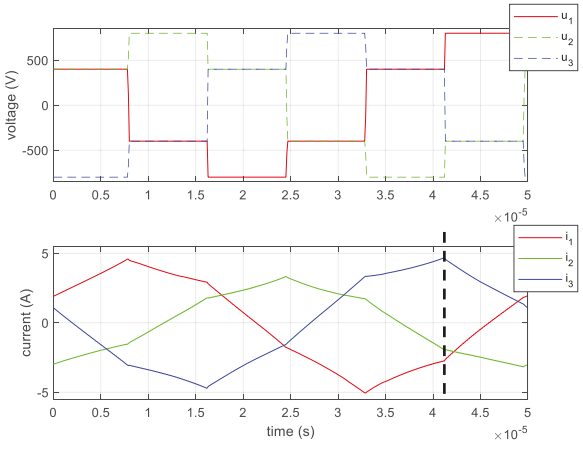


Figure 10. MFT no load test magnetic transient simulation result: primary phase voltage (**top**) and primary current (**bottom**); the dashed vertical line indicates the time instant for the magnetostatic simulation.

In Figure 11, the magnetostatic simulation result corresponding to the time instant defined by the dashed line in Figure 10 is presented. The magnitude of the flux density is plotted on the core surface and the maximum value of 0.27 T is observed, as expected. In Figure 12, the magnetic field strength and the magnetic flux density are plotted along the path defined by the dashed line in Figure 11. The different values of quotient $B/(\mu_0 H)$ in the central and the right column can be observed due to the nonlinearity of the $B(H)$ curve.

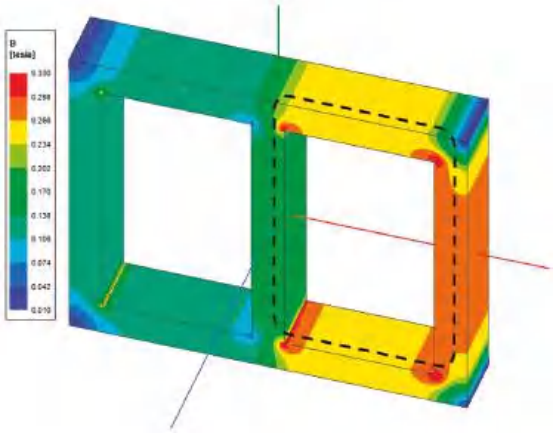


Figure 11. Magnetic flux density B magnitude on the core surface with the current excitation $i_1 = -2.76$ A, $i_2 = -1.93$ A, $i_3 = 4.69$ A; the dashed line indicates the magnetic flux path in the centre of the core.

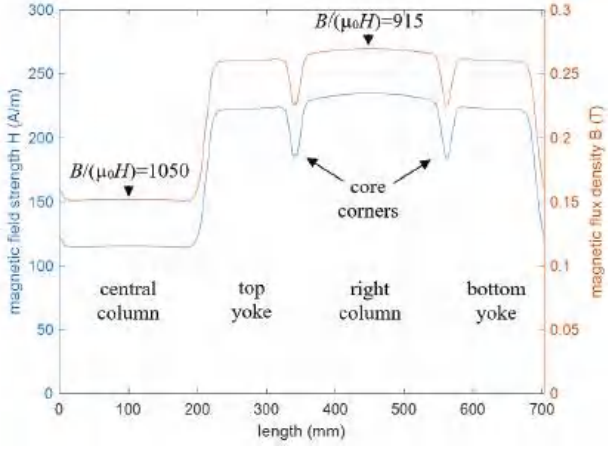


Figure 12. Magnetic field strength H and magnetic flux density B along the path in the centre of the core passing through the central column, top yoke, right column, and bottom yoke; the values of static permeability $B/(\mu_0 H)$ are presented.

5. Experimental Verifications

5.1. Converter Test Bench

The power converter test bench was developed for the 100 kW dc-dc converter, as presented in Figure 13. A MFT no load test was considered in order to evaluate the magnetizing inductance. In the no load test, the VSC1 operates normally with 1200 Vdc input voltage and the AC terminals of the VSC2 are disconnected. The circuit diagram of the experimental setup is equivalent to the one used in the simulation that is presented in Figure 9. The test was performed at an ambient temperature of 25 °C. The MFT temperature was measured nearly equal to the ambient as the test lasts for a few minutes only.

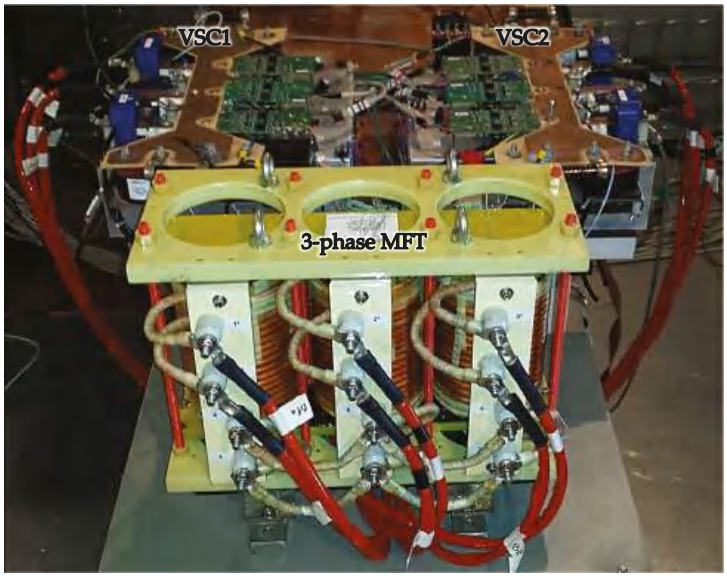


Figure 13. 100 kW three-phase isolated dc-dc converter test bench implementation.

5.2. No Load Test Experimental Results

The measured waveform of the MFT T2 no load current is presented in Figure 14. The simulated no load current from the previous section is plotted for the comparison. Generally, quite a good fit between the simulation and the measurement is observed. Some minor differences are discussed hereafter.

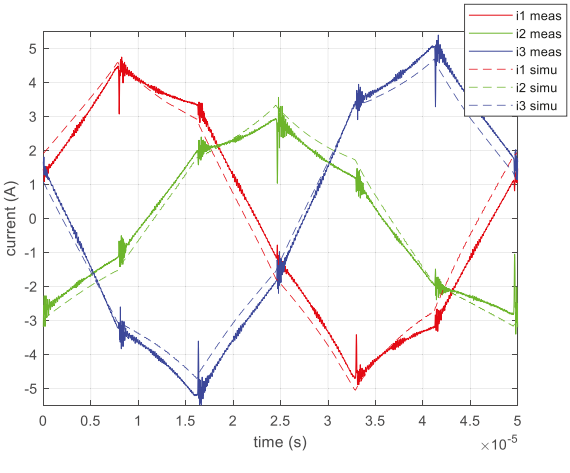


Figure 14. MFT T2 no load test primary current: experimental result (solid line), magnetic transient simulation result (dashed line).

There are some high frequency oscillations present in the measurement. They are due to the parasitic capacitance of the windings that have not been modelled. This could be improved by adding the winding self and mutual capacitances into the model. However, the simulation time would increase significantly.

There are some differences in the current amplitude of different phases. As it has been presented in Figure 7, the $B(H)$ is not strictly the same for the whole core. Since in the simulation, the authors have assumed a single equivalent $B(H)$, then it seems normal to observe some differences in the measured currents.

Moreover, there might be some differences due to the fact that the simulation model assumes the anhysteretic $B(H)$. In Figure 6, one can see that the measured equivalent $B(H)$ is hysteretic, thus it may influence the shape of the current waveform, in particular, the corresponding ascending and descending slopes of the current.

Finally, the RMS current error is within 10% and the authors consider this acceptable. If the datasheet $B(H)$ was used (Figure 7), then the RMS current error would reach approximately 500%. This experimental result proves the validity of the measured equivalent $B(H)$.

6. Scaling of Relative Permeability

The approach presented in the previous paragraphs has limited usage in the MFT design process since it is based on the measurement on a physical device. This limits the practical usage to post-manufacturing analysis or to a new design of a similar transformer. In this section, an approach based on a simple count of perpendicular parasitic air gaps is proposed.

In the MFT design process from scratch, when evaluating the performance of isolated dc-dc converters, one is usually interested in the magnetizing inductance at the nominal $B(H)$ operating point. This is usually below the $B(H)$ saturation, so the anhysteretic curve from Figure 7 can be linearized as presented in Figure 15.

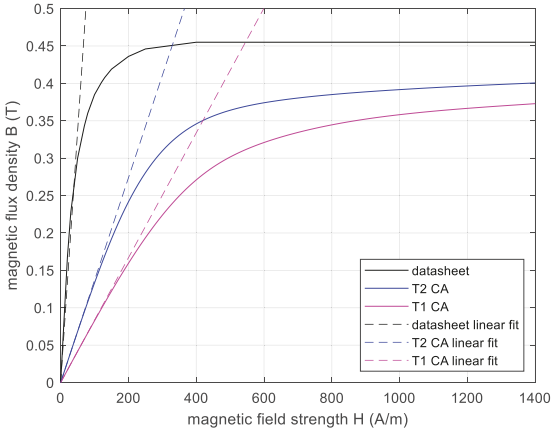


Figure 15. Equivalent anhysteretic $B(H)$: datasheet and measurement (solid line), linear interpolation (dashed line).

From Figure 3, we can count the number of perpendicular parasitic air gaps along the magnetic path. This equals to 10 and 14 for T2 and T1 respectively. The core used for the datasheet measurement had zero air gaps. The value of datasheet linearized relative permeability, which equals $\mu_{r0} = 5300$, is read from Figure 15. Thus, the equivalent relative permeability ratio K_μ of the multi air gap core can be calculated with:

$$K_\mu = \frac{\mu_r}{\mu_{r0}} \tag{10}$$

where μ_r is the equivalent relative permeability defined in Figure 15 for T1 or T2. The equivalent relative permeability ratio is plotted in Figure 16 as a function of a number of parasitic air gaps.

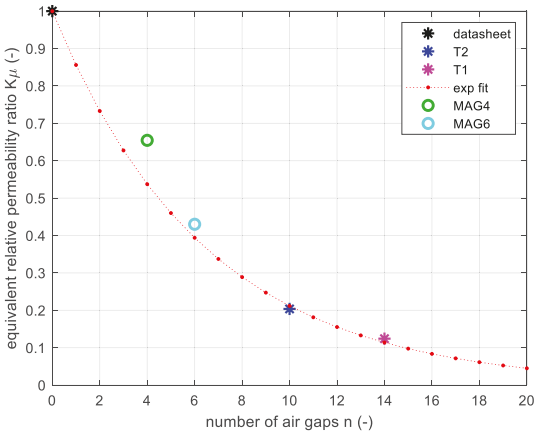


Figure 16. Equivalent relative permeability ratio K_μ in the function of a number of parasitic air gaps n: datasheet, T2 and T1 measurement (stars), exponential interpolation (red dashed line), and single-phase multi air gap transformer MAG4 and MAG6 measurement (circles).

In addition, an exponential interpolation is proposed allowing to estimate the equivalent relative permeability for any high power ferrite core MFT with a similar core assembly. The exponential interpolation function is defined as:

$$K_\mu(n) = e^{-0.155n} \tag{11}$$

where n is the number of perpendicular parasitic air gaps along the magnetic flux path.

This function was validated with the experimental $B(H)$ measurement on two single-phase multi air gap (MAG) transformers presented in Appendix B. The MAG4 transformer has four air gaps and MAG6 has six air gaps. Both use the same I-cores as T1 and T2. The resulting ratios are displayed in Figure 16 and it can be seen that for MAG4 the ratio is slightly higher than the exponential interpolation. This is normal because for this transformer the I-cores were carefully selected to minimize the parasitic air gaps and the core assembly is simpler compared to the three-phase MFT. However, a general trend of the equivalent relative permeability ratio is clearly observed even if the four MFT prototypes involve different technologies and different manufacturers.

Furthermore, a simple reluctance model of the magnetic core neglecting the fringing effect is considered according to [35]. The total magnetic circuit reluctance can be related to the sum of the I-core and air gap reluctances as:

$$\frac{l_m}{\mu_0 \mu_r A_c} = n \frac{l_I}{\mu_0 \mu_{r0} A_c} + \frac{l_a}{\mu_0 A_c} \tag{12}$$

where l_m is the average magnetic circuit length, l_I is the length of the I-core, l_a is the average air gap length, and A_c is the average cross-section of the core. Assuming that the average magnetic circuit length l_m is equal to $n \cdot l_I$, then it can be found the relative average air gap length l_a/l_m defined as:

$$\frac{l_a}{l_m} = \frac{1}{\mu_r} - \frac{1}{\mu_{r0}} \tag{13}$$

Considering an ideal core assembly, where the average air gap length l_a equals n times the known individual air gap length l_g, the relative average air gap length l_a/l_m is a linear function of n:

$$\frac{l_a}{l_m} = \frac{l_g}{l_m} n \tag{14}$$

In Figure 17, these linear functions are presented for four transformers T2, T1, MAG4, and MAG6. It was verified that the individual air gap length l_g changes between prototypes. However, considering the proposed exponential interpolation (11), the effective relative average air gap length is a nonlinear function of n as presented in Figure 17. This is due to the fact that the I-core is not an ideal rectangular cuboid and its dimensions vary from one sample to another. As a consequence, the mechanical assembly of the core gets more difficult when a large number of I-cores is assembled.

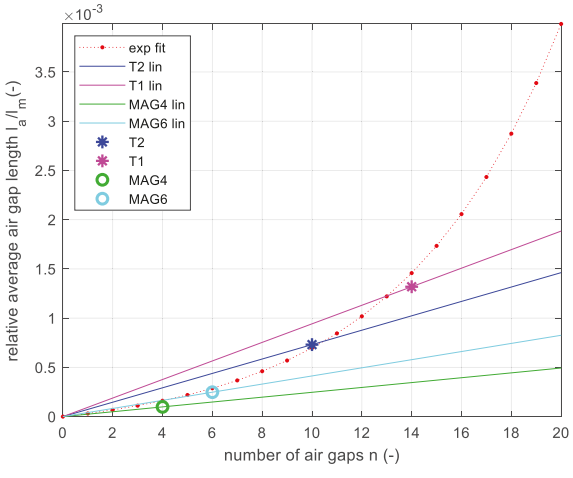


Figure 17. Relative average air gap length l_a/l_m in the function of a number of parasitic air gaps n: T2, T1, MAG4 and MAG6 measurement (stars/circle), the corresponding idealized reluctance model (solid lines), and the relative average air gap length calculated based on the proposed exponential interpolation (red dashed line).

The proposed approach can be used in scaling the datasheet $B(H)$ for a finite element simulation, in the rapid estimation of transformer magnetizing inductance or in evaluating the size of the average air gap length. The magnetizing inductance can be estimated based on the magnetic reluctance model according to:

$$L_m = K_\mu(n)\frac{\mu_0\mu_{r0}N^2A_c}{l_m} \tag{15}$$

where N is the primary/secondary number of turns. It shall be mentioned that the proposed estimation is meant to provide an order of magnitude of the magnetizing inductance. This shall be sufficient when evaluating the performance of isolated dc-dc converters. However, the proposed scaling function could be further validated with a large number of MFT prototypes with different types of I-cores and a different number of parasitic air gaps.

7. Conclusions

The analysis of the effective permeability and average air gap length in multi air gap ferrite core three-phase medium frequency transformer was presented. The calculation of the magnetizing inductance in multi air gap ferrite core MFT based on core material datasheet leads to significant errors. This may impact the design of isolated dc-dc converters as the magnetizing inductance influences their performance.

The measurement of the equivalent $B(H)$ and the equivalent permeability for two three-phase MFT prototypes was presented. The measured equivalent $B(H)$ was used in a finite element simulation, giving good results when compared to a 100 kW dc-dc converter no load operation. The use of the anhysteretic $B(H)$ gives satisfactory results within 10% error compared to the experiment.

This article demonstrates that the equivalent magnetic permeability and the average air gap length of the multi air gap ferrite core MFT are nonlinear functions of the number of air gaps. An empirical scaling function is proposed for the rapid estimation of the magnetizing inductance in the multi air gap MFT. In fact, the relative average air gap length increases with the number of parasitic air gaps due to the increasing difficulty in mechanical assembly of the core. The proposed scaling function can be used in the design of isolated dc-dc converters using 25 mm × 25 mm × 100 mm I-cores or similar, based on the core material datasheet and a number of parasitic air gaps.

The measured or scaled equivalent $B(H)$ can also be used in the equivalent circuit simulation instead of finite element simulation. This would allow more convenient simulations as well including the winding capacitance. The measured $B(H)$ can be further utilized in the simulations taking into account the hysteresis. This work shall be further extended taking into account the influence of the temperature since the ferrite relative permeability depends on the temperature. The proposed scaling function could be further validated with a large number of MFT prototypes with different types of I-cores and a different number of parasitic air gaps in order to determine the uncertainty range. The experimental validation of the influence of the magnetizing inductance on the performance of three-phase isolated dc-dc converters is recommended.

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Appendix A

In Figure A1, two example views of the ferrite core assembly are presented where the perpendicular and longitudinal parasitic air gaps can be observed up to about 0.5 mm. In each assembly, 4 randomly selected I-cores are aligned along a calliper on a flat surface. The I-cores are assembled tight together so that even if there is an air gap on the visible surface then there is somewhere a direct contact between the neighbour I-cores. In the 3-phase MFT core assembly, composed of tens of I-cores, the air gaps are even larger due to the cumulating I-core misalignments.

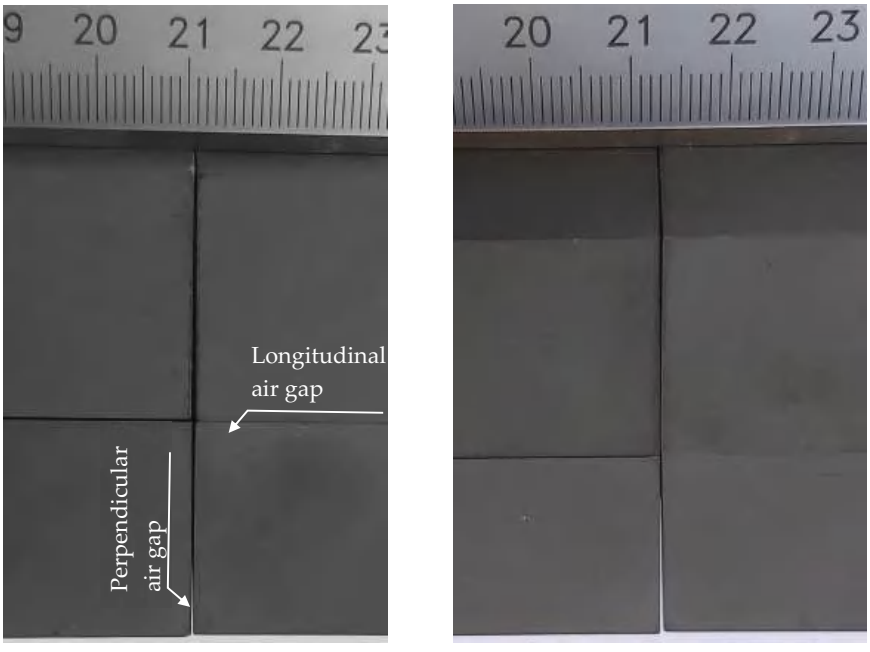

Figure A1. Two assemblies of 4 randomly selected 3C90 ferrite I-cores showing the perpendicular parasitic air gap and the longitudinal parasitic air gap measuring up to about 0.5 mm.

Appendix B

The core assemblies of the single-phase multi air gap MFTs are presented in Figure A2. The MAG4 has 4 and the MAG6 has 6 perpendicular parasitic air gaps along the magnetic flux path. The MAG4 is detailed in [58].

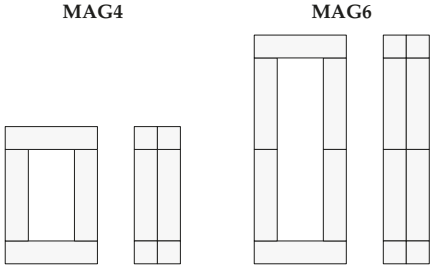

Figure A2. Single-phase multi air gap MFT core assembly: MFT4 with 4 air gaps (**left**) and MFT6 with 6 air gaps (**right**).

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SiC-Based Power Electronic Traction Transformer (PETT) for 3 kV DC Rail Traction

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Abstract: The design of rolling stock plays a key role in the attractiveness of the rail transport. Train design must strictly meet the requirements of rail operators to ensure high quality and cost-effective services. Semiconductor power devices made from silicon carbide (SiC) have reached a level of technology enabling their widespread use in traction power converters. SiC transistors offering energy savings, quieter operation, improved reliability and reduced maintenance costs have become the choice for the next-generation railway power converters and are quickly replacing the IGBT technology which has been used for decades. The paper describes the design and development of a novel SiC-based DC power electronic traction transformer (PETT) intended for electric multiple units (EMUs) operated in 3 kV DC rail traction. The details related to the 0.5 MVA peak power medium voltage prototype, including the electrical design of the main building blocks are presented in the first part of the paper. The second part deals with the implementation of the developed SiC-based DC PETT into a regional train operating on a 3 kV DC traction system. The experimental results obtained during the testing are presented to demonstrate the performance of the developed 3 kV DC PETT prototype.

Keywords: silicon carbide; dual active bridge dc-dc converter; power electronic traction transformer; 3 kV DC railway traction; electric multiple unit

1. Introduction

Rail is among the most efficient and lowest emission modes of transport. It is under constant pressure to increase the accessibility of connections and quality of passenger services to enhance their competitiveness with other transport modes. For rail to compete more effectively with other modes of transport and attract more passengers, it needs the next generation of passenger trains that will be lighter, more energy-efficient and cost-effective. Traditional passenger trains consisting of a locomotive and several carriages penalize performance in terms of acceleration since they have a limited number of available drive wheelsets. Modern electric multiple units (EMUs) do not require a locomotive, as hey consist of several self-propelled units in a fixed assembly. Traction is distributed along the length of the train and the motors are housed by bogies of different carriages [1]. The demand for EMUs used for local, regional and intercity transport, grows globally every year. Thanks to the use of common bogies for the central wagons, EMUs are shorter and lighter than trains pulled by locomotives. This translates into lower movement resistance, better acceleration and lower energy consumption [2]. Moreover, EMUs better implement the specificity of passenger traffic and station service as they have a greater number of doors and provide better exchange of travelers.

Quantitatively, the most important part of energy drawn from the overhead traction line by an EMU is consumed by the traction propulsion systems. Traction drive is crucial for the EMU's efficiency, reliability and availability. The on-board propulsion converters, which for years have been traditionally

installed in separate technical compartments, are currently mounted on the roof [3] or under the floor [4,5] of the EMU train. This corresponds to the growing requirements for the number of passenger seats due to the limited length of the passenger train.

The most common R&D works carried out by the manufacturers of traction drives are focused on improving efficiency and reducing the size of the on-board propulsion and power systems [3–6]. Another important topic is the reduction of noise emission [3]. Noise from mechanical and electrical components is troublesome to the human ear and significantly reduces travel comfort. A noticeable source is the working traction motor, whose noise depends on the frequency of switching transistors and the control method used in the drive inverter [7,8].

In the case of a drive inverter for rolling stock for 3 kV DC traction, it would be difficult to find any significant changes in the construction and control technology in the last decades [2,9,10]. The 3 kV dc-line voltage is a challenging task for power electronics. Due to a significant voltage drop on the overhead line, the traction power supply works at a higher voltage, usually 3.6 kV or even higher. This results in a requirement where the operation of a vehicle is often expected from 2.4 kV up to more than 4 kV, with the nominal power available from 2.8 kV or 3 kV DC [9]. A power conversion chain operating under direct current catenary is reduced to a bulky input filter and a voltage source inverter (VSI). Nowadays, EMUs powered by 3 kV DC voltage are equipped with two-level VSIs constructed of six 6.5 kV insulated gate bipolar transistors (IGBTs) generating pulse width modulated (PWM) voltage for supplying medium voltage asynchronous traction motors.

A small number of EMUs are equipped with three-level neutral point clamped (NPC) VSIs using 3.3 kV IGBTs [11]. A typical traction drive with a two-level VSI is shown in Figure 1a. In such a system, the LC filter capacitor also takes on the role of energy storage and is cyclically charged and discharged with impulse currents. The line filter choke, which is the most massive element of the inverter and weighs several hundred kgs, serves to limit high frequency, high di/dt pulse currents flowing between the catenary and the traction vehicle when the capacitor is recharged.

The power supply of the inverter has a large impact on both noise and the electromagnetic and thermal properties of traction motors. Table 1 shows the switching frequencies of HV IGBTs used in propulsion inverters for 3kV DC traction.

The harmonic voltages caused by PWM inverters operated with frequency ranging from individual hundreds of Hz to 2 kHz are the cause of significant current heat losses in the traction motor winding resistances [7,8]. The additional losses due to inverter supply can amount in the range of a few percent of the rated motor power and also occur in the laminated core of the traction motor. The winding and core losses most notably entail thermal problems, increasing the traction motor temperature by an average 30–50 K compared with a sinusoidal supply [8], but also lead to reductions in efficiency. Moreover, the negative effects of the low frequency PWM operation of the inverter feeding the traction motor are increased mechanical loads and increased noise emission. Typical voltage and current transients during the switching of the 6.5 kV IGBT are shown in Figure 1b. The main reason for low IGBT switching frequency are the relatively long switching times of the order of several microseconds and a characteristic current tail during turning off. The increase in the switching frequency of IGBTs would be at the expense of an unacceptable increase in the switching losses. Due to the above-mentioned reasons, current research and development conducted by manufacturers of the traction drives for rolling stock are focused on the utilization of new generation power transistors made of silicon carbide (SiC). Thanks to the exceptional properties, such as: significant achievable energy savings, quieter operation, improved reliability, and reduction in maintenance costs, SiC MOSFETs are ideal for traction power converters new designs instead IGBTs—which were in use in the rolling stock industry for decades [3–6,10]. The most obvious benefit of SiC metal-oxide semiconductor field-effect transistors (MOSFETs) compared to IGBTs is a significant reduction in switching losses, up to 55%, and total power losses, up to 80% [6].

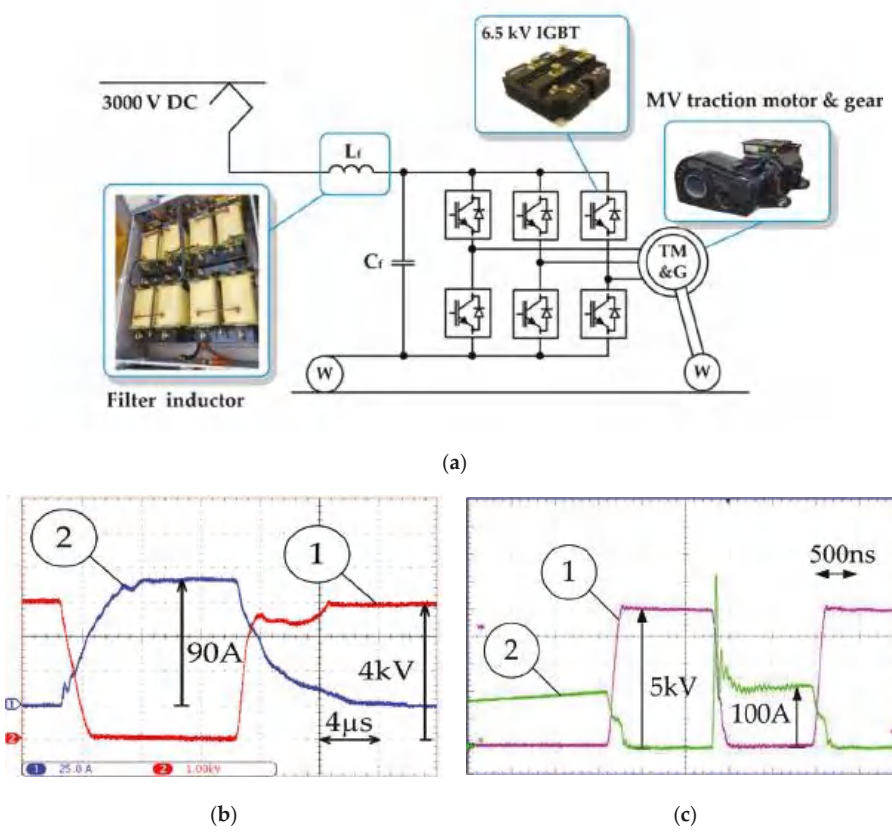


Figure 1. Conventional electric drive of 3 kV DC traction rolling stock with asynchronous traction motor and 6.5 kV IGBT-based two-level inverter: L_f, C_f—inductance and capacitance of the traction line filter; TM&G—traction motor and gear, w—wheels (**a**); Typical collector-emitter voltage (1) and collector current (2) transients during switching of the 6.5 kV IGBT, 4µs/div (**b**); Typical drain-source voltage (1) and drain current (2) transients during switching of the 10 kV SiC MOSFET, 500 ns/div (**c**) (comparison in the text).

Table 1. Switching frequencies of HV IGBTs used in rail inverters for 3kV DC traction.

Inverter Type	Manufacturer	Topology	IGBT Ratings	Switching Frequency	Brochure Publication Year
BORDLINE® CC750	ABB	three-level	3.3 kV/1200 A	2 kHz	2018
FT-800-3000-LQC	MEDCOM	two-level	6.5 kV/600 A	1 kHz	2018
TF09 Traction converter	INGETEAM	two-level	6.5 kV/600A	500 Hz	2012

Typical voltage and current transients during switching of the 10 kV SiC MOSFET are shown in Figure 1b. As it can be seen from Figure 1, in the case of an SiC-MOSFET there is in principle no tail current, and so without this contribution, clearly the switching loss is extremely smaller. Table 2 shows the overall losses distribution between the switching and conductive losses for HV SiC MOSFET and HV IGBT technology [12].

Table 2. Loss comparison between IGBT and SiC MOSFET: 5 kV, 33A/cm^2, 50% duty [12].

Device	Breakdown Voltage	$P_{switching}$ 500 Hz	$P_{switching}$ 5 kHz	$P_{switching}$ 20 kHz	$P_{conduction}$ 100 °C
Si IGBT 5SMX 12M6500	2 × 6.5 kV *	72.5 W/cm^2	725 W/cm^2	2900 W/cm^2	182 W/cm^2
SiC n-IGBT CREE	12 kV	6.5 W/cm^2	65 W/cm^2	260 W/cm^2	100 W/cm^2
SiC MOSFET CREE/Powerex	10 kV	4 W/cm^2	40 W/cm^2	160 W/cm^2	100 W/cm^2

* two 6.5 kV IGBTs in series have been selected as device closest to HV SiC IGBT and SiC MOSFET.

The IGBT switching frequency is limited by the power dissipation, which increases the IGBT junction temperature. To preserve the reliability of operation, the total power dissipation density is limited at the value of 200 W/cm^2 which maintains the chip temperature of 125 °C. The packaging technology further reduces the switching losses of the IGBT to 100 W/cm^2, which is the reason for limiting the operating frequency of the 6.5 kV IGBT-based two-level inverters to below 1000 Hz.

Lower switching losses of HV SiC MOSFETs give the possibility of increasing the PWM frequency of the propulsion converters towards tens of kilohertz. This, in turn, makes it possible to reduce the size of passive components of the traction inverter-primarily the bulky traction line filter. The weight of the filter inductor for the conventional traction inverter shown in Figure 1a is about 500 kg. The unique properties of SiC transistors allow to reduce the weight of the input filter inductor proportionally to the increase in the switching frequency. The issue supporting the reduction of dimensions of the input filter is the use of an additional high-efficiency active-front end (AFE) stage at the input of the traction inverter, which provides regulation of the current drawn from the grid. Due to the lower losses of SiC devices, the need for cooling is also substantially reduced [5]. Reducing the size of the cooling system leads to a reduction in the volume, weight and costs of the entire traction drive [6,8–10].

The higher resolution of the PWM generation in SiC-based traction inverters has a positive effect on reducing harmonic losses of the traction motors-making the whole traction systems more efficient. As stated in [4], the use of SiC power modules combined with expanding the control region outputting regeneration torque have made it possible to reduce the energy consumption rate of the railbound vehicle operated on suburban line by more than 37% compared to conventional systems. By increasing the PWM frequency above 20 kHz the acoustic noise level on the platform and in the cabin may be pushed beyond the audible range. In the case of railway inverters, the switching frequency of high voltage (3.3 kV and 10 kV) MOSFET SiC transistors is several kHz [4–6]. In order to obtain noiseless operation of MV drives, multi-level topologies are used with the use of low-voltage (1.2 kV or 1.7 kV) SiC transistors. Among others, power electronic traction transformers (PETTs), built with power electronic building blocks (PEBB) with built-in input/output isolation, realized by small size and high power density medium frequency transformers (MFT) are of particular interest [13–19].

So far, the primary purpose of SiC-based PETTs were primarily traction drives powered from the AC lines: 15 kV/16.7 Hz [13,14,18,19] and 25 kV/50 Hz [15–17]. AC powered locomotives and EMUs have a complex and voluminous conversion chain including a step-down transformer, rectifier, low-frequency filter and traction inverter. Conventional line frequency transformers (LFTs) used in AC EMUs occupy up to 12% of the weight of rail vehicle and a corresponding part of the train space [2]. Lightweight PETTs using MFTs, if they replaced bulky LFTs, could be easily installed on the roof, resulting in more space for passengers inside the train. AC PETTs offer not only a way to reduce the weight of the on-board electric equipment, but also to add additional functionalities and improve energy efficiency [19].

Strictly speaking, the AC PETT replaces the system of an LFT and an active rectifier and the AC PETT topology does not include a propulsion inverter, which stays the same as in a classical propulsion system and is connected to DC output terminals of the PETT [3,13–19].

As it has been highlighted in [13], the presently most promising medium frequency MF topologies for traction feature on their input-side a large number of series connected four-quadrant converters, with an overall switching frequency in the range of 5–8 kHz, modulated with Phase-Shifted PWM.

The results presented in [13] have shown that the use of a passively-damped LCL filter for the input-side results in a significantly lighter solution, compared to a single-pole type (single inductor) reported in most cases. The work [14] shows the benefits of using the originally 15 kV/16.7 Hz-type PETT in a traction drive supplied from a 3kV DC network. The main innovation aspect of the PETT proposed in [14] is the possibility to be operated with a HV-AC electric system, as well as after reconfiguration on a MV-DC catenary. A three-stage technology have been studied. Four-quadrant converters (4QC) connected in cascade and forming the PETT input stage provide, via insulated dual active bridge (DAB) DC-DC converters, voltage stabilization at the output DC terminals of the PETT, while limiting the ripple of current drawn from the DC traction network. Two solutions have been presented: the first solution using hard switching techniques, using a three-times silicon-conversion, and a second solution based on ZVT/ZCS switching of silicon semiconductor devices. The DC PETT described in [14] provides a higher quality of drive operation during DC voltage disturbances which normally occur in 3 kV DC traction, than conventional propulsion systems with two-level and three-level inverters. Prototype modules have been realized with association of diodes and IGBTs in order to provide reverse-blocking devices. However, the concept was verified only on a small scale test rig. The works [15] and [16] present the method of optimal sizing of 25 kV/50 Hz-type PETTs using 3.3 kV SiC MOSFETs that leads to the best efficiency at rated power in a given volume. The authors emphasize that the efficiency cannot be the only parameter to make a clear choice of an isolated DC-DC converter included in a PETT. An important parameter should be also the acoustic noise, even if it is difficult to take it into account in preliminary studies. The results obtained in [16] for 3.3 kV SiC MOSFET-based resonant DC-DC converters show that designing converters with a switching frequency in the range of 20 kHz would not lead to a dramatic reduction of the PETT efficiency. In [19] the design and development of the 1.2 MVA medium voltage PETT prototype for 15 kV/16.7 Hz traction applications have been presented. The use of MFTs developed in [19] allows for weight reduction and power density improvement (0.5–0.75 kVA/kg) compared to conventional traction chains (0.2–0.35 kVA/kg). The authors highlight the new possibilities in terms of management of the railway networks due improved power quality and grid compliance due to the multilevel input voltage waveform and high apparent switching frequency seen from the grid side. The application of PETT to 3 kV DC rail traction means that the entire modular converter operates at much lower maximum voltage than in the case of the AC PETT, which encourages the integration of the propulsion inverter within the structure of the DC PETT with the use of unified low-voltage cells. The use of low-voltage (1.2 kV or 1.7 kV) SiC devices for this purpose seems to be an excellent solution.

The presence of built-in galvanic isolation in low voltage cells, realized utilizing MFTs, allows for series connection of the cells on the catenary side to obtain DC rail traction voltage and, independently, the configuration of the output terminals of the cells as a three-phase medium voltage multi-level inverter on the traction motor side. However, the use of low voltage power devices and electronics in combination with high insulation requirements, imposed by the application to 3 kV DC rail traction, is a challenging research topic regarding the insulation strength of the cells, in particular SiC power devices and MFTs.

The world's first and only traction unit equipped with the roof-mounted SiC-based 3 kV DC PETT is shown in Figure 2. It is the PESA 308 EN81 series electric passenger railcar (construction number 308B-007) with an originally rated power of 560 kW that operates in Polish regional passenger rail transport since 2007. The work presented in this paper covers some of the recent research and development efforts to develop, design, test, commission, and install of the 335 kVA (500 kVA peak) SiC-based 3kV DC PETT on the PESA 308 test traction unit for a field trial.

Figure 2. The EN81 series 3 kV DC electric passenger railcar used for the field trial with the roof-mounted SiC-based DC power electronic traction transformer (PETT) prototype.

2. Configuration of the 3 kV DC PETT Topology

The general description of the 3kV DC traction propulsion system with the SiC-based DC PETT is shown in Figure 3.

The key parts of the system include: nine power electronic cells (1) each consisting of eight commercially available 1.2 kV SiC MOSFET power modules (2) and medium frequency transformers (3) placed in separate air-cooled chambers; a compact input traction LCL filter of a small size has an area of a small chamber (4); a medium voltage asynchronous traction motor integrated with the gear unit (7). The DC PETT has, essentially, a three-stage construction: (1) DC input conversion stage; (2) AC output conversion stage and (3) AC-link, which is an especially designed medium frequency power transformer. The DC input conversion stage is used to adapt constant frequency DC traction voltage to a medium frequency required for conversion, while the AC output stage adapts medium frequency of the AC link to the output AC voltage useful for controlling the traction motor. The input terminals of the nine power electronic cells are connected in series which means that the DC PETT input stage is configured as a 19-level cascaded H-bridge four-quadrant converter (4QC) supporting the 3 kV DC railway traction network. The output terminals are connected in series, three pairs of terminals per phase, creating a three-phase output stage, which means that the traction motor is supplied by a three-phase seven-level cascaded H-bridge (CHB) traction inverter. Table 3 lists the overall system requirements and specifications.

The proposed SiC-based DC PETT takes full advantage of the SiC technology while meeting the requirements of train manufacturers. During DC PETT operation, the energy drawn from the 3kV overhead contact line is processed in discrete portions, with full DC voltage divided into 19 levels, which helps meet stringent electromagnetic compatibility (EMC) standards, including EN 50121-2, EN 50121-3-1, EN 50121-3-2 and EN 50238. The use of a cascade system of series-connected 1.2kV SiC MOSFETs to switch the full voltage of the railway traction enables a much higher operating frequency of the power converter than using HV counterparts. At the same time, the selection of low-voltage transistors with high switching frequency can provide noiseless operation with comparable or even smaller total switching losses of the power converter [19]. The internal terminals of the power electronic cells are configured as nine DAB DC-DC converters connected in series and forming the insulation

stage of the DC PETT. Each of the nine 4QC-DAB-DC/AC power electronic cells assembled in this configuration is rated for 38 kVA (56 kVA peak). Each cell, in addition to the galvanic isolation realized with the MFT, contains two energy storage elements, which is a characteristic feature of PET devices and enables the independent implementation of various control tasks at the input and output of the device.

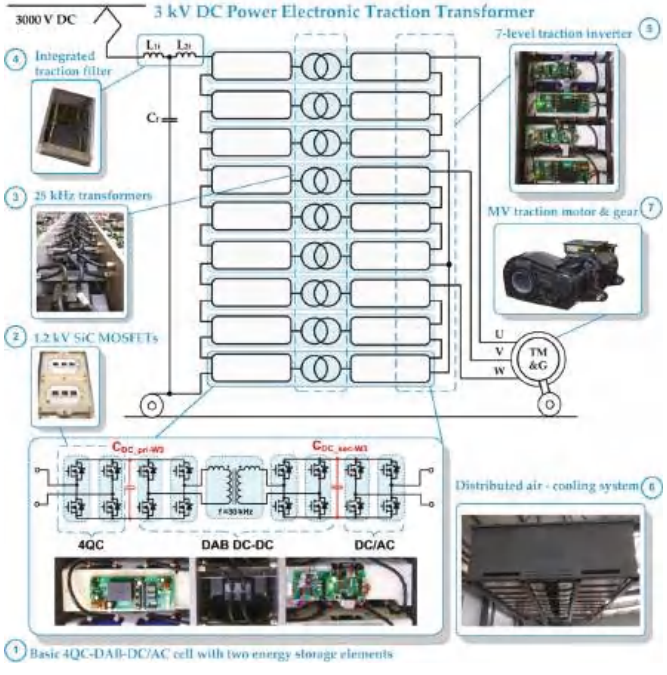


Figure 3. General scheme of the SiC-based 3 kV DC PETT: (1) Basic 4QC-DAB-DC/AC power electronic cell with two energy storage elements; (2) 1.2 kV SiC MOSFET power modules assembled in a 9 kV insulation frame; (3) medium frequency transformers; (4) compact input LCL traction filter; (5) output stage configured in the form of seven-level CHB inverter; (6) medium voltage traction motor integrated with the gear; (7) distributed air cooling system; U, V, W—traction motor phases.

Table 3. 3kV DC PETT system specification.

Parameter	Description
Input stage circuit structure	19-level 4QC
Output stage circuit structure	3 phase seven-level CHB inverter
Rated input voltage	3 kV V_{DC}/2.2 kV V_{AC}
Operating DC traction voltage	2 kV DC … 3.9 kV DC
Operating power	335 kVA
Rated output current	88 A (RMS)
Rated output frequency	60 Hz
LCL traction filter parameters	L_{1f} = 2 mH, L_{2f} = 1 mH, C_f = 10 µF
Filter inductors total weight	60 kg
MFT and DAB cells switching frequency	30 kHz
4QC cells switching frequency	20 kHz
CHB inverter cells switching frequency	20 kHz

As the heat generation is concentrated around the MFTs and SiC power modules, a distributed air cooling system (6), when uses PWM controlled fans and eighteen cooling ducts is provided in order to deal with the heat. The use of low voltage SiC MOSFETs makes the construction of the DC PETT more competitive in price than two-level traction inverters using HV SiC MOSFETS due to very high costs of high voltage semiconductor power devices, high voltage capacitors and other high voltage electronic components. The price of CAS120M12BM2-type 1.2 kV/193 A SiC MOSFET power module starts at about $300, the price of CAB450M12XM3-type 1.2 kV/450 A SiC MOSFET starts at about $700, while for the 3.3 kV nHPD2-type SiC MOSFET modules prices start at about $9500. The 10 kV and 6.5 kV SiC MOSFET power modules are not available on the market yet.

The modular construction of the DC PETT ensures even weight distribution on the roof of the EMU train. The center of gravity of the device is distributed symmetrically on both sides of the longitudinal axis of the vehicle. The distribution of the basic cells of the PETT on the EMU roof surface is shown in Figure 4. The operation of current-controlled nine-level four-quadrant converter connected to the 3 kV DC traction enables the minimization of the integrated input LCL traction filter and the mitigation of the resonances coming from the railway grid at a level that cannot be obtained in a conventional two-level inverter. As it can be seen from Table 3, for the investigated EN81 railcar, the weight of the traction filter chokes was reduced by nearly 10 times.

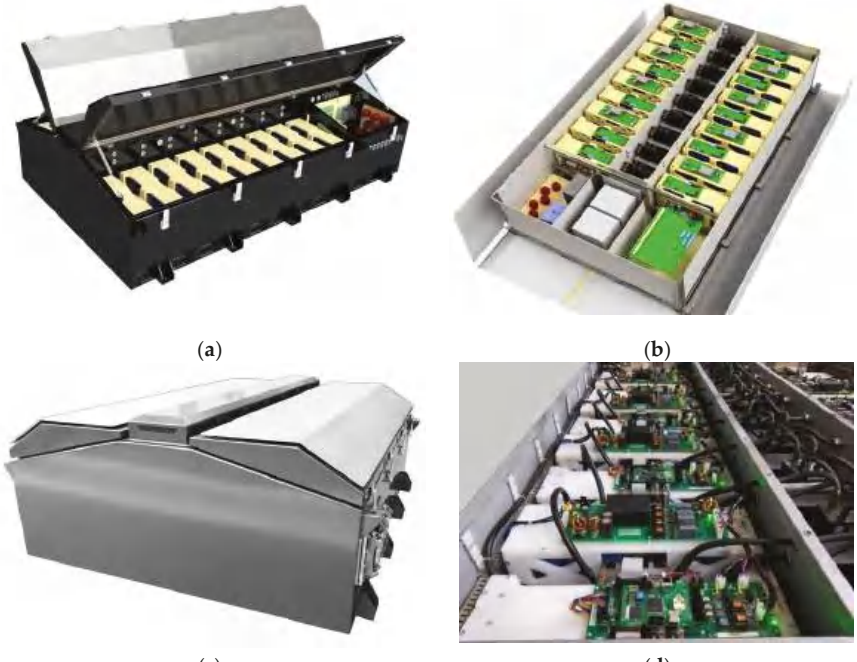


Figure 4. Assembly of power electronic cells of the DC PETT on the roof surface: (**a**) overall view of the whole device from the CAD program; detailed view of the 4QC-DAB-DC/AC power electronic cells and the LCL filter in the middle at the bottom (**b**); photos of the prototype (**c**) and (**d**).

Moreover, modular construction enables quick replacement of individual cells in case of failure. Therefore, the minimization of the MTTR (Mean Time to Repair), which is one of the basic indicators of reliability required in the railway industry [20,21] can be provided.

3. Low Voltage SiC Power Modules

According to numerous recent publications, e.g., [20,21], cascaded cells converter systems, such as the CHB topology, are a very attractive solution to interface power electronic systems to MVA-scale medium voltage applications. For the systems connected to medium voltage grids the choice of fast switching and low voltage drop 1.2 kV or 1.7 kV devices (giving up to 15 cells per phase stack) can be the most suitable trade-off between efficiency and power density, with efficiencies above 99% at a power density of about 5 kW/dm^3 [22].

Higher switching frequency obtainable at lower blocking voltages allows to reduce loss and volume contributions of the grid filter inductances and the cooling system.

With the wide availability of low voltage SiC MOSFET power modules on the market their performance in the range of maximum working currents offered is constantly increasing along with the progressive heat dissipation capacity. Figure 5 shows a comparison of the dimensions of the 1.2 kV SiC MOSFET power module, part no. CAS120M12BM2, used in this project, with a rated drain current of 138 A (T_C = 90 °C), $R_{DS(on)}$ = 23 mΩ, junction to case thermal resistance R_{thJC} = 0.125 °C/W, maximum dissipated power P_D = 450 W (T_C = 90 °C) characterizing commutation circuit series inductance of 15nH and a base surface of 65.4 cm^2, and new generation 1.2 kV SiC MOSFET power module, part no. CAB450M12XM3, available on the market from mid-2019, with 3 times higher rated drain current I_D = 409 A (T_C = 90 °C), $R_{DS(on)}$ = 4.6 mΩ, R_{thJC} = 0.11 °C/W, P_D = 750 W (T_C = 90 °C), and characterizing commutation circuit series inductance more than twice as low, L_{stray} = 6.7 nH and 36% less footprint.

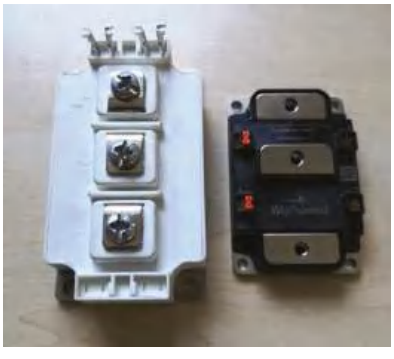
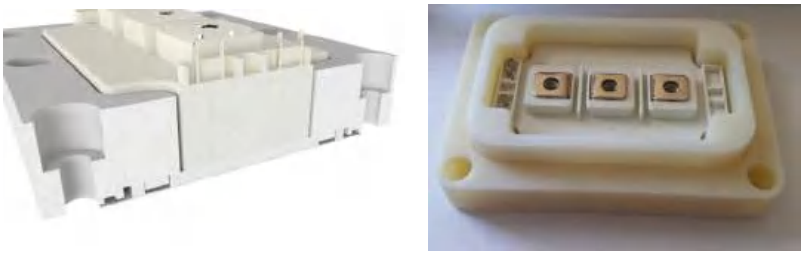


Figure 5. The 1.2 kV SiC MOSFET power module, part no. CAS120M12BM2, used in the project, with a rated current of 138 A (left) and a 36% smaller 1.2 kV SiC MOSFET power module, part no. CAB450M12XM3, with a rated current of 409A, available on the market from mid-2019.

The use of SiC MOSFET 1.2 kV power modules in the design of the proposed 3 kV DC PETT requires higher insulation strength than the original housing offers to withstand the full operating voltage of the converter. To increase the voltage strength, an additional frame made of insulating material has been developed and mounted between each transistor module and the heat sink, which is shown in Figure 6. A flexible, thermally conductive silicone film with thermal conductivity of 5 W/mK and a breakdown voltage of 9 kV AC was used between the base of the power modules and the heat sink.

There are several design challenges associated with switching performance of the SiC power modules which need to be carefully addressed including the minimization of ringing and overshoots caused by the parasitic loop inductance. These loop inductances together with SiC MOSFET output capacitance create a resonant tank, which is the source of unwanted EMI emissions [23,24]. To overcome the ringing, parasitic parameters converter should be minimized by a careful converter design.



(**a**) (**b**)

Figure 6. General view and cross-section of the frame of insulating material, ensuring increased voltage strength of the SiC MOSFET transistor module housing and heat sink insulation: (**a**) overall view from the CAD program; (**b**) photo of the prototype.

Figure 7 shows the drain-source voltage (U_{DS}) of the SiC MOSFET and the primary side transformer current of the developed DAB DC-DC converter measured in the developed SiC-based 3 kV DC PETT during commutation of 700 V DC voltage within 80 ns. A single standard PPA2124150-type, 1.5 uF snubber capacitor was attached to the DC bus of each SiC MOSFET power module. As can be seen in Figure 7, thanks to the obtained minimization of the switching loop inductance the measured magnitude of the voltage ringing is about 40 V (5.7%), which is an acceptable level.

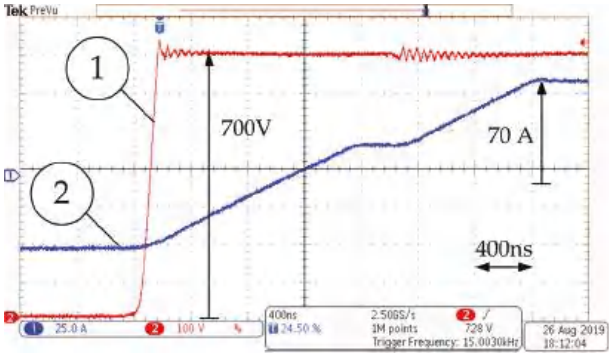


Figure 7. SiC MOSFET drain-source voltage (1), 100 V/div and the primary MFT current (2), 25 A/div of the developed DAB DC-DC converter during commutation of 700V DC voltage, 400 ns/div.

4. Design of MFT for 3kV DC PETT

The proposed 3kV DC PETT topology requires individual isolated DC-DC converters for the feeding of each H-bridge of the three-phase seven-level traction converter. The primary function is to provide galvanic insulation of each supply voltage [17]. The isolation stage is ensured by nine DAB DC-DC converters [25–32], which, in the same time, are core elements of the entire system (Figure 3). The main idea of the DC-DC DAB converter design is to combine the advantages of hard-switching pulse-width modulation (PWM) topologies characterizing a large dynamic range and no (reactive) circulating power operation and resonant topologies, which can operate in a soft-switching manner with a reduced electromagnetic interference (EMI) and effective utilization of transformer parasitics but, with strongly increased circulating power and a limited dynamic range.

The performance of DAB DC-DC converters and the entire DC PETT system is strongly affected by the design of the MFTs [26]. The key element enabling each DAB DC-DC converter to transfer energy between input DC stage and output AC stage is the series inductance L_s, which acts as a

decoupling element between the square-wave voltages and influences the conducted currents and switched currents of all the semiconductors of the active bridges of the DAB DC-DC converter. Series inductance can either be implemented as a separate component, using its own magnetic core, or can be built into the MFT. Using the MFT leakage inductance as the series inductance, $L_s = L_\sigma$, simplifies the mechanical design, eliminates the losses and volume resulting from the interconnection of the external inductor, and enables the achievement of higher power densities. However, in some justified cases, the use of additional auxiliary inductance may be unavoidable [33].

The insulation between the primary and secondary side of the MFT must withstand the rated voltage of the DC railway overhead line. Achieving the desired MFT design that will maximize power density and efficiency while maintaining space and weight restrictions requires a complicated optimization procedure [25]. Therefore the following considerations have been taken into account at the design stage:

- Interleaving of windings was not considered in order to avoid voltage isolation problems,
- The windings have been designed to provide very low coupling capacity between primary and secondary side to avoid capacitive coupling currents,
- The coil-formers have been designed in order to implement the required leakage inductance L_σ, at the same time to comply with minimum clearance and creepage distances to the core and to maximize the cooling surface of the windings.

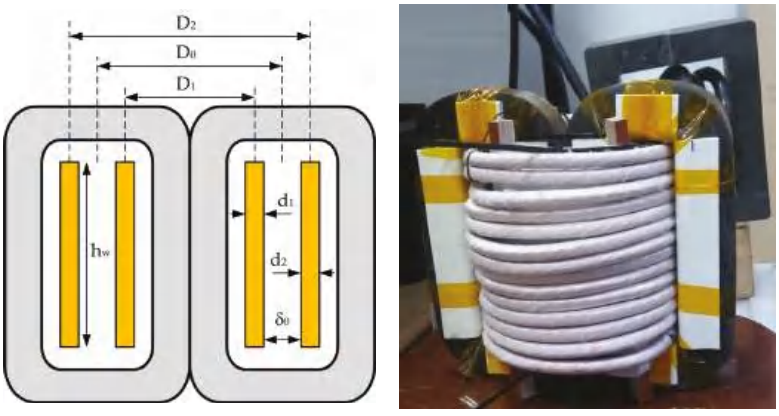
The working principle of the DAB DC-DC converter lies in the phase-shift δ, introduced between the rectangular AC voltages generated by the two active bridges [26,28]. The AC current flowing through the MFT is introduced by the phase shift of the active bridges AC voltages and depends on the difference of the primary and secondary DC voltages V_{dc1} and V_{dc2} and the value of the series inductance L_s. For rectangular AC voltages characterizing the same duty cycle $D = 0.5$, the transferred power P_{DAB} is adjusted by controlling the phase angle δ, according to the following formula:

$$P_{DAB} = \frac{V_{dc1} V_{dc2} |\delta| (\pi - |\delta|)}{2\pi^2 f_s L_s} \quad (1)$$

where L_s is the primary-referred leakage inductance [26]. In principle, the designed transformer had to meet the thermal requirements and insulation distances required to achieve the desired leakage inductance. To design and manufacture of two prototype transformers, two types of magnetic material, i.e., amorphous material characterizing high saturation level and N87 ferrite core have been used. Both materials, amorphous and ferrite, are suitable for high power and high-frequency applications and it can be of interest to investigate their performance on two transformer prototypes.

Figure 8 shows the dimensions of the windings and view of the first developed MFT prototype consisting of two high performance iron-based amorphous alloy (Fe-Cu-Nb-Si-B) wound cores with a rectangular shape (core length 222 mm, core width 118 mm, core height 30 mm, core build 35 mm). The classical shell-type structure with two uniform, concentric windings has been selected for the design. The leakage inductance has been set by arranging the position of the primary and secondary windings.

Uncut cores have been used, which can help reduce noise emissions from the transformer [27] and are valuable for rail vehicles. Moreover, the absence of an interlayer impregnation, which can be found in cut cores, eliminates additional mechanical stress to the lamination. Both, the primary and secondary windings consist of 1400 × 0.2 mm Litz-wire with 14 turns. As can be seen from Figure 8b, to facilitate the construction of the winding, plastic formers have been used. Since the magnetic core is uncut, an insulating tape was used to assemble the fragments of the former—so that they can be mounted around the central limb of the core.



(**a**) (**b**)

Figure 8. Main dimensions (**a**); and the overall view (**b**) of the first developed MFT with concentric windings of cylindrical shape (auxiliary inductor visible in the right top corner).

The leakage inductance of two uniform, concentric windings, of equal height, for which the leakage field inside the windings can be assumed to be axial, can be determined from Rogowski approximation method [34] using the mean length per turn for the whole arrangement of coils l_{m}:

$$L_\sigma = \mu_0 N_P^2 \frac{l_m\left(\frac{d_1+d_2}{3}+\delta_0\right)}{h_w} k_\sigma \tag{2}$$

where $\mu_0 = 4\pi \times 10^{-9}$ H/cm is the vacuum magnetic permeability, N_P is the number of turns in one winding, d_1 and d_2 are the radial sizes of internal and external windings, δ_0 is the width of the channel between the windings, h_{w} is the windings height and k_σ is Rogovskii's coefficient:

$$k_\sigma = 1 - \frac{d_1 + d_2 + \delta_0}{\pi h_w} \tag{3}$$

or, alternatively, using the area of reduced leakage channel S_L:

$$L_\sigma = \mu_0 N_P^2 \frac{S_L}{h_w} k\sigma \tag{4}$$

The area of the reduced leakage channel for concentric windings from Figure 8 can be calculated from [34]:

$$S_L = \frac{\pi}{6}\left(D_2^2 - D_1^2 + 2\delta_0 D_0\right), \tag{5}$$

where D_1 and D_2 are mean diameters of the primary and secondary winding and D_0 is mean diameter of the clearance ring between windings. Using k_σ, real concentric windings with height h_w are replaced by conditional windings of height h_{w}/k_σ, which reach the yokes. This permits one to replace a real leakage field that is not convenient for calculations with an ideal one in which all field lines are parallel to the winding axis [34]. For the developed prototype N_P = 14; h_w = 14.6 cm; D_1 = 9 cm; D_2 = 13.7 cm; D_0 = 11.4 cm; $d_1 = d_2$= 0.9 cm; δ_0 = 1.5 cm; k_σ = 0.92. Specifications of the first MFT prototype are listed in Table 4.

The first MFT prototype from Figure 8 has been operated with a DAB DC-DC converter. The dual phase-shift (DPS) control which uses the phase-shift between output voltages of the bridges along with the pulse width variation of both bridges output voltages has been applied to the DAB DC-DC converter. Although the applied DPS modulation helps to minimize the reactive power and thus

maximize the active power transmitted by the DAB DC-DC converter, the desired output active power of 40 kW could not be achieved due to too low obtained leakage inductance of the prototype transformer of about 5.5 µH per side. Hence, two auxiliary series inductors of 5 µH have been added to increase the resultant series inductance value and keep the transformer running at rated power.

Table 4. First MFT prototype specification.

Parameter	Description
Feeding voltage	$V_{DC1n} = V_{DC2n} = 700$ VDC
Output current	$I_{DC2} > 70$ A
Rated output power	40 kW
Operating frequency	20 kHz
Magnetic material	Amorphous alloy (Fe-Cu-Nb-Si-B)
Maximum induction	$B_{sat} = 1.56$ T
Specific Losses @ 0.1 T, 100 kHz	0.2 kW/kg
Diameter of a strand of a Litz wire	0.2 mm
Number of strands in a Litz wire	1400
Effective surface of a Litz wire	44 mm^2
Number of windings	$N_1 = N_2 = 14$
Leakage inductance (sum of primary and secondary)	$L_\sigma = 11.5$ µH
Auxiliary series inductors	5 µH (x2)

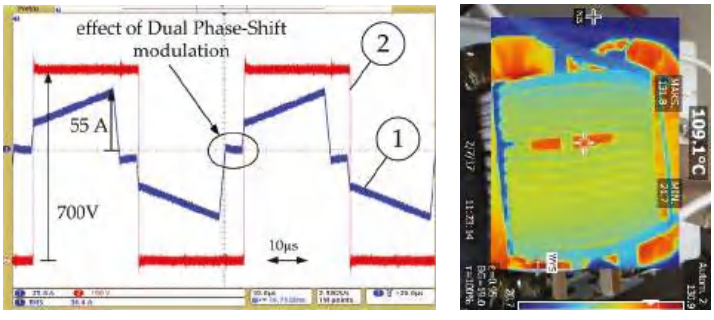
Thermal management to dissipate power losses is key to achieving high power density strongly required in the roof-mounted power electronic converters. During laboratory tests, particular attention was paid to the mechanism of formation of local temperature hot spots. In order to carry out transformer thermal measurements a thermal camera has been used to show the temperature distribution in the MFT. Figure 9a shows experimental waveforms of the developed first prototype transformer operating at half rated power: primary current and the collector-emitter voltage of the SiC MOSFET of the DAB DC-DC converter operating with 20 kHz switching frequency and the DPS modulation while Figure 9b describes the thermal characterization of the transformer operating without forced cooling at rated power of 40 kW. Excessive heating of the core was measured, which can be seen in Figure 9b. Local temperature increase far above 100 °C was observed during the tests, even at partial load, which was associated with: local heat-up of the core and the proximity effect losses in the transformer windings. The used laminated amorphous cores are wound from a strip of material of several tenths of micrometric thickness. Local heating of the amorphous alloy core was observed in the strip-end area, which was attributed to eddy current losses due to normal flux components in the zone of the amorphous strip-end. On the other hand, the reason for the observed proximity effect in windings was the time-varying flux density field in a conductor caused by a current flowing in another conductor nearby. Non-uniform current density of a conductor section, caused by the proximity effect, leads to higher effective resistance which in turn increases winding losses and the total MFT losses and is directly responsible for the hot-spot temperature gradients. The hottest observed places of the first prototype transformer occurred around the middle limbs of the transformer core and in the center of the primary winding, inside of the leakage layer. The maximal temperature of windings exceeded 109 °C while the maximum measured temperature of the core reached 200 °C in the strip-end area. Additionally, a disadvantageous fact was that the presence of two additional auxiliary inductors has significantly increased the volume of the magnetic circuit of the DAB DC-DC converter. For the above reasons, an improved version of the MFT was produced with a split planar litz-wire windings placed coaxially one above the another in the disc arrangement. Split windings construction enables obtaining a higher leakage flux density and correspondingly higher leakage inductance compared to the cylindrical transformer with the same number of turns [35]. In the disc type transformer the winding height h_w is measured in the direction of the core window width, while windings width d_1 and d_2 are in the direction of the core window height [26], which is shown in Figure 10. Therefore, the trapezoidal field distribution occurs in a direction perpendicular to the direction that occurred in

the first prototype with the concentric windings. In the second prototype the N87 ferrite material with four times lower saturation level was used, which required increasing the core cross-section A_c of the second prototype, according to the relationship below:

$$A_c = \frac{V_{rms1}}{k_f k_c N_1 B_m f_s} \tag{6}$$

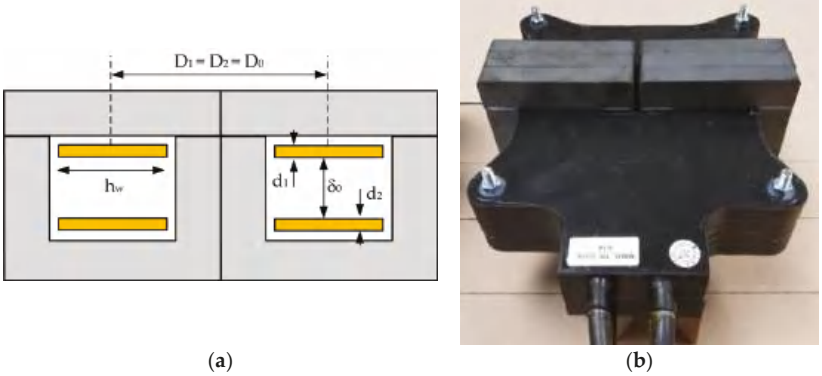
where V_{rms1} is the RMS value of the primary voltage, k_c is the filling factor of the core, N_1 is the number of primary turns, and f_s is the fundamental frequency. The coefficient k_f in Equation (6) depends on the duty cycle D of the phase shift modulation of the DC-DC DAB converter:

$$k_f = \frac{2\sqrt{2D}}{D} \tag{7}$$



(**a**) (**b**)

Figure 9. Primary MFT current i_{TR} (25 A/div) and drain-source voltage v_{DS} (100 V/div) of the SiC MOSFET of the DAB DC-DC converter operating with 20 kHz switching frequency and the DPS modulation (20 µs/div) (**a**); temperature measurement of the amorphous alloy core and observed heating of individual coils as a result of the proximity effect at rated power (**b**).



(**a**) (**b**)

Figure 10. Main dimensions (**a**); and the overall view (**b**) of the second developed MFT with a split planar litz-wire windings placed coaxially one above the another in the disc arrangement.

To minimize the desired A_c of the second MFT prototype, the switching frequency of the DC-DC DAB converter has been increased from 20 kHz to 30 kHz. Six pairs of U126/91/20 and I126/20 cores, i.e., three core stacks and litz wires comprised of 700 strands with a thickness of 0.2 mm have been used

in the second MFT prototype. The effective surface of the used litz wires is 22 mm^2. The transformers were placed in separate chambers inside the DC PETT housing and are cooled by air blown by fans. The used forced cooling enables the maximum permissible current density of 4 A/mm^2 [26] and the windings of the second prototype can carry a maximum current of 88 A. The used planar winding technology enables to adjust the leakage inductance of the transformer very precisely and reproducibly by using insulation distances between the primary and secondary windings.

The application of standard U-type and I-type ferrite core profiles for the core construction enables the use of prefabricated windings and supporting trays made of insulation material. To achieve isolation level of 9 kV, which is two times of the maximum DC-rail traction voltage level, casting the windings by the epoxy resin has been applied. The primary and secondary coils of the second prototype have the same height h_w, measured in the direction of the core window width. Hence it fulfils the precondition for the application of the method of Rogowski (Equation (2)) for prediction of leakage inductance [36]. Specifications of the second MFT prototype are listed in Table 5. Figure 10 shows the dimensions of the windings and view of the first developed MFT prototype.

Table 5. Second MFT prototype specification.

Parameter	Description
Feeding voltage	$V_{DC1n} = V_{DC2n} = 700$ VDC
Output current	$I_{DC2} > 70$ A
Rated output power	38 kW
Operating frequency	30 kHz
Magnetic material	N87 ferrite
Maximum induction	$B_{sat} = 0.4$ T
Specific Losses @ 0.1 T, 100 kHz	0.009 kW/kg
Diameter of a strand of a Litz wire	0.2 mm
Number of strands in a Litz wire	700
Efective surface of a Litz wire	22 mm^2
Number of windings	$N_1 = N_2 = 8$
Leakage inductance (sum of primary and secondary)	$L_\sigma = 24.5$ µH
Isolation voltage	$U_{Ni} = 9$ kV *

* The isolation voltage is defined as two times of the maximum DC-rail traction voltage level.

The windings were cast with a resin of good thermal conductivity and high mechanical strength, thanks to which the transformer can be placed in the so-called dirty area of the DC PETT housing. The final volume of the whole transformer is:

$$V_t = 307\ mm \times 270\ mm \times 131\ mm = 10.85\ dm^3$$

With a power density of 3.5 kW/dm^3 (≈5 kW/dm^3 peak). In order to carry out transformer thermal measurements a thermal camera has been used to determine the core and winding temperature distribution. The transformer has been running for 2 h at rated load. Figure 11 describes the thermal characterization of the transformer operating at a power of 45 kW without forced cooling.

In of the second MFT prototype, with the split windings, the dimension of both the primary and the secondary windings are equal, which provides presenting equal dc resistances, while in the first prototype with the concentric windings the length difference between interior and exterior windings was considerable. The realized 30 kHz MFT prototype has been successfully tested at various operating conditions in a full power rated DAB DC-DC converter, which will be presented in detail in Section 5.3.

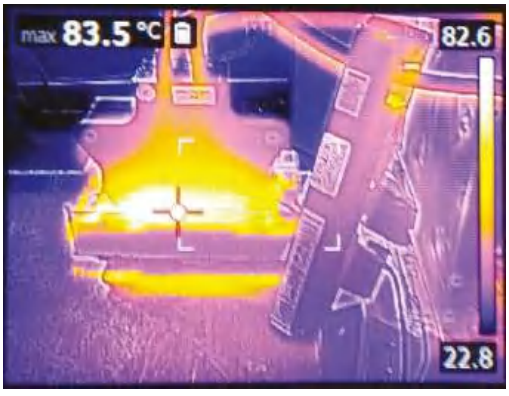


Figure 11. Temperature measurement of the second developed MFT with split windings at power of 45 kW without forced cooling.

5. Control Strategy and Controller Hardware

5.1. Main Control Tasks

As mentioned in Section 2, DC PETT carries out independent control tasks at its output and input, which consist in precisely generating the PWM voltage supplying the traction motor and maintaining full control over the current drawn from the railway overhead contact line. The PWM voltage which feeds the asynchronous motor must be generated in accordance with current tasks of the drive system: control of the electromagnetic torque, which determines the driving dynamics, and control of the magnetic excitation of the motor, which determines the energy consumption.

5.2. Control of the 19-Level H-Bridge 4QC

The presence of galvanic isolation in the DC intermediate circuit and two energy storage elements in each of the power electronic cells, enables independent control of the SiC MOSFET H-bridges on the primary (railway traction) side and secondary (traction motor) side. As mentioned, the nine SiC MOSFET H-bridges of the DC PETT input stage are connected in series and configured as 19-level H-bridge 4QC ensuring a low ripple amplitude of the current drawn from the 3 kV DC overhead contact line. Each H-bridge of the input stage has a capacitor at the output, which plays a role on the DC voltage source: $v_{\mathrm{DC\_pri\text{-}U1}}$, $v_{\mathrm{DC\_pri\text{-}U2}}$, ⋯ , $v_{\mathrm{DC\_pri\text{-}V1}}$, ⋯ , $v_{\mathrm{DC\_pri\text{-}W3}}$ for nine individual DAB DC-DC converters. The proposed control scheme of the DC PETT input stage is illustrated in Figure 12.

The 19-level H-bridge 4QC controller has two closed control loops: the voltage controller to deal with the primary DC voltage $v_{\mathrm{DC\_pri}}$ of the nine SiC MOSFET H-bridges and the current controller for the purpose to control the input current i_{L2f}. The set value for the voltage controller is the desired DC voltage value at the individual capacitors of the H-bridges. The voltage regulator amplifies and integrates the deviation between the voltage set point on a single capacitor and the average value of the voltages measured across the capacitors of all H-bridges. The voltage regulator output signal is the set point value to the current regulator. The output of the current regulator corrected by the actual value of the traction voltage $v_{\mathrm{DC\_traction}}$, measured on the traction current collector, constitutes the set signal to the PWM modulator. The control method described in [36] was used to control individual SiC MOSFET H-bridges of the 19-level 4QC from Figure 12. The essence of the operation of the entire 19-level H-bridge 4QC is that the energy from individual capacitors $C_{\mathrm{DC\_pri\text{-}U1}}$, $C_{\mathrm{DC\_pri\text{-}U2}}$, ⋯ , $C_{\mathrm{DC\_pri\text{-}V1}}$, ⋯ , $C_{\mathrm{DC\_pri\text{-}W3}}$ is transferred through isolated DAB DC-DC converters to the three-phase seven-level CHB traction inverter supplying the traction motor. The energy flow from primary DC capacitor of the input H-bridge through the DAB DC-DC converter to the output H-bridge of the

U, V or W phase of the CHB traction inverter reduces the voltage on this capacitor. During each control program execution sequence, the individual H-bridges of the input stage, whose intermediate DC circuit voltage reaches the lowest values, are activated, causing the primary DC capacitors to charge and the voltage on these capacitors to rise. The sequence of switching individual cells on and off depends on the current DC voltage levels of individual capacitors C_{DC_pri-U1}, C_{DC_pri-U2}, ... , C_{DC_pri-V1}, ... , C_{DC_pri-W3}. On the other hand, in the case of energy recuperation, the bridges with the highest voltage value on the DC capacitors are connected to the overhead contact line.

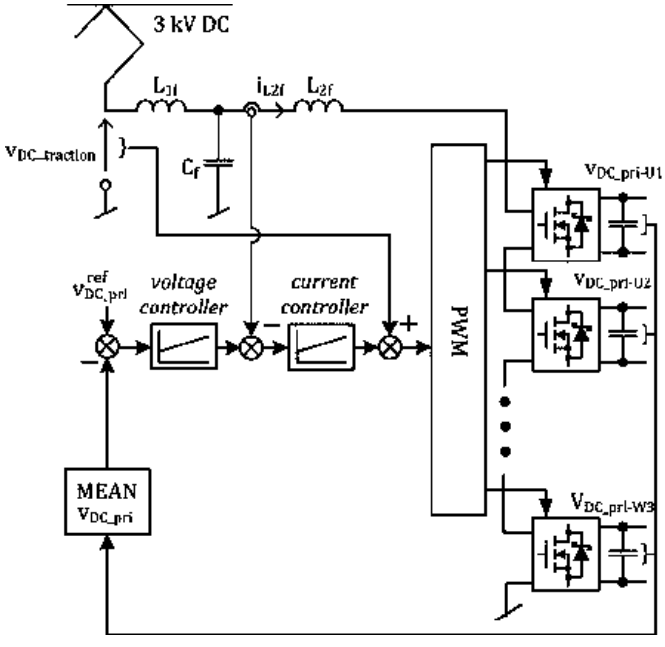


Figure 12. The overall control scheme for the DC PETT input stage.

All the electronic circuits of the 4QC-DAB-DC/AC power electronic cells are designed with the floating ground. The ground planes of the electronic circuits of each 4QC H-bridge shown in Figure 12 is connected to the middle points of the DC-links adjacent H-bridges through the resistive dividers. These resistive dividers acts simultaneously as the bleeder resistors for the DC-link capacitors of the power electronic cells. Thanks to this, the full voltage appearing on the electronic circuits will never exceed several hundred volts and the use of optically isolated op-amps with maximum working insulation voltage of 1 kV is sufficient. All electronic circuits are powered from the train's on-board 24 V DC auxiliary power converter via isolated DC-DC power supplies. These isolated DC-DC power supplies must be able to withstand the full voltage of the 3 kV DC overhead traction line. The measurement of the DC traction voltage $v_{DC\_traction}$ required in the control system from Figure 12 is performed using voltage divider placed on a separate insulated electronic board. Measured signal is transmitted to the MASTER controller via optical fiber. The voltage measurement electronic board is supplied by the on-board 24 V DC auxiliary power converter via an isolated DC-DC power supply. By using high-voltage insulation of the cable connecting the L_{1f} and L_{2f} input filter chokes, the i_{L2f} input current measurement is performed using a conventional current transducer. The measuring signal from the current transducer is transmitted directly to the MASTER controller interface board.

5.3. Control of DAB DC-DC Converters

As can be seen from Figure 3 in Section 2, nine DAB DC-DC converters are used to transfer the electrical energy between the primary DC links ($C_{DC\_pri\text{-}U1}$, $C_{DC\_pri\text{-}U2}$, ... , $C_{DC\_pri\text{-}V1}$, ... , $C_{DC\_pri\text{-}W3}$) of the 19-level 4QC and the secondary DC links ($C_{DC\_sec\text{-}U1}$, $C_{DC\_sec\text{-}U2}$, ... , $C_{DC\_sec\text{-}V1}$, ... , $C_{DC\_sec\text{-}W3}$) of the three-phase seven-level CHB traction inverter. Individual DAB DC-DC converters are controlled independently and no information exchange about the control process with the 19-level 4QC, seven-level CHB traction inverter and other DAB DC-DC converters is needed. The single DAB DC-DC converter is shown in Figure 13. The control system of the DAB DC-DC converter is designed to obtain the same voltages on the primary DC-link capacitor and secondary DC-link capacitor $v_{DC\_sec} = v_{DC\_pri}$. As a result, each DAB DC-DC converter equalizes the individual DC-link voltages of the 19-level 4QC and the seven-level CHB traction inverter [36].

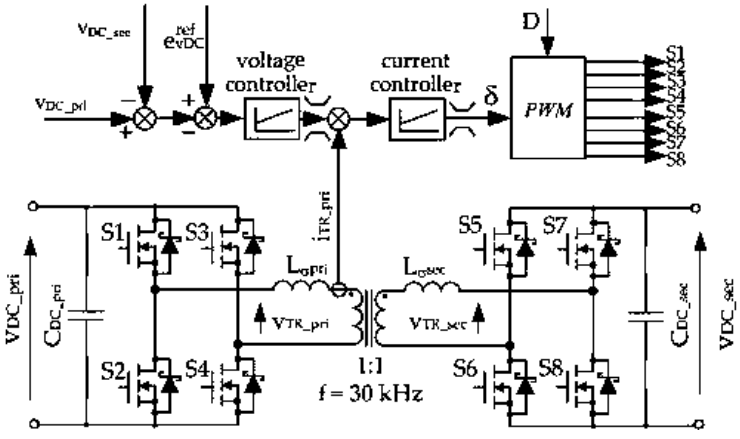


Figure 13. The single DAB DC-DC converter and its control system.

The DC voltages: v_{DC_pri} on the primary side and v_{DC_sec} on the secondary side are converted into high frequency rectangular pulses v_{TR_pri} and v_{TR_sec}, with constant ($D = const$) or modulated ($D = var$) pulse width. The transferred power depends on the mutual phase shift ratio δ between primary and secondary voltages v_{TR_pri} and v_{TR_sec}. For simple phase-shift control transferred power P_{DAB} is defined by (1). Tests in the DAB DC-DC converter with the second MFT prototype were done at 640/640 V and powers of 10 kW, 38 kW and 45 kW for switching frequency of 30 kHz and a dead time 500 ns. Figure 14a shows the characteristic waveforms of the developed DAB DC-DC converter operating at rated power of 38 kW: the primary transformer current i_{TR_pri} (25 A/div), the primary transformer voltage v_{TR_pri} (500 V/div) and the secondary transformer voltage v_{TR_sec} (500 V/div). Figure 14b shows the impact of the dead time on the time duration of the voltage pulses of the primary and secondary transformer voltages v_{TR_pri} and v_{TR_sec}. Although both voltages are controlled with the same constant value of the duty cycle $D = 0.96$, the voltage pulses of the secondary voltage v_{TR_sec} are longer than voltage pulses of v_{TR_pri}. It can be seen from Figure 14, that in the time period when $v_{TR\_pri} = v_{TR\_sec} = 0$ there is no resultant voltage forcing the dynamics of the current and the dynamics of transformer current changes decreases for a fraction of a microsecond. This phenomenon was also recorded when the tested DAB DC-DC converter was operated with a reduced power of 10 kW (Figure 15a). After applying the correction of the duty cycle and taking into account the dead time effect, the above did not occur any more—which can be seen in Figure 15b describing the primary and secondary transformer voltages and current of the DAB DC-DC converter operating with a power of 45 kW.

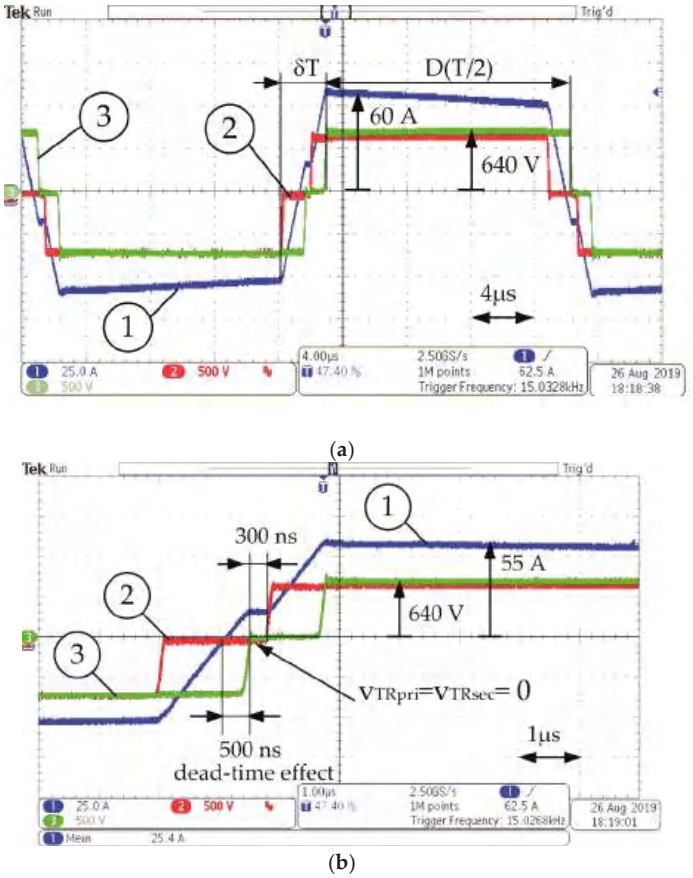


Figure 14. Measured waveforms of the DAB DC-DC converter with the second MFT prototype: primary transformer current i_{TR_pri} (1), 25 A/div; primary voltage v_{TR_pri} (2), 500 V/div; secondary voltage v_{TR_sec} (3), 500 V/div at the rated load. Time scale 4 µs/div. (**a**) and 1 µs/div. (**b**).

Figure 15a shows the characteristic waveforms of the developed DAB DC-DC converter operating at partial power of 10 kW: the primary transformer current i_{TR_pri} (25 A/div), the primary transformer voltage v_{TR_pri} (1 kV/div) and the secondary transformer voltage v_{TR_sec} (1 kV/div). Figure 15b shows the primary transformer current i_{TR_pri} (50 A/div), the primary transformer voltage v_{TR_pri} (1 kV/div) and the secondary transformer voltage v_{TR_sec} (1 kV/div) for the DAB DC-DC converter with the second MFT prototype overloaded with a power of 45 kW. The efficiency of the DAB DC-DC converter has been calculated using the voltages and currents measurements and the math functions of the digital oscilloscope Tektronix DPO4104. The measured resistances of the primary and secondary windings of the MFT was 11 mΩ and 12 mΩ, respectively. The experimental efficiency results are presented in Figure 16. The developed DAB DC-DC converter characterizes peak efficiency above 98 % and has efficiency around 97.5 % in a wide range of the output power.

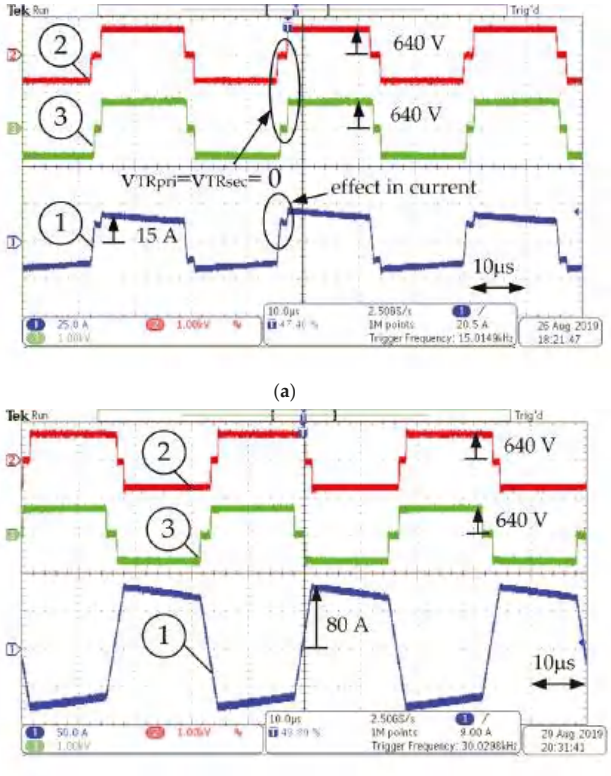


Figure 15. Measured waveforms of the DAB DC-DC converter with the second MFT prototype: primary transformer current i_{TR_pri} (1), 25 A/div; primary voltage v_{TR_pri} (2), 500 V/div; secondary voltage v_{TR_sec} (3), 500 V/div at partial power of 10 kW (**a**) and the corresponding waveforms at power of 45 kW (**b**).

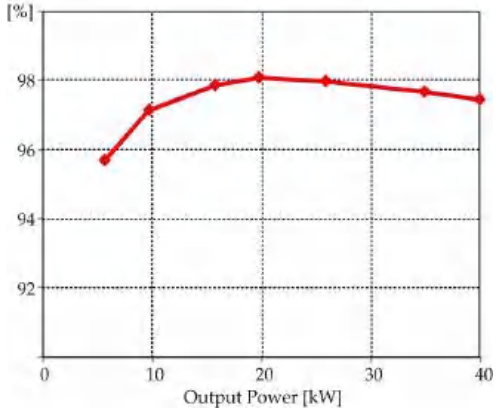


Figure 16. Measured efficiency versus output power of the DAB DC-DC converter with the second MFT prototype.

5.4. Control of Seven-Level CHB Traction Inverter

As it can be deduced from Figure 3, the seven-level CHB traction inverter is composed of three H-bridges connected in series in any of the phases. The traction inverter is controlled using space vector PWM (SVPWM) by successively activating one H-bridge per phase until the reference voltage vector is reached [36]. The CHB topology enables the operation with advantageously high modulation indexes of individual H-bridges. The DC links of the individual H-bridges are coupled with nine DAB DC-DC converters. If the obtained output voltage is different from the reference motor voltage, the next H-bridge is activated in each phase. At each switching sequence only one H-bridge per phase provides a modulated output voltage, while the others are negatively/positively connected or bypassed [37]. Since their transistors do not switch, they do not generate commutation loses. For the above reason, the control system can consider the topology of the seven-level CHB converter as a set of 3 three-level CHB converters connected in series, which simplifies the control strategy. Each of them is then composed using three H-bridges (one H-bridge in each phase of the inverter) and can be controlled using simple SVPWM patterns [37].

5.5. Control of the Traction Motor

The precision of PWM voltage generation resulting from the seven-level topology of the three-phase traction inverter and the adopted transistor switching frequency of 20 kHz, allows the use of advanced traction motor control algorithms, not previously used in rolling stock. The multiscalar model based control [38,39] has been used to control the torque and excitation of the traction motor. According to the multiscalar model concept, the motor torque is defined as the state variable instead of the current vector component in the q axis that occurs in conventional Field Oriented Control (FOC). The complete multiscalar model (or *natural variables* [40]) of the induction motor is received after the nonlinear transformation of the stator current and rotor flux vector components occurring in the classic vector model. The multiscalar variables of the induction motor model are selected as follows:

$$x_{11} = \omega_r, \tag{8}$$

$$x_{12} = \psi_{r\alpha} i_{s\beta} - \psi_{r\beta} i_{s\alpha}, \tag{9}$$

$$x_{21} = \psi_{r\alpha}^2 + \psi_{r\beta}^2, \tag{10}$$

$$x_{22} = \psi_{r\alpha} i_{s\alpha} + \psi_{r\beta} i_{s\beta} \tag{11}$$

where $i_{s\alpha}$, $i_{s\beta}$, $\psi_{r\alpha}$, $\psi_{r\beta}$ are the stator current and rotor flux vector components, x_{11} denotes traction motor rotor speed, x_{12} is proportional to electromagnetic torque, x_{21} is square of the magnitude of rotor flux vector and represents the excitation of the traction motor, and x_{22} is a multiscalar variable with no direct physical interpretation and proportional to the reactive power consumption. Figure 17 shows the basic structure of the multiscalar model based control system for the traction motor. The rotor fluxes $\psi_{r\alpha}$, $\psi_{r\beta}$, rotor speed (8) and remaining multiscalar variables (9)–(11) are estimated in a speed observer. The variables estimated in the speed observer denoted by Λ are used in the control system. Nonlinear feedback is applied to the system of first-order multiscalar model equations obtained from nonlinear transformation of the multiscalar model [38,39].

The approach of using the multiscalar variables (8)–(11) instead of *d*–*q* components of the stator current and rotor flux vectors, advantageously eliminates the need for continuous synchronization of the rotating reference frame with the rotating rotor flux vector, which is absolutely required in the FOC method. The use of the linearizing feedback allows to obtain a linear relationship between the outputs and inputs of the multiscalar model and enables decoupled control of the mechanical subsystem of the induction motor, related to the dynamics of the shaft rotational speed x_{11}, and the electromagnetic subsystem, related to the dynamics of the square of the rotor flux vector module x_{21}. Hence, the x_{21} reference value for the control system from Figure 17 can be modulated according to

the arbitrary chosen efficiency optimizing formulation, which ensures the improved efficiency of the traction drive [40]. A detailed analysis of the multiscalar control of the traction motor is beyond the scope of this article and will be discussed in more detail in the forthcoming papers.

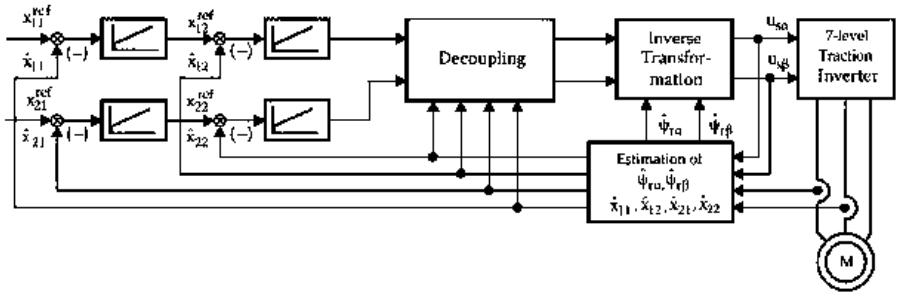
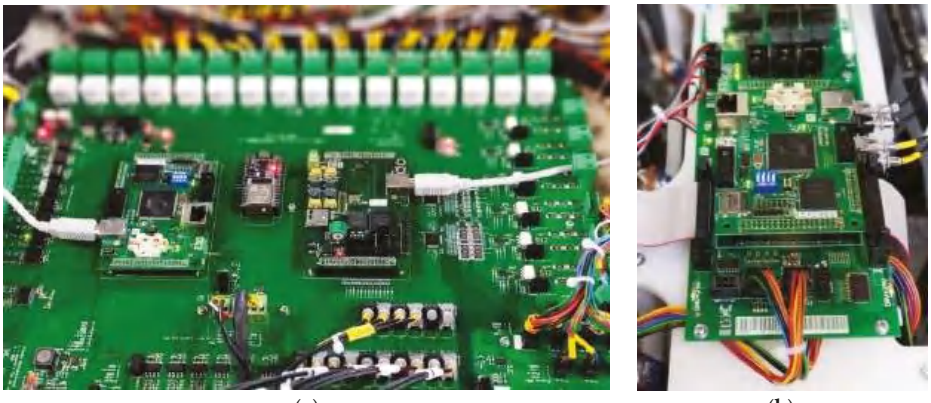


Figure 17. The basic structure of the multiscalar model based control system for the traction motor.

5.6. Controller Hardware

For implementing the proposed control strategy a DSP-based MASTER controller board and ten ARM processor-based SLAVE controller boards have been designed as shown in Figure 18 with the features of advanced functionalities and fast execution time. As shown in the Figure 18a, the MASTER controller board consists of a digital signal processor (ADSP-21363) control card, including a FPGA (FPGA-CYCLONE II EP2C8F256) and additional ARM Cortex-M4 32b processor (STM32F407IGT6) control card. The ADSP-21363 floating-point signal processor (3 Mb SRAM, 333 MHz, 2GFLOPS) implements the traction motor torque and excitation control, and the traction line current and voltage control, while the STM32F407IGT6 processor (MCU + FPU, 210DMIPS, 1MB Flash/192 + 4KB RAM, USB OTG HS/FS, Ethernet) realizes human-machine interfacing (HMI) and the communication with other STM32F407IGT6 ARM Cortex-M4 32b processors of nine power electronic cells.



(**a**) (**b**)

Figure 18. MASTER controller board consisting of main ADSP-21363 based control card and the auxiliary STM32F407IGT6 Arm Cortex based control card (**a**); one of nine STM32F407IGT6 Arm Cortex based SLAVE controller boards controlling nine 4QC-DAB-DC/AC power electronic cells (**b**).

The DSP-based MASTER controller board receives the measurements from 4QC-DAB-DC/AC power electronic cells and implements the traction motor control and traction line voltage and current

control algorithms. The FPGA receives the input DC voltage and three-phase output voltage commands from the DSP and implements the PWM algorithm and outputs nine command signals to ARM-based SLAVE controller boards, shown in Figure 18b, via optical fibers. The individual ARM-based SLAVE controller boards receive a command from the MASTER controller board and implement PWM times and outputs gate signals to the transistors. Ten SLAVE controller boards output gate signals to 72 SiC MOSFET dual power modules. To ensure complete isolation between the input stage and the output stage of the DC PETT, one SLAVE controller controls the SiC MOSFET H-bridges of the input sides of the two 4QC-DAB-DC/AC power electronic cells, while the other SLAVE controller controls the transistor bridges of the output sides of these two 4QC-DAB-DC/AC power electronic cells. Both SLAVE controllers communicate with each other using fiber optics.

The MASTER controller board and all SLAVE controller boards contain signal conditioning circuits designed to receive individual voltage and current sensors signals and send them to the DSP or ARM processors respectively. The isolated communication interfaces are realized by a serial Controller Area Network (CAN) interface port.

The overall MASTER control commands of the DSP can be received in two modes: from the driver's console in the train driver's cab (train running mode) and from the operator's PC through the DSP CAN port (service mode). The execution period of one cycle of the control scheme in the main DSP is 150 µs, while the FPGA on the MASTER control card works with a three times shorter execution period of the PWM algorithm. Individual FPGAs on SLAVE controller boards operate with the execution period equal to 33.33 µs. The accuracy of the PWM time counting on the SLAVE controller board results from the used 150 MHz clock.

The control relay outputs on the main-board shown in Figure 18a are used to control the train's individual switching devices, such as the circuit breaker circuit or the contactor circuits in the on-board high-voltage switchgear.

6. On-Track Testing

The developed DC PETT prototype for the railway applications has been assembled as shown in Figure 4 in Section 2. Due to the direct availability of the 3 kV DC railway network on the railway siding, a number of experiments were conducted with the developed DC PETT prototype mounted on the roof of the EN81 series electric passenger railcar shown in Figure 2 in the introductory section. During the tests, only one drive set of the traction motor powered by the developed 3kV DC PETT was running, which made it possible to obtain measurement results specifically for one complete drive system. The second traction motor of the EN81 series electric passenger railcar was not running during the tests. Due to the limitation of the track length, the maximum achievable speed during the experiments was, however, limited and did not reach the operating speed of 120 km/h given by the manufacturer of the rail vehicle. The route of the test runs with a length of 600 m on the Bydgoszcz-Towarowa railway siding used during on-track testing is shown in Figure 19.

Figure 19. The route of test runs with a length of 600 m on the Bydgoszcz-Towarowa railway siding.

Specifications of the DKLBZ 0910-04 type traction motor of the EN81 series electric passenger railcar are listed in Table 6.

Table 6. DKLBZ 0910-04 type traction motor specification.

Parameter	Description
Rated stator voltage	U_{sN} = 2200 V
Rated stator current	I_{sN} = 88 A
Rated power	P_N = 300 kW
Rated torque	M_N = 1506 Nm
Power factor	$\cos\varphi_N$ = 0.89
Efficiency	η = 94.3%
Max. voltage during breaking	U_{sMAX} = 2300 V
Max. power during breaking	P_{break} = 320 kW
Max. torque	M_{MAX} = 2160 Nm

The results of the track test run on 600 m railway siding are shown in Figure 20. The recorded waveforms were saved on a PC connected to the DSP-based MASTER controller card via USB.

Figure 20 illustrates recorded waveforms during accelerating of the train with the DC PETT based asynchronous traction drive to the speed of 45 km/h and immediate braking. Before the connection of the DC PETT to the overhead traction line voltage there is no energy stored in the DC PETT and all DC links are empty. Similar to AC PETT reported in [19], initial charging is performed from the DC side utilizing the startup resistor that is bypassed later on. Moreover, the developed DC PETT has a second mode of pre-charging the intermediary circuits from the on-board battery bank using a set of DC-DC converters. The latter mode enables the DC PETT to be connected to the overhead traction line without any inrush current.

Referring to Figure 20, after the train pantograph is on, the uncontrolled voltage on each of the primary DC links equals the overhead line voltage divided by nine. Then, after starting DC PETT, the primary DC-link voltage is controlled to 520 V and the secondary DC-link voltage is controlled to be equal primary DC-link voltage. During DC PETT operation the input current drawn from the overhead traction line is controlled according to the control scheme shown in Figure 14. In all experiments, the power recovered during braking was transferred back to the traction network. As can be seen from Figure 20, the delivery of braking power of the order of 200 kW to the traction network did not significantly change the voltage of the traction network.

Figure 21 shows the characteristic traction motor stator current and the PWM output voltage waveforms obtained during three different operation modes of the DC PETT. Figure 21a shows the stator current waveform during start-up and the acceleration of the traction motor (50 A/div; 1 s/div). Thanks to the use of high-performance torque control, mentioned in Section 5, the stator current magnitude is limited at the desired value and its amplitude does not exceed 100 A at all times.

As can be seen, there are no undesirable oscillations in the current waveform. Figure 21b shows the stator current waveform during the final braking phase of the train from 15 km/h until the train stops (50 A/div; 1 s/div). Figure 21c shows the stator current and the PWM voltage at the DC PETT output in the steady-state operation of the traction motor (50 A/div; 1 kV/div; 10 ms/div). As it is shown in Figure 21c, the applied three-phase, seven-level CHB topology provides an almost sinusoidal PWM voltage, which has not been demonstrated in any other 3kV DC rail traction inverter so far. By using CHB technology, the instantaneous maximum value of the voltage switched by the SiC MOSFET transistors does not exceed a few hundred volts. At high switching speeds of SiC MOSFET transistors, this will significantly facilitate compliance with the stringent requirements of railway electromagnetic compatibility (EMC) standards, which will be the focus of the planned continuation of the work carried out by the authors.

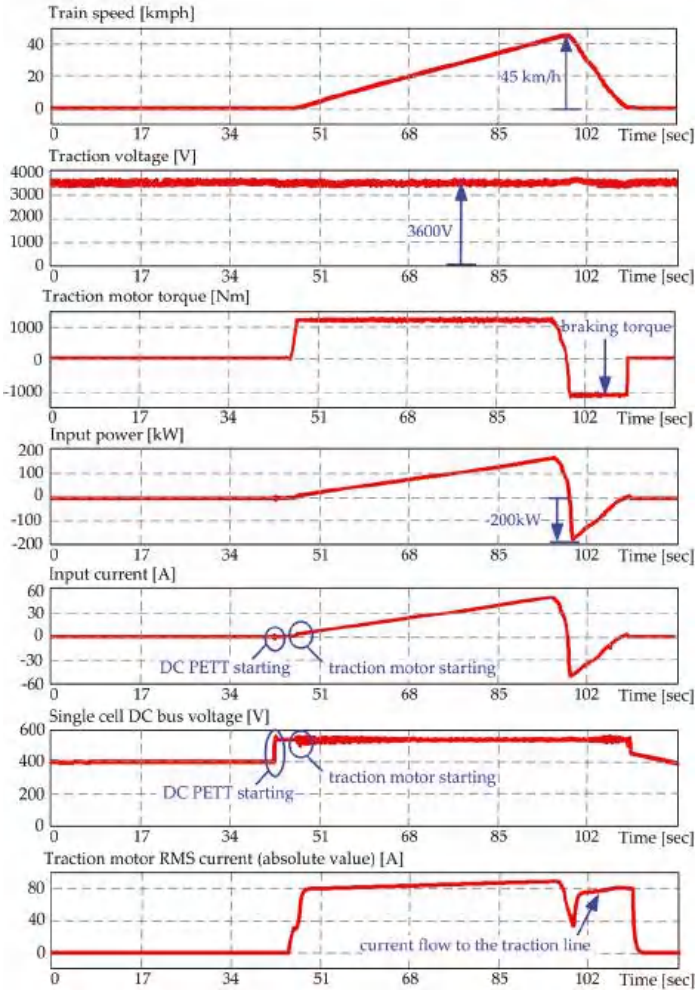


Figure 20. Track test results: Recorded waveforms during start-up of the train with the DC PETT based asynchronous traction drive to a speed of 45 km/h and immediate braking. Top to bottom: (1) train speed; (2) traction motor torque; (3) DC PETT input power; (4) DC PETT input current; (5) traction DC voltage; (6) primary DC bus voltage of a single 4QC-DAB-DC/AC power electronic cell.

The efficiency of the SiC-based 3kV DC PETT prototype has been measured. As in [19], the power consumption of the auxiliary converters supporting the cooling system and the control system has not been included in the efficiency calculations. The plots of efficiencies versus output power are shown in Figure 22.

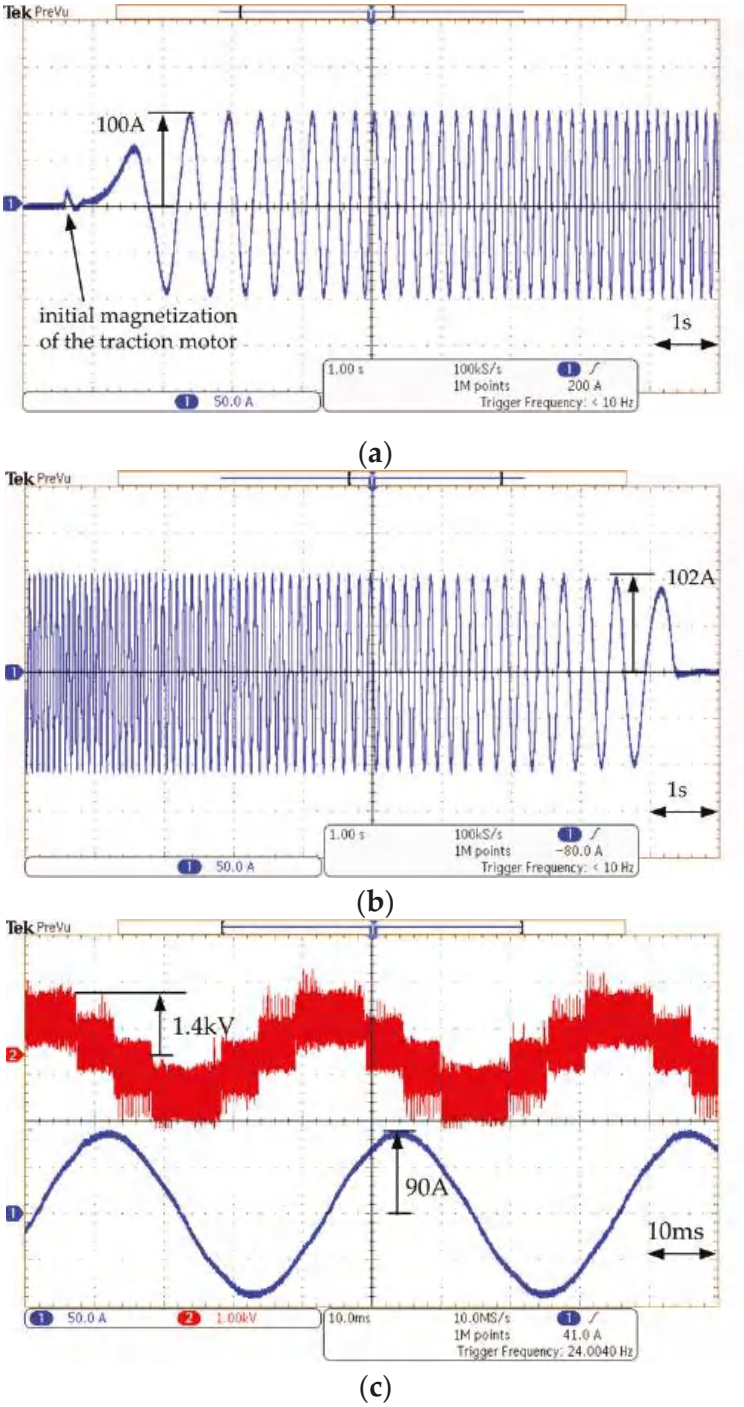


Figure 21. Traction motor stator current and output PWM voltage waveforms obtained during three operation modes of the DC PETT: start-up and acceleration mode (**a**); braking (**b**); phase voltage and phase current of the traction motor steady-state operation (**c**).

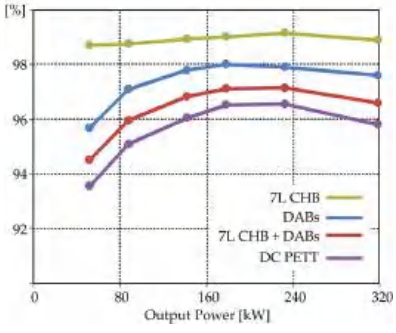


Figure 22. Measured efficiency versus output power of the three power stages and the entire 3kV DC PETT prototype.

As can be seen from Figure 22, the three-phase seven-level CHB traction inverter (7L CHB), considered separately, characterizes peak efficiency around 99%, which is comparable to the corresponding SiC based MV multilevel CHB inverters constructed from low-voltage SiC MOSFET transistors, presented in the literature [22]. The efficiency of the 4QC input stage is slightly higher than that of the seven-level CHB traction inverter, because when cascaded H-bridges operate with a constant voltage of 3kV DC overhead traction line, actually only two SiC MOSFETs work in each H-bridge. However, thanks to the use of the full H-bridges in the DC PETT input stage instead of half bridges, it is possible that the developed SiC-based DC PETT can also work with an AC input voltage, as is the case with multi-system locomotives. However, the operation of the proposed SiC-based DC PETT in an AC voltage system is beyond the scope of this paper and will be the subject of future publications. As can be seen in Figure 22, the isolation stage ensured by nine DAB DC-DC converters has the greatest impact on the efficiency of the entire SiC-based DC PETT. The SiC-based DC PETT prototype has an efficiency of around 96% in a wide range of output power and the peak efficiency around 96.5%.

7. Conclusions

The design and development of the SiC-based DC PETT intended for EMUs operated in 3 kV DC rail traction have been presented in this paper. The developed DC PETT has been implemented into the PESA 308 EN81 series electric passenger railcar that operates in Polish regional passenger rail transport. The conducted experimental tests during train runs on the trial confirm the full functionality of the developed device.

As with the MV PETT for AC traction [19], the proposed DC PETT offers a number of advantages that make it very attractive for rolling stock operating in 3 kV DC traction. First of all, in the era of widespread striving to design highly efficient and ultra-quiet drive converters from SiC semiconductor devices, the proposed solution has a number of advantages if one compares it to high-voltage SiC traction inverters with a classic design being currently at the stage of analyzes and preliminary tests. Conventional two-level voltage source traction inverters of the working voltage in the catenary 3 kV DC would contain SiC MOSFET transistors with a voltage blocking of 6 kV, and the conventional three-level inverter voltage would contain SiC MOSFET transistors with a voltage blocking of 3 kV. It is already known that obtaining high voltage switching frequencies SiC MOSFET above 5 kHz is energy inefficient and the management of electromagnetic disturbances at such high switched energies is quite a challenge. The component modules of the proposed DC PETT, in the form of nine 4QC-DAB-DC/AC power electronic cells, are made with the use of low-voltage SiC technology (1200 V). The applied high switching frequency: 30 kHz to 1.2 kV SiC MOSFETs used in DAB DC-DC converters and 20 kHz to 1.2 kV SiC MOSFETs used in SiC MOSFET H-bridges of the

input and output stage, do not cause as significant energy losses as it would be in the case of high voltage (>3 kV) SiC MOSFET technology. The applied high switching frequency allows for favorable elimination of noise from the converter operation. Moreover, the use of multi-level topology made it possible to follow the command voltage from the control system with very high precision and, therefore, enables the application of the high precision control of the traction motor. Moreover, compared to classical topologies, the applied active input stage with the regulator of the current drawn from the overhead line enables the minimization of the input LC filter and, thus, minimization of the total volume and cost, which the authors intend to make the subject of detailed analysis in future publications.

The MFT design path, discussed in detail in the article, shows that the important factors influencing the power density of the developed transformers are the provision of appropriate insulation gaps to ensure galvanic isolation at the level of 9 kV DC and the provision of structural gaps between the windings to obtain the desired transformer leakage inductance. In the case of the traction drive investigated in the paper, with a relatively small power of 325 kVA (500 kVA in peak), the power density of the designed 38 kW MFT was 3.5 kW/dm^3 (≈5 kW/dm^3 peak). This allows the authors to reasonably hope that for a higher power MFT, the power density obtained will also be higher. At the present stage, it is difficult to compare the power density of the developed 3kV DC PETT prototype with a built-in lightweight LCL input traction filter with 3 kV DC roof-mounted traction inverters available on the market because the solutions known to the authors have a heavy external traction filter mounted in a separate container, which is not taken into account by manufacturers to estimating the power density of the traction converter. The developed 3kV SiC-based DC PETT prototype, thanks to the built-in 4QC power input stage, is immediately ready for cooperation with the AC traction network in a multi-system EMUs. The proposed modular DC PETT structure, composed of the same repeatable power electronic cells, could ensure lower maintenance costs, short inspection and repair times for potential faults, and thus high availability - required in the rolling stock.

Author Contributions: Conceptualization, M.A.; software, J.S.; validation, M.A., J.S.; investigation, M.A., J.S.; writing—original draft preparation, M.A.; writing—review and editing, M.A., J.S.; visualization, M.A.; All authors carried out the theoretical analysis and contributed to writing the paper. All authors have read and agreed to the published version of the manuscript.

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Feasibility Study GaN Transistors Application in the Novel Split-Coils Inductive Power Transfer System with T-Type Inverter

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Abstract: A promising solution for inductive power transfer and wireless charging is presented on the basis of a single-phase three-level T-type Neutral Point Clamped GaN-based inverter with two coupled transmitting coils. The article focuses on the feasibility study of GaN transistor application in the wireless power transfer system based on the T-type inverter on the primary side. An analysis of power losses in the main components of the system is performed: semiconductors and magnetic elements. System modeling was performed using Power Electronics Simulation Software (PSIM). It is shown that the main losses of the system are static losses in the filter inductor and rectifier diodes on the secondary side, while GaN transistors can be successfully used for the wireless power transfer system. The main features of the Printed Circuit Board (PCB) design of GaN transistors are considered in advance.

Keywords: wireless power transfer; inductive power transmission; multilevel converter; AC-DC power converters; T-type inverter; GaN-transistors; electromagnetic coupling

1. Introduction

Interest in inductive wireless power transmission is constantly growing due to the increasing interests of both low-power wireless chargers for mobile and wireless charging stations of medium and high power for electric bikes and electric vehicles. Such chargers transfer the electric energy wirelessly from primary to secondary inductor by means of inductive coupling [1]. Inductive wireless power transfer systems consist of a transmitting part (contains an inverter, compensation circuit and primary inductor) and a receiving part (receiving inductor, compensation circuit, rectifier) [1]. The researchers have already analyzed the main possible topologies of compensation schemes, their advantages and disadvantages, and described the general recommendations for their implementation. It is well known that Wireless Power Transfer (WPT) systems have some limitations, such as short transmission distance(centimeters or dozens of centimeters at acceptable levels of transmission efficiency) [2,3], sensitivity to the exact positioning of the receiving coil relative to the transmission coil [2,4], size and cost of the system.

Among existing limitations, the issue of the size and cost of the WPT system is one of the most important. Researchers are still looking for the optimal system configurations and topologies of power converters that would best meet the above requirements.

Different types of switches are utilized in the power electronics converters [5–8]. The conventional Insulated Gate Bipolar Transistors (IGBTs) are gradually going out of use in industrial circuits of WPT systems due to their low switching capability [9]. The reverse blocking voltage capability of the conventional IGBT is very low; there are relatively large power losses [10]. It is well known that the use of wideband gap semiconductors (such as GaN-transistors) instead of classical Si power switches can significantly reduce the power losses that lead to the increasing of the system efficiency or significantly increase switching frequency reducing size of passive elements [11–13]. It is advisable to use GaN transistors for T-type topologies [5–8,14]. The GaN features fast switching, low parasitic charges, reverse conductivity with zero recovery charge and low driving power losses and dynamic losses; compared to Si-IGBTs and SiC-MOSFETs [5,6,15–18], higher efficiency, low parasitic output capacitance [16–18] can be achieved. The advantage of GaN over Si is mostly visible at higher frequencies in dynamic losses [15,19]. However, the conduction losses are comparable with the SIC semiconductors [18,19].

The main goal of the article is to study the feasibility of GaN transistor application in the proposed non-traditional (non-classical) WPT system. This will be based on the loss analysis of the main components of the circuit.

The paper, consisting of seven sections, proposes a new solution of the wireless power transfer system based on two parallel single-phase T-type GaN-based invertors (dual T-type inverter) with two transmitting coils on one ferrite core (coupled transmitting inductances). The case study system description and advantages of such solution are represented in Section 2 of the paper. According to previous research [20], more than 70% of the losses in WPT systems for various cases of power, loads and working frequencies depend on semiconductors and inductors [20,21]. Therefore, the contribution of such parameters was taken into account in calculations in this paper. Confirmation of the advantages of the proposed solution, made mainly by power losses analysis, described in Sections 3–5. Sections 3 and 4 proposes the losses models of the GaN transistors and coil inductors, respectively. Simulation and experimental verification of the proposed solution is described in Section 5, with conclusions and list of patents devoted to the proposed WPT system on Sections 6 and 7, respectively.

2. Case Study System Description

Figure 1 depicts the proposed circuit of a multi-level converter for WPT. The primary converter consists of a full-bridge three-level T-type inverter connected to bidirectional auxiliary semiconductor switches. The GaN-based T-type inverter is first proposed for use in a WPT system together with two coupled inductors. It provides a number of advantages over existing analogues.

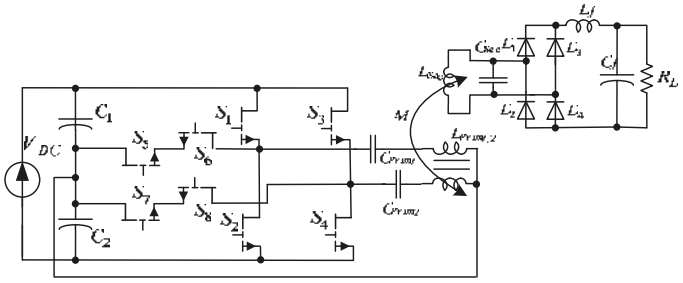

Figure 1. Proposed Inductive Power Transfer IPT converter.

The DC source is applied to the T-type inverter. The energy is transmitted to the secondary side through the primary coils with an air gap (Figure 1). The output current is rectified by the passive full-bridge rectifier, filtered and supplied to the load.

In the scheme, V_{dc} is the source of the input dc voltage; C_1, C_2—input capacitors; S_1–S_4—switches of the single-phase full-bridge inverter; S_5, S_6 and S_7, S_8—auxiliary bidirectional switches; $L_{prim1,2}$—coupled primaries inductances; C_{prim1}, C_{prim2}—primaries compensating capacitances; L_{sec}—secondary inductance; C_{sec}—secondary compensating capacitance; D_1–D_4—bridge rectifier; C_f—filter capacitor; L_f—filter inductance; R_L—output resistive load.

First of all, the multi-level inverters have a number of advantages over conventional H-bridge inverters, including better Electromagnetic Compatibility EMC and higher efficiency [14,22–24], which are extremely important for wireless power transmission systems [24]. However, analysis of the existed publications shows that using of multi-level inverters for WPT systems are just at the beginning stage [25].

Each multi-level circuit has its advantages and disadvantages, but among these types, T-type has some advantages over other types: smaller size, simpler operation principles, lower THD, lower conduction losses and smaller number of semiconductors [10,14,23]. The most important advantage of T-type solution in the WPT application is that only half of dc-link voltage applied to the primary side coil which in turn reduces the primary inductance and size of the coil [14]. The equation (1) for calculating the primary inductance L_{prim} at SP compensation analytically confirms this fact [20]:

$$L_{\mathrm{P}rim} \approx L_{Sec}\left(\frac{8}{\pi^2 k_{nom}}\frac{V_{in}}{V_{out}}\right)^2, \quad (1)$$

where L_{sec}-secondary side self-inductance, k_{nom}—nominal coupling, V_{in} and V_{out}—input and output voltages, respectively.

Finally, the splitting of the transmitting coils will reduce the conduction and overall diameter of the primary inductance. The application of two coupled transmission coils of inductance on a single ferrite core reduces the total dimensions of the magnetic components on the primary side (and the losses in copper and ferrite). Multiple magnetic resonant coils lead to higher transmission efficiency and longer transmission distances [26]. In addition, the coupling coefficient between them is considered constant, which simplifies certain calculations of the system. Furthermore, this solution reduces the current through each coil. This leads to a lower overall resistance of the transmission coils, which, in turn, increases the Q factor and the energy transfer efficiency.

It is expected that wireless power transmission systems based on of multi-coil circuits with GaN-based T-type inverters in the transmission part is a promising solution, joining the advantages of the parts which already existed. The proposed solution does not have any heatsinks, has reduced the size of primary coils and can be considered for industrial application. Such a system can be used directly in power supply systems for transmission on different power levels.

Compensating capacitors are required to compensate the leakage inductance on the primary and secondary sides in the WPT systems. In this case, the possible distance between the coils increases [2]. Systems with Series-Parallel (SP) compensation work efficiently with a wide range of loads in addition to the advantages for middle-power and low-power applications and allow reducing dimensions of the receiver coil [20]. Series-Series (SS) compensation does not depend on the change of magnetic coupling and load. These compensation topologies are most widely used for wireless charging. This solution is very well investigated; its benefits and drawbacks are well known [2,27–29].

3. Losses Models of the GaN Transistors

The main sequence of the calculations is presented in this section and Section 5. Initially, the control signals and the shape of voltage and current signals in the inverter were derived from simulation and are used for calculations of power losses in semiconductors.

3.1. T-type Inverter Operation Mode

Two auxiliary switches S_5 and S_6 (Figure 1) are turned on in the T-type topology (Figure 2). Switching states and the voltage are shown for the 3-level T-type Neutral Point Clamped NPC inverter in Table 1 for Figure 1 (for one leg).

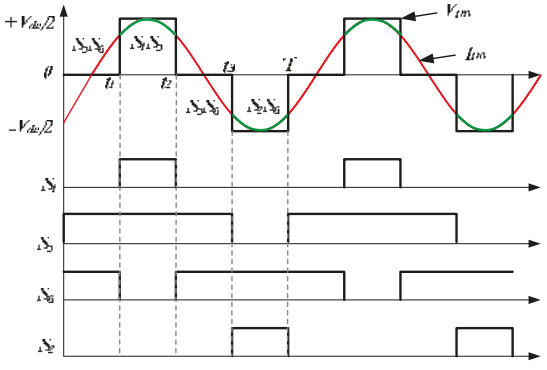

Figure 2. Control signal sequences and shapes of the voltage and the current of the IPT converter. Static losses are calculated, knowing the current through each transistor at a certain interval.

Table 1. Switching States and Voltage for the 3-Level T-Type NPC Inverter [23].

Level	S_1	S_5	S_6	S_2	Voltage
Positive (+)	1	1	0	0	$+V_{dc}/2$
Neutral (N)	0	1	1	0	0
Negative (−)	0	0	1	1	$-V_{dc}/2$

Figure 2 shows the control signal sequence of the transistor (shown for one phase), the voltage (V_{Inv}) and the inverter output current (I_{Inv}).

3.2. Losses Model of the GaN Transistor under Compensation Condition

It is well known that the conduction losses are a significant component to estimate the total losses in the transistors [19]. In addition, the dynamic losses in GaN transistors should be taken into account.

The total transistor power losses are determined by the sum of the static and dynamic losses [17].

$$P_{Total} = P_{Cond} + P_{Dyn}, \tag{2}$$

where P_{Cond}–static losses (conduction losses), P_{Dyn}—dynamic losses.

The equation that determines the conduction losses (when the transistor is fully on) is as follows:

$$P_{Cond} = {I_{Drms}}^2 + R_{DS(on)}, \tag{3}$$

where I_{Drms}–rms current value through drain, $R_{DS(on)}$—on-resistance of a transistor's drain-source.

The current I_{Drms} is determined at each interval (Figure 2) for the positive half wave as follows:

$$I^2_{S1S5} = \frac{1}{T}\int_{t1}^{t2} (i_m \sin(\omega t))^2 dt, \tag{4}$$

where i_m—amplitude value of drain current, ω—angular frequency, T—period. For the negative half wave:

$$I_{S2S6}^2 = \frac{1}{T}\int_{t3}^{T}(i_m \sin(\omega t))^2 dt. \tag{5}$$

Two sections are defined for the zero state (Figure 2):

$$I_{S5S6}^2 = \frac{1}{T}\int_{t0}^{t1}(i_m \sin(\omega t))^2 dt + \frac{1}{T}\int_{t2}^{t3}(i_m \sin(\omega t))^2 dt. \tag{6}$$

Currents are added from all sections and multiplied by the resistance of the transistor over a period of time due to (3) to calculate the conduction losses of the transistor.

Total dynamic power losses [17]:

$$P_{Dyn} = P_{SW(on)} + P_{SW(off)} + P_G + P_{rcl} + P_{oss} + P_{RR}, \tag{7}$$

where $P_{SW(on)}$ and $P_{SW(off)}$—switching losses, P_G—gate charge losses, P_{rcl}—power loss due to the reverse conduction voltage through the body diode; P_{RR}—reverse recovery loss; P_{OSS}—power loss due to the output capacitance.

Gate charge power losses of a transistor:

$$P_G = Q_G + V_{dr} f_{sw}, \tag{8}$$

where Q_G—total gate charge of a transistor, V_{dr}—driving voltage, f_{sw}—switching frequency.

The equations show, that charge losses are increasing at high switching frequency.

Reverse recovery loss is caused by the charge stored in the junction of the internal body diode of a transistor in the T-type inverter [19]:

$$P_{RR} = Q_{RR}\frac{V_{In}}{2} f_{sw}, \tag{9}$$

where Q_{RR} is the reverse recovery charge, V_{in}—input voltage of the inverter. In the transistor datasheet, GaN transistors do not contain the internal body diode, so, reverse recovery loss is not present in these devices.

Power losses due to the output capacitance [17] are the following:

$$P_{OSS} = f_{sw}\int_{0}^{Vin}(V_{DS} C_{OSS}(V_{DS}))dv_{DS}, \tag{10}$$

where C_{OSS}—output capacitance of the transistor (determined by the dependencies in the datasheet). These losses are independent of power and are insignificant at the increase of power, but the contribution of this type of losses is significant at low power and high switching frequency.

The power losses due to the reverse conduction voltage through the body diode (or dead-time losses):

$$P_{rcl} = V_{REV} I_D t_{dead} f_{sw}, \tag{11}$$

where t_{dead}—length of the dead-time (reverse diode conduction time), V_{REV}—reverse voltage drop in a GaN transistor.

The exact equations from [17,19], take into account several values (values of switching time, level of corresponding voltages, etc.) from the simulation data or the experimental data. It is not possible to accurately determine the switching time of the transistors from the model in PSIM and at high frequency. The approximate switch-on time is 4.9 ns, the switch-off time is 3.4 ns according to the

datasheet. At the same time, the duration of the on- and off-transistors of each of the shoulders in the model is much larger.

Therefore, a simplified equation is used to estimate the magnitude of switching losses quantitatively [18]:

Turn-on switching losses of a transistor:

$$P_{SW(on)} = \int_0^{t\_rise} (V_{DS} I_D) dt, \tag{12}$$

Turn-off switching losses of a transistor:

$$P_{SW(off)} = \int_0^{t\_fall} (V_{DS} I_D) dt, \tag{13}$$

where t_{rise} and t_{fall}—transistor's time for turn-on and turn-off (values from datasheet), V_{ds}—drain-source voltage, I_D—drain current.

According to [19], at frequencies below 100 kHz, switching losses of transistors are very low. Switching losses are increasing at frequencies up to 500 kHz but they have no significant effect on the total loss estimation [19]. Thus, most transistor losses are conduction losses and power losses due to the output capacitance.

3.3. Losses Model of Rectifier Diode Losses

The losses in rectifying diodes are also significant, especially at high switching frequency and high current through diodes. The parameters of high-speed Schottky diodes were used for modeling and in the experimental verification.

It is known that the static losses in a diode are determined by the current flow through the diode multiplied by the voltage drop across the diode. Two diodes simultaneously conduct current in the case of a diode bridge:

$$P_{Cond.D} = 2 I_{forv} V_{drop}, \tag{14}$$

where I_{forv} is the forward current value through the diode, V_{drop}—voltage drop per diode.

Dynamic losses in the diode are switching losses. All diodes in the diode bridge are involved in the process of rectification. If a Q_{RR} value (this is the reverse recovery charge) is given in the datasheet, then the equation is as follows:

$$P_{SW\_D} = 4 Q_{rr} V_{rev} f_{sw}. \tag{15}$$

Reverse recovery charge value is defined as a product of $C_{junction}$ (junction capacitance) by V_{rev} (the reverse voltage on the diode). The result in (16) is obtained by substituting this product into Equation (15):

$$P_{SW\_D} = 4 V_{rev}^2 C_{junction} f_{sw}. \tag{16}$$

The total losses in all semiconductors in this scheme are higher than the losses in the transmitting and receiving coils.

4. Design and Losses Models of Coils Inductors

Coupled primary coils were calculated with a nominal value of 90 μH each and a receiving coil with a nominal value of 24 μH (Table 2).

Table 2. Parameter Table for Experiments.

Symbol	Description	Value
V_{in}	Input voltage	300 V
S_1-S_8	GaN transistors	GS66508T
F_{sw}	Switching frequency	150; 200 kHz
C_{sn}	Snubber capacity	100; 470 pF
D_1-D_4	Rectifying diodes	RB228NS100TL
$L_{prim1,2}$	Primary inductances	90 µH
L_{sec}	Secondary inductance	24 µH
k	Coupling coefficient	0.7; 0.9

4.1. Design of the Transmitter and Receiver Coils

The simulation was performed in almost the same order as described in [4]. The model of coils was carried out in ANSYS Electrimagnetic Suite and designed using the Finite Elements Modeling (FEM) method. The transmission coils are on the top and the receiving coil is on the bottom (Figure 3).

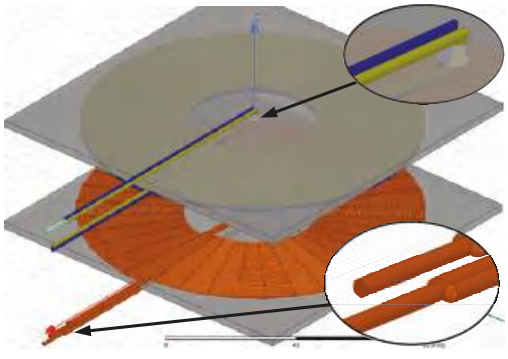

Figure 3. Designed model of coils for WPT.

The primary coil consists of two coils connected in parallel at one lead. One end of the coil pins is drawn through a hole in the ferrite. They do not interfere with the coils as close as possible to each other and do not distort the magnetic flux with this solution. Both primary coils have equal turns each. They are arranged in two layers, one above the other. This solution reduces losses in copper and ferrite and also the total dimensions of the magnetic components on the primary side. Multiple magnetic resonant coils lead to higher transmission efficiencies and longer transmission distances.

The secondary coil consists of double turns (shown in the figure with an enlarged fragment) in one layer. Coil winding with double turns reduces the coil's own resistance at the same value of the inductance itself and increases the quality factor. It increases also the maximum current that the secondary coil misses.

4.2. Losses Model of the Coils Inductors under Compensation Condition

Certain simplifications are allowed in the calculations of losses in the inductors. It is quite a complex mathematical problem to determine the core losses and eddy current losses, especially including the skin and proximity effects of inductors [30]. It is not always possible to achieve acceptable accuracy of calculations even when those losses are determined. The challenges are caused by the complex physical nature of these phenomena.

The core is mainly intended for shielding the magnetic induction flux in the WPT system [4]. Losses in the core are determined by the modified bulky Steinmetz equation at non-ideal sinusoidal voltage [20,30]. However, it is difficult to determine the ferrite coefficients for the equation since an experimental procedure is needed for a specific material under right conditions with high quality equipment. These factors are given rarely by the manufacturer. Therefore, determination of the value of core losses by other methods for this material is not accurate and has no scientific validity.

Most of the available FE tools do not support Litz wire modeling. In addition, magnetic field H differs from turn to turn at determining the proximity effect [4]. Hence, H must be evaluated in the center of each turn individually to calculate the proximity loss for each turn [20]. Conduction losses are usually added to this value at determining a skin effect [20,30]. The Litz wire reduces the skin effect and proximity effect significantly. Furthermore, the proximity effect is minimal between the transmitting and the receiving coils due to the large air gap.

The value of DC conduction losses is sufficient to understand the effect of the geometrical parameters of the coils on the losses value in transistors and coils.

Conduction (ohmic) losses in the primary coils:

$$P_{Lprim12} = {I_{Lprim\_rms}}^2(2R_{Lprim}), \tag{17}$$

where I_{Lprim_rms}—current through primary coils; R_{Lprim}—resistance of one primary coil. Both paired transmitting coils are the same and have the same resistance in this case.

Conduction losses in the secondary coil are as follows:

$$P_{L\,\mathrm{sec}} = {I_{L\,\mathrm{sec}\_rms}}^2 R_{L\,\mathrm{sec}}, \tag{18}$$

where I_{Lsec_rms}—current through the secondary coil.

Power losses in the primary coils mostly depend on the inverter current, together with the own resistance of the primary coil.

5. Results of Experiments and Simulation

An experimental model was made to check the feasibility of using GaN transistors in the described scheme (Figure 4). Transistors GS66508Twere used with maximum drain current of 30 A, maximum drain-to-source voltage 650 V, drain-to-source on resistance at 25 °C equal to 50 mΩ. The transistor has zero reverse recovery loss, fast fall and rise times, low inductance and low thermal resistance in a small package. The GS66508T is a top-side cooled transistor that offers very low junction-to-case thermal resistance. Transistors are located at the bottom of the Printed Circuit Board (PCB) without additional radiators. These features combine to provide very high efficiency of power switching.

The PCB consists of four copper layers, divided into signal and power parts. In the signal part of the board top and bottom layers are devoted for signal traces and internal layers for power supply voltage and ground polygons. In contrast, all layers, external as well as internal, are used for power traces. Some special techniques were used on the PCB aiming increase the efficiency and decrease power losses. First of all, high-current power traces were repeated on all four layers and stitched with via matrix to reduce parasitic resistance of such traces. GaN transistors, as it was mentioned above, were placed on the bottom side of the board in accordance to the producer's recommendations [31]. Taking into account that GaN transistors can operate on high frequencies, EMC considerations was implemented on the board. Image of the bottom side of the board with power GaN transistors and other components of one half of T-type circuit is shown on Figure 5. It should be noted that component designators on Figure 5 corresponds to designators on Figure 1. Highlighted components representing current flow in the circuit for switching states marked as "*Positive* (+)" in the Table 1. As it can be seen, such placement of the components on PCB provides as low as possible square of current loops.

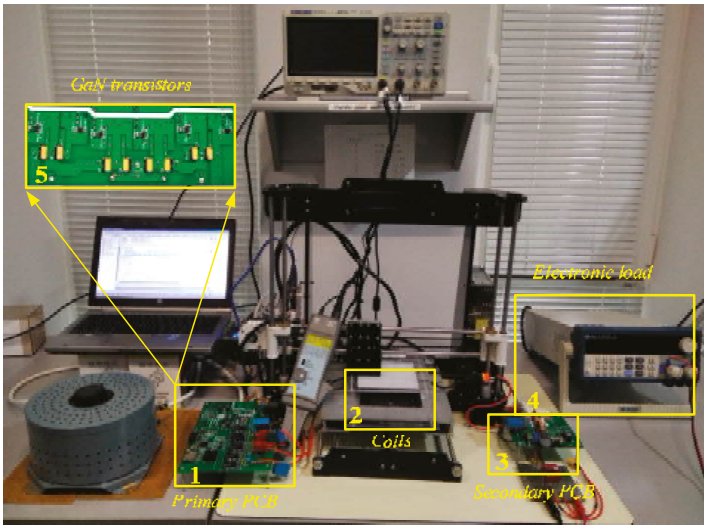

Figure 4. Experimental laboratory GaN-based WPT system: (**1**)—primary side Printed Circuit Board (PCB); (**2**)—transmitting and receiving coils; (**3**)—secondary side PCB; (**4**)—electronic dc load; (**5**)—GaN transistors located on the bottom of the primary PCB.

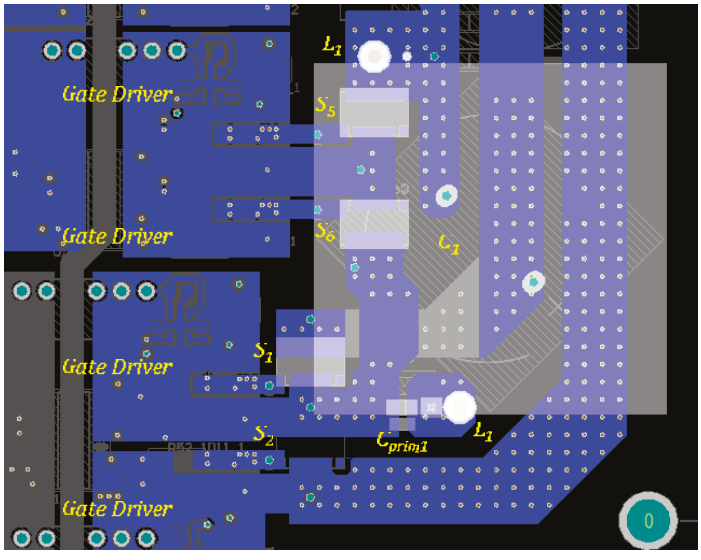

Figure 5. Bottom side of the power part of primary PCB.

The similar square of current loops on PCB are also provided for other switching states, presented in the Table 1. Therefore, such small squares of the current loops in all possible operation modes of the inverter provide low electromagnetic interferences of the power converter, improving EMC of WPT.

The experiments were performed at a distance between the coils of 1 cm (coupling coefficient = 0.9) and at a distance of 2 cm (k = 0.7)—Table 2. The dependences of the output parameters on the operating frequency (150 and 200 kHz) were investigated at different load resistances for each of these distances.

A wirewound resistor was connected for power distribution since the available electronic load has a maximum power of 300 W.

Combinations of the two frequencies described above and the two coupling coefficients were investigated. Figure 6, for example, shows the cases at a coupling coefficient of 0.7.

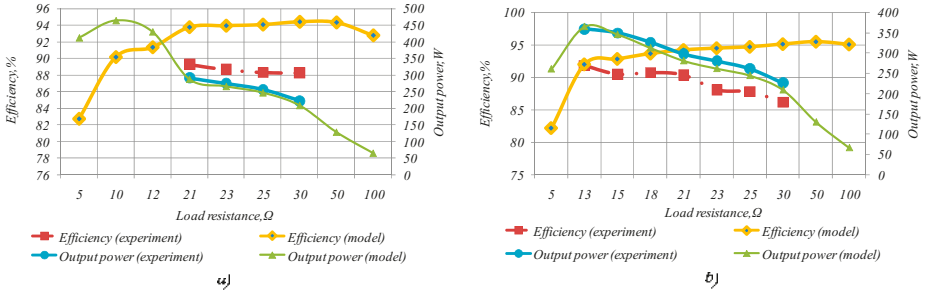

Figure 6. Experimental and simulation dependencies at the load resistance variable at k = 0.7: (**a**) efficiency and output power on the load resistance for f = 150 kHz; (**b**) efficiency and output power on the load resistance for f = 200 kHz.

Figure 6 shows that, in general, the efficiency in the model was slightly higher than in the experiments. However, the experimental efficiency also reached more than 90%. The unevenness of the experimental graphs is explained by the fact that the voltage in the grid can vary constantly during the experiment, while in the model, the desired value is specified.

The investigated maximum transmitted power was 360 W during the experiment under the operating frequency of 200 kHz and load resistance of 15 Ω (Figure 6b). The measured temperatures are shown in Figure 7. The temperature on the transistors surface and coils has almost not changed (40 °C and 42 °C, respectively) during a long-term operation of the circuit at this power. This indicates to the power reserve in these elements (they can withstand more power). The temperature increased to 89 °C on the rectifier diodes. Obviously, the losses in the diodes are the largest of the whole scheme, which confirms the power losses calculations. The heating temperature can be reduced by using a larger radiator or forced air cooling. As a conclusion, the diode losses are the main limitation factor of the further switching frequency increasing.

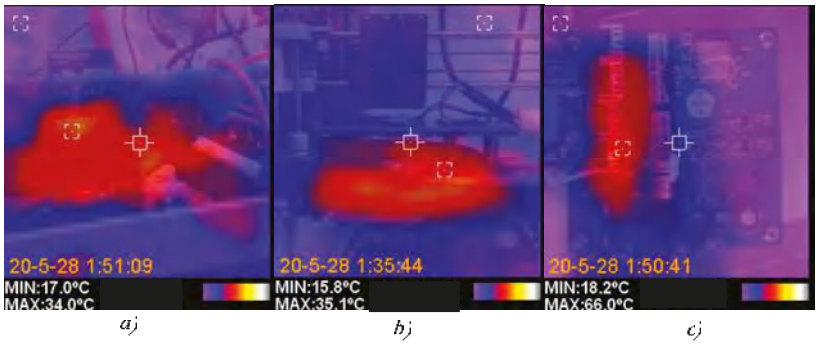

Figure 7. Pictures from the thermal camera at R_L = 15 Ω, k = 0.7, f = 200 kHz, V_{in} = 300 V: (**a**) transistors temperature; (**b**) coils temperature; (**c**) temperature of rectifying diodes.

Large coupling coefficients has been studied to obtain more power (Figure 8). Higher power with a larger duty cycle is of course due to the longer time when the transistors are open and conducting.

The duration of the zero voltage level is minimal under such conditions (Figure 9). The change in the duty cycle has little effect on the efficiency. The dead-time of the transistors was selected taking into account the maximum efficiency of energy transfer. Dead-time in the transistors was set less than 5% of the period.

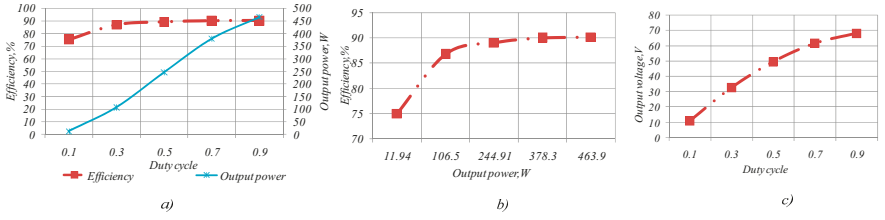

Figure 8. Experimental dependencies at R_L = 10 Ω, k = 0.9, f = 150 kHz, V_{in} = 300 V: (**a**) efficiency and output power on the duty cycle; (**b**) efficiency on the output power with the duty cycle change; (**c**) output voltage on the duty cycle.

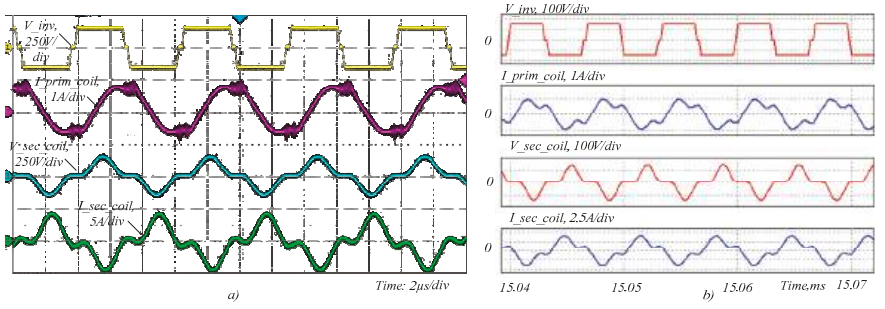

Figure 9. The waveforms on the primary and secondary sides at R_L = 30 Ω, k = 0.9, f = 150 kHz, V_{in} = 300 V: (**a**) experiment; (**b**) simulation.

The shape of the signals in the experiment is shown in Figure 9 for one of the used cases. In particular, the voltage at the output of the inverter (*V_inv*), the current through the primary coil (*I_prim_coil*), the voltage (*V_sec_coil*) and current on the secondary coil (*I_sec_coil*) were recorded.

The shape and the magnitude of the currents and the voltages are very close. The resonance condition is fulfilled.

The influence of the snubber capacity on the power and energy transfer efficiency was also investigated experimentally (Figure 10).

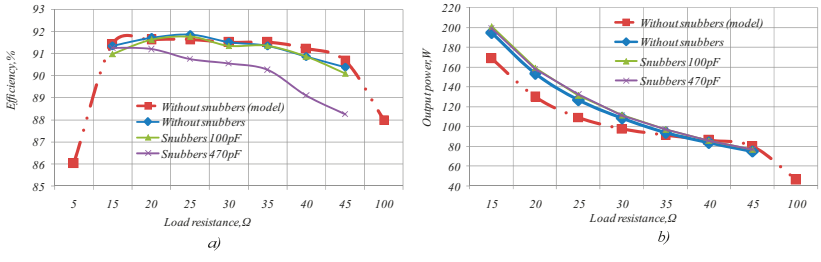

Figure 10. Experimental and simulation dependencies at the load resistance variable at k = 0.9, f = 150 kHz, V_{in} = 300 V: (**a**) efficiency on the load resistance; (**b**) output power on the load resistance.

The snubber capacitance was designed to reduce voltage peaks when the transistor is turned on and off, especially at voltage levels close to critical. Snubber capacitors of different capacities were alternately installed between the drain-source leads of the transistors. The addition of a small snubber capacity in the bridges of the T-type scheme has almost no effect on the energy efficiency (Figure 10a). The effect was more noticeable with an increasing capacitor value and an increasing operating frequency of the transistors.

The distribution of losses is shown at changing the load resistance for the case $k = 0.7, f = 150$ kHz, $V_{in} = 300$ V (Figure 11). The circuit model made in PSIM simulation is an exact copy of the experimental circuit. The data were taken from the model to calculate the losses in the circuit elements.

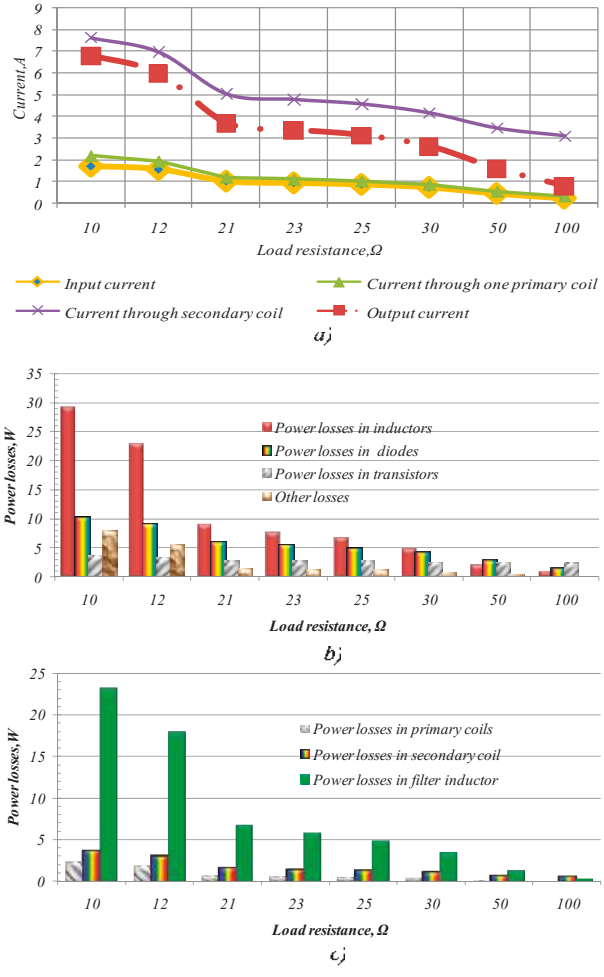

Figure 11. Calculation of power losses at $k = 0.7, f = 150$ kHz, $V_{in} = 300$ V and change of load resistance: (**a**) dependencies of currents through elements on the load resistance; (**b**) distribution of losses by major groups; (**c**) power losses in inductors.

The losses in the inductors and diodes are decreasing significantly with an increasing resistance (and hence with a decreasing current: see Figure 11a. Evidence for this is shown in the charts (Figure 11b,c). Other losses are also decreasing with increasing load resistance for the same reasons.

The total power losses in the transistor remain at approximately the same level in this case. It means that GaN transistors do not reach the maximum current, which they can pass through themselves.

The losses distribution in the semiconductor and magnetic components of the circuit for the same case $k = 0.7$, $f = 150$ kHz, $V_{in} = 300$ V at a load resistance of 10 Ω and 50 Ω are compared in more detail in Figure 12. The static losses in the inductors and diodes are significant (predominant) (Figure 12a). The reason is that with less resistance there is more input and output current. The total calculated losses are 84% relative to other losses. This ratio is already 95% in Figure 12 that confirms the statement described in [32]. It can be explained due to a significant decrease in the current value through all elements of the circuit, especially the output current.

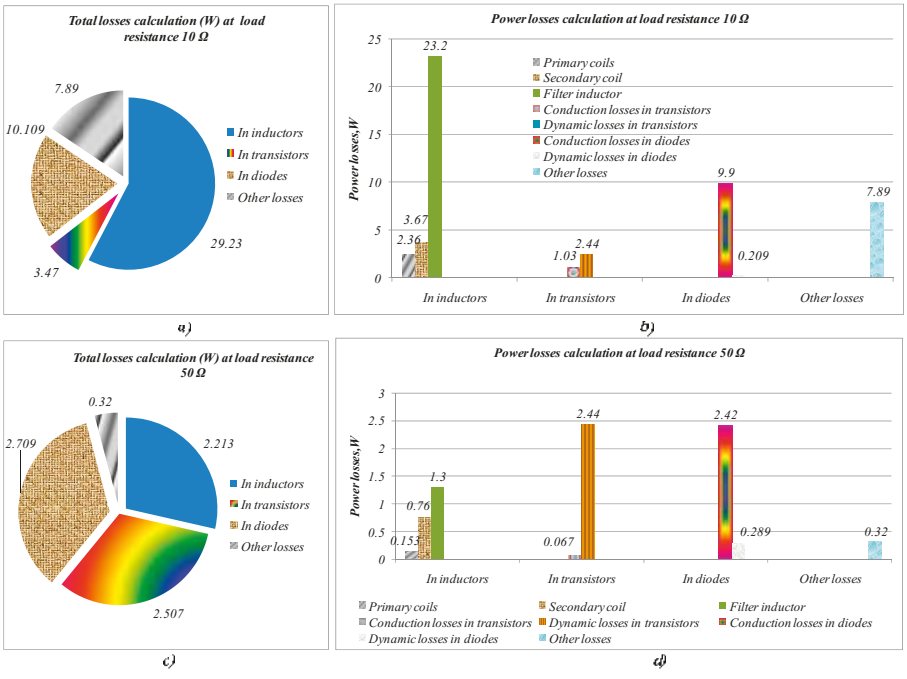

Figure 12. Power losses calculation at $k = 0.7$, $f = 150$ kHz, $V_{in} = 300$ V: (**a**) distribution of losses by major groups for the load resistance 10 Ω; (**b**)detailed distribution of losses for the load resistance 10 Ω; (**c**) distribution of losses by major groups for the load resistance 50 Ω; (**d**)detailed distribution of losses for the load resistance 50 Ω.

The current in the secondary coil is higher due to the lower resistance in the secondary coil and the value of the self-inductance (turns ratio). This causes greater losses compared to the primary coils (Figure 12b,d).

The effect of dynamic losses in the transistor is less noticeable with an increasing transmission power. It means that the contribution of the transistor dynamic losses to the total power losses will be smaller (because they are almost constant due to the large value of P_{oss}).

The dynamic losses of the diode are not significant (Figure 12b,d). They are dependent on the change of output voltage and the operating frequency according to the expression (15) and do not depend on the current.

In summary, in this topology and these transistors, it is possible to obtain an efficiency of up to 95% and a power greater than that shown in this article. This requires very accurate instruments for measuring data and more careful selection of rectifier diodes.

6. Conclusions

The paper analyzes the feasibility of utilizing of GaN transistor in the three-level T-type NPC inverter with two coupled transmitting coils for WPT. The promising T-type topology of the inverter was selected because of the advantages described in the paper over the classical solutions.

To study the system operation, a detailed analysis of the calculation of static and dynamic losses in the transistors and rectifier diodes and static losses in the inductors was conducted. A series of experiments followed, focused on changing different input and output parameters and calculated power losses in the magnetic components and semiconductors. It was established that the greatest losses have concentrated in the magnetic components and rectifying diodes. These losses are mainly of conduction nature, caused by the significant current through these elements. At the same time, the total losses in the transistors are the smallest compared to all other losses on the circuit elements, which shows that this transistor type is absolutely justified for wireless power transfer in this non-classical circuit. However, these transistors are more critical to overvoltage (surges) on the drain-source than other types of transistors. Due to this fact, the particular attention should be paid to PCB design.

The overall energy transfer efficiency was 90% at the maximum experimentally investigated power of 360 W, which is at the level of industrial samples. The system showed excellent stability at different load resistances and changes in different parameters. At the same time, due to the T-type application, along with GaN transistors, this solution has reduced primary coil and does not have heatsink. It has great potential and can operate at higher power with greater efficiency of wireless power transfer.

7. Patents

Ukrainian patent No. 142050 "Wireless power transfer system based on three-level T-type inverter and two coupled transmission coils".

Author Contributions: Idea, supervising: O.H.; theoretical review and writing: D.S.; analytical calculations, simulations and final writing of paper: V.S.; PCB design: O.V.; software and the experiments: B.P.; final editing, revising: R.S. All authors have read and agreed to the published version of the manuscript.

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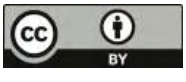

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Aggregated Conducted Electromagnetic Interference Generated by DC/DC Converters with Deterministic and Random Modulation

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Abstract: The assessment of electromagnetic compatibility (EMC) is important for both technical and legal reasons. This manuscript addresses specific issues that should be taken into account for proper EMC assessment of energy systems that use power electronic interfaces. The standardized EMC measuring techniques have been used in a laboratory setup consisting in two identical DC/DC converters with deterministic and random modulations. Measuring difficulties caused by the low frequency envelopes, resulting from frequency beating accompanying aggregation of harmonic components of similar frequencies, were indicated as a phenomenon that might lead to significant problems during the EMC assessment using currently binding standards. The experimental results describing deterministic and random modulated converters might be useful for practitioners implementing power interfaces in microgrids and power systems as well as for researchers involved in EMC assurance of power systems consisting in multiple power electronic interfaces.

Keywords: conducted electromagnetic interference; electromagnetic compatibility; aggregated electromagnetic interference; power electronic interfaces; frequency beat

1. Introduction

Electromagnetic compatibility (EMC) assessment is demanded for technical as well as legal reasons. EMC evaluation is usually based on the use of the dedicated standards, which determine the permissible limit values for electromagnetic interference (EMI), measurement methods, test equipment and provide classification of products according to their characteristics and electromagnetic environment where they are intended to be used [1]. The shape of conducted EMI depends on the source of the interference as well as complex phenomena accompanying the flow of interference in circuits, including parasitic couplings. In the subject matter literature, some papers emphasize the necessity for assurance of reliable operation of complex energy systems and the need for EMC assurance [2–8]. Furthermore, some papers highlight how approaches concerning deterministic modulation (DetM) and random modulation (RanM), based on the parameters' control of fundamental switching frequency (f_{sw}) and duty cycle (d), may contribute to achieving EMC requirements [9–20]. Indeed, the RanM has been widely used since the 1980s [21]. From the practical viewpoint, beyond the reduction in the maximum level of voltage or current harmonics, the choice for RanM has been considered in order to provide, for instance, reduced of burdensome acoustic noise related to switching frequency [10]. However, some manuscripts have shown that the aggregation of interference in the case

of deterministic modulation might be accompanied by low frequency envelopes. This phenomenon may lead to misinterpretations during the EMC assessment [22–25].

According to requirements of the EMC Directive [26] "where apparatus is capable of taking different configurations, the electromagnetic compatibility assessment should confirm whether the apparatus meets the essential requirements in the configurations foreseeable by the manufacturer as representative of normal use in the intended applications". Moreover, the EMC Directive defines responsibility of standard organizations in this context: "The European standardisation organisations should take due account of that objective (including the cumulative effects of the relevant types of electromagnetic phenomena) when developing harmonised standards". Taking into account a global approach to standardization, the issues presented in this paper, concerning aggregation of the conducted electromagnetic interference introduced by power electronic converters with deterministic [27] and random modulation, might constitute a contribution to the elaboration of relevant standards as well as practical information for engineers dealing with assurance of EMC in systems consisting power electronic converters.

As mentioned above, random modulation might contribute to a reduction of maximum levels of EMI spectrum due to more even dispersion of interference over frequency range in comparison with deterministic modulation. Figure 1 shows the EMI measurement of one buck converter topology, with the f_{sw} = 60 kHz, d = 0.5 and with both switch control strategies, DetM and RanM. The EMI measurement presented by Figure 1 was carried out based on the FPGA-based system proposed in [20].

The detailed standard requirements concerning conducted EMI can be found in CISPR 16. Standardized conducted EMI measurements consider the frequency range from 9 kHz to 30 MHz, where the Intermediate Frequency Band Width (IFBW) equal to 200 Hz is applied for the range from 9 kHz to 150 kHz (CISPR A) and IFBW = 9 kHz is applied for the range from 150 kHz to 30 MHz (CISPR B). Since the core concept of the DetM is to provide a f_{sw} constant under the time. The power spectral density is concentrated for frequencies equal to the harmonics of the switching frequency. On the other hand, RanM provides the spreading of interference over frequency range, thus the reduction of maximum observed values is obtained.

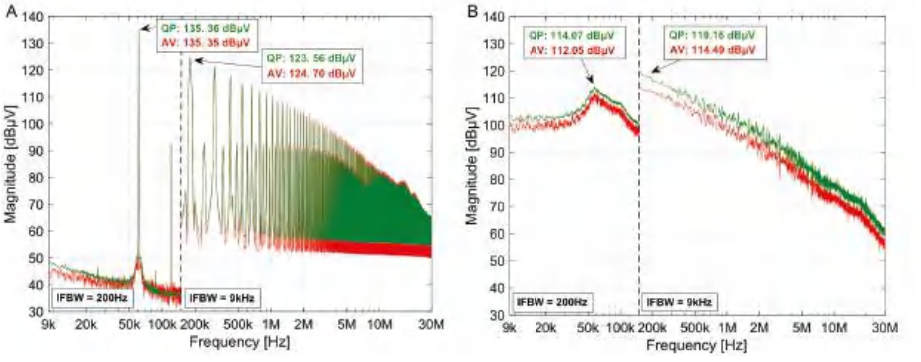

Figure 1. Electromagnetic interference (EMI) measurement of DC/DC converter with the fsw = 60 kHz and d = 0.5: (**A**) for deterministic modulation (DetM) and (**B**) for random modulation (RanM). Results obtained through the FPGA-based system proposed in [20].

The novelty of this paper lies in the presentation of the comparative analysis concerning aggregated interference generated by converters with DetM and RanM. This approach allows us to comprehend the behavior of low-frequency envelopes phenomena beyond the traditional knowledge related with DetM and RanM, i.e., the absence of f_{sw} variation means high disturbance values for the f_{sw} and its harmonics. On the other hand, through the introduction of f_{sw} variation means reduced of disturbances levels. The analyses presented in this paper consider simulations and experimental results based on a standardized testing setup.

2. Simulation Results of Aggregated EMI Generated by DC/DC Converters with Deterministic and Random Modulation

The simulations of DC/DC buck converters with deterministic and random modulation have been run on MatLab software. The function spectrogram was used, and it returns the Short-Time Fourier Transform (STFT) of the aggregated signal with a Hamming window.

Figure 2 shows the results of the simulation in the form of 3D spectrograms. Simulations have been performed for the f_{sw} = 80 kHz and d = 0.5. The spectrogram (A) shows results for one interference signal generated by a single converter with DetM, while spectrogram (B) shows the aggregated interference introduced by two converters operating in parallel. Since the superimpositions of the switching frequency harmonics can be related to the summation of sinusoidal signals of similar frequency. This process of aggregating sinusoidal components with similar frequencies causes modulation of their amplitudes with low frequency envelopes. This phenomenon is well-known in acoustics as frequency beat. The theory of frequency beats [24] highlights that the sum of the harmonic vibrations with the frequencies f_1 and f_2 of amplitudes equal to 1 can be expressed by:

$$S_2(t;\{f_1,f_2\}) = \sin(2\pi f_1 t) + \sin(2\pi f_2 t) = 2\cos\left(2\pi\frac{f_1-f_2}{2}t\right)\sin\left(2\pi\frac{f_1+f_2}{2}t\right). \quad (1)$$

The frequency beat effect appears when $|f_1 - f_2| \ll f_1 + f_2$. In such conditions, the absolute value

$$\mathrm{Env}_2(t;\{f_1,f_2\}) = \left|2\cos\left(2\pi\frac{f_1-f_2}{2}t\right)\right| \quad (2)$$

is the envelope of the aggregated signal. It is also possible to observe that the period of the envelope does not depend on the frequencies of the components, but on the difference between the frequencies of the aggregated signals [24].

The appearance of low frequency envelopes in the case of aggregated interference might cause significant measuring problems.

Additionally, the comparison between spectrograms (A) and (B) in Figure 2 reveals that the maximum observed amplitude is lower in the case of the aggregated interference. However, it should be noted that the power spectral density in a sufficiently wide frequency range and measuring time is higher in the case of aggregated interferences.

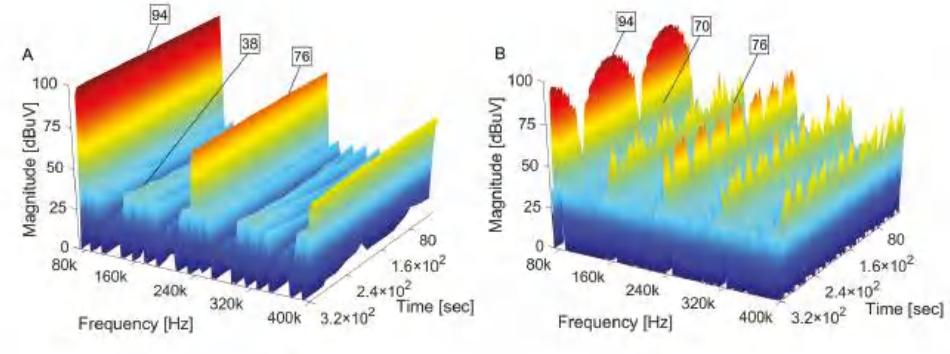

Figure 2. Simulation 3D spectrograms of interference caused by one DC/DC converter with DetM (**A**), and two DC/DC converters with DetM (**B**).

Figure 3 shows the spectrograms corresponding to those presented in Figure 2 with the same parameters, but for random modulation. In both cases of Figure 3, item (A) and (B), the interference

power has been spread over the frequency range, and is more even in comparison with DetM, Figure 2. As a result of a more even distribution of interference power, the maximum measured levels have been significantly decreased.

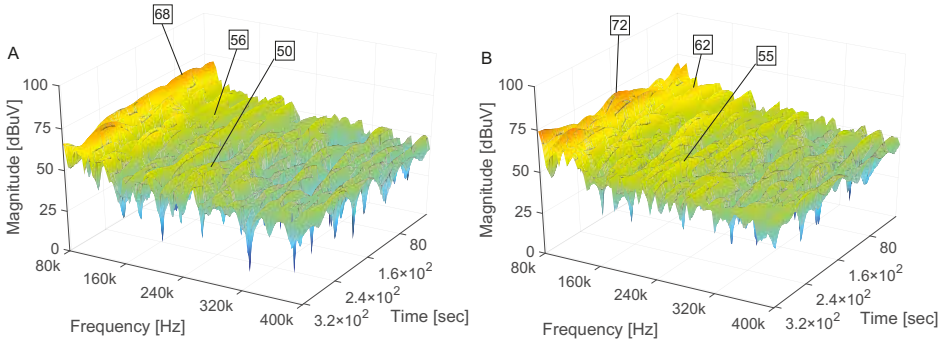

Figure 3. Simulation 3D spectrograms of interference caused by one DC/DC converter with RanM (**A**), and two DC/DC converters with RanM (**B**).

3. Measurements of Aggregated EMI Generated by DC/DC Converters with Deterministic and Random Modulation

In order to confirm the results of the simulation, standardized EMI measurements have been obtained from a laboratory setup fully compliant with EN 55011 based on a voltage probe. Two DC/DC buck-converters constitute the Equipment Under Test (EUT). Both converters are based on a C2-class high speed insulated-gate bipolar transistor (IGBT). The hardware interface for signal and ground are made by the R-Series Multifunction RIO (FPGA PXI-7854R), with VIRTEX-5 LX110. The control signal output (RanM and DetM) is provided at the hardware level by the shielded connector block NI SCB-68A. Figure 4 illustrates the scheme for the measuring testbed.

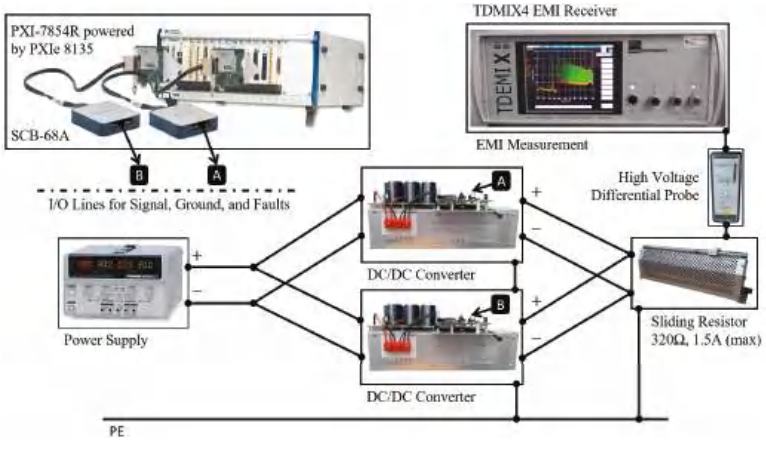

Figure 4. Schematic diagram of measuring testbed.

The schematic diagram presented in Figure 4 shows that both buck-converters are powered by the same regulated laboratory power supply by means of the cables of equal length. In addition, two FPGA control boards were used, and both were powered by controller PXIe 8135 to avoid additional couplings through the power source. A 1.5 A Leybold sliding resistor 320 Ω, was connected as the load on the

output of buck-converters (24 V) connected in parallel. In addition, equal length of cables has been applied. The most important parameters of the buck-converter topology have been summarized in Table 1.

Table 1. The main parameters of buck-converter topology.

Component/Function	Specification
Transistors type	IXGH40N60C2D1
I_C(max)	40 A
t_{on}	40 ns
t_{off}	180 ns
Transistor Gate Drivers	HCPL-316J
Converter Power	1800 W (max)
DC capacitors	1500 µF
Max DC voltage	450 V
Load	sliding resistor 320 Ω (max), 1.5 A (max)

The output voltage was measured by a differential voltage probe SI-9010A from Sapphire Instruments (with a 40 dB attenuation level). In both cases, for all presented experimental results, the f_{sw} = 80 kHz and d = 0.5 remained unchanged. Figures 5 and 6 show the measurements obtained using a digital receiver type TDMIX6 EMI, which provides a 3D spectrogram for both Quasi Peak (QP) and Average (AV) detector and CISPR 16-1-1 compliant measurements. In order to increase readability of the figures, measurements have been taken up to 6^{th} harmonic with IFBW = 200 Hz. The experimental results presented in Figure 5 have confirmed the presence of the frequency beat phenomenon observed in simulations. In a case of two converters low frequency envelopes resulting from frequency beat are superimposed on the interference harmonics.

The use of random modulation to disperse interference over the frequency range prevents the frequency beating phenomenon, which appears during aggregation of sinusoidal components of similar frequencies. Thus, in the case of RanM presented in Figure 6 the low frequency envelopes do not appear for aggregated interference introduced by two DC/DC converters connected in parallel Figure 6B.

Generally, the shapes of experimental results, presented in the form of 3D spectrograms, based on data from a laboratory setup, fit well with corresponding 3D spectrograms obtained by simulations. Both simulation and experimental results confirm the theoretical assumptions concerning aggregation of interference for deterministic and random modulation. The obtained results encouraged us to perform multiple measurements according to standard requirements.

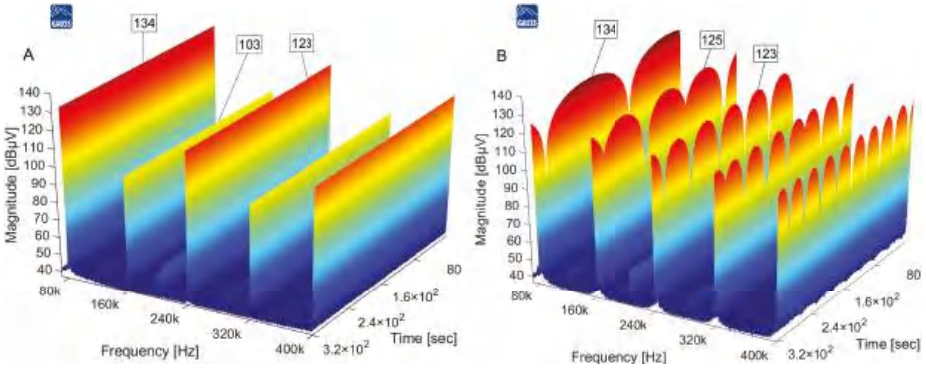

Figure 5. Experimental 3D spectrograms of interference measured using AV detector, caused by one DC/DC converter with DetM (**A**), and two DC/DC converters with DetM (**B**).

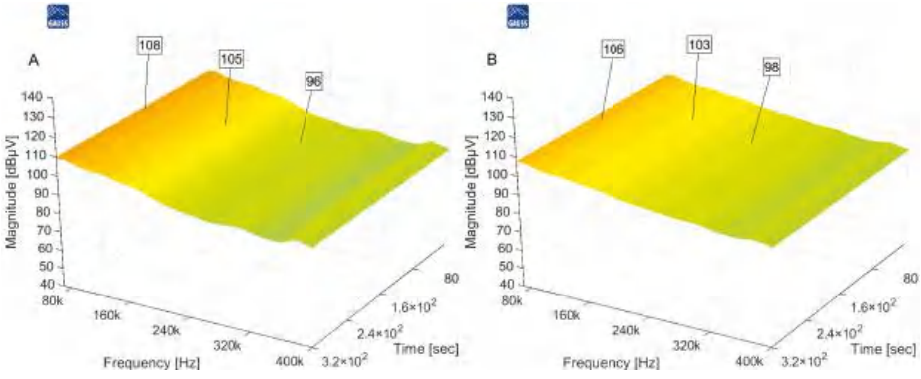

Figure 6. Experimental 3D spectrograms of interference measured using AV detector, caused by one DC/DC converter with RanM (**A**), and two DC/DC converters with RanM (**B**).

4. Statistical Analyses of Aggregated EMI Generated by Converters with Deterministic and Random Modulation Measured According to Standards

In order to present measurement problems connected with the frequency beat phenomenon multiple measurements of the frequency linked with the highest emission were taken. The results of the measurements have been presented in the form of box-and-whisker plots, supplemented with individual values of measured EMI depicted as points. According to standard requirements [28], one final measurement taken during a measuring period equal to 1 s can be compared with the limit line for a presumption of conformity based on harmonized standards. The standards require measurements using QP as well as AV detector. Since the results obtained for both detectors did not differ significantly the presented analyses were based on AV detector measurements only. For each investigated case, 1000 final measurements during 1 s were taken [29].

Figure 7 shows distributions of the results obtained for single DC/DC converters with DetM (A) and RanM (B). The dispersion of the 1000 results in the case of DetM (A) is lower than 0.1 dB. The randomization of the switching frequency caused an increase of the dispersion up to 2 dB. Such distributions of the results confirm that a case of EMI generated by a single DC/DC converter is sufficient for EMI evaluation.

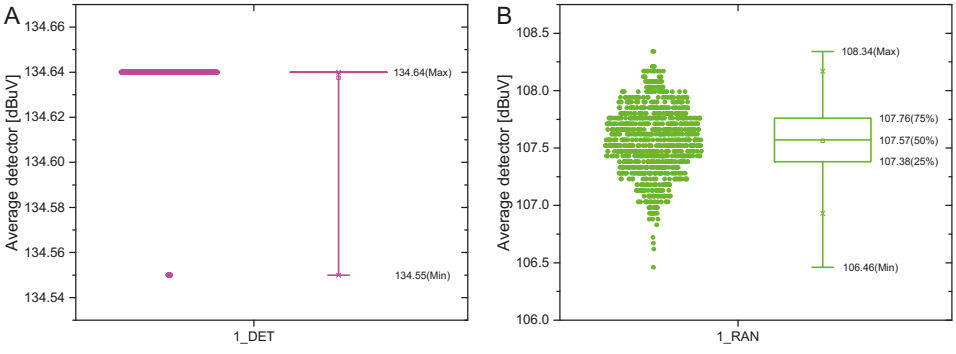

Figure 7. Box-and-whisker plots of 1000 average detector 1 s measurements for one DC/DC converter with: (**A**) deterministic modulation and (**B**) random modulation

The 2 dB dispersion remained unchanged in the case of aggregated interference introduced by two DC/DC converters with random modulation, Figure 8B. However, low frequency envelopes, linked with the frequency beat phenomenon and accompanying aggregation of EMI introduced by

converters with deterministic modulation, caused a significant increase in the range of measured levels. The observed differences reached 25 dB (18 times), Figure 8A.

The observations based on the Figures 7 and 8 are confirmed by statistical parameters determined for empirical distributions presented in the figures. The values of variance and standard deviation of measurements in an arrangement consisting of two DC/DC converters are much greater than in other investigated cases (Table 2). The variance and standard deviation calculation, from the EMI measurement viewpoint, represent the dispersion of the measurements of the AV detector, indicating "how far" in general its values are from the expected value. In fact, such dispersion of the results makes evaluation of aggregated EMI, based on one final measurement, in arrangement consisting converters with deterministic modulation unreliable.

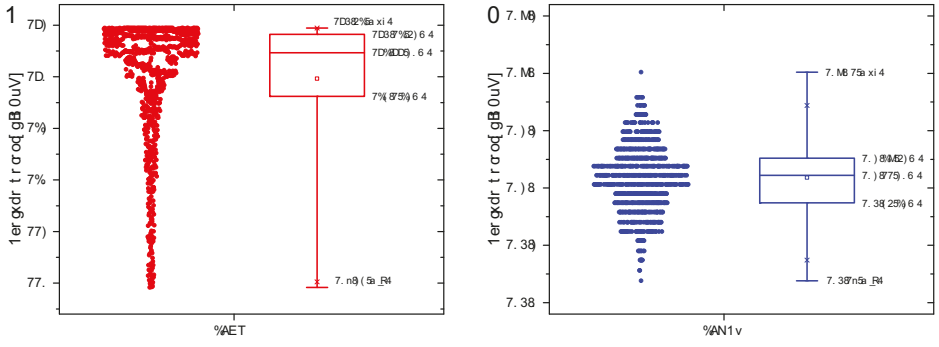

Figure 8. Box-and-whisker plots of 1000 average detector 1 s measurements for two DC/DC converters with: (**A**) deterministic modulation and (**B**) random modulation

Table 2. Statistical parameters of empirical distributions of 1000 final measurements using AV detector.

	Mean	Standard Deviation	Variance	Median	Minimum	Maximum
1_DET	134.64	0.01	0.0002	134.64	134.55	134.64
1_RAN	107.56	0.29	0.08	107.57	106.46	108.34
2_DET	129.82	6.02	36.25	132.33	109.58	134.72
2_RAN	105.09	0.28	0.08	105.11	104.19	106.01

5. Conclusions

In the paper both simulation and experimental results concerning aggregated conducted electromagnetic interference generated by DC/DC converters with deterministic and random modulation have been presented. In the case of deterministic modulation the obtained results have shown that the amplitudes of aggregated interference are modulated with low frequency envelopes caused by the frequency beat phenomenon accompanying summation of sinusoidal components of close frequencies.

The investigation presented in this paper, despite consisting of two identical DC/DC converters, is corroborated by conducted electromagnetic interference in multiconverter systems, as recently investigated by [24], through a real 1 MW photovoltaic power plant. Furthermore, the statistical analyses of large series of final measurement data has confirmed assumptions that low-frequency envelopes might make the standardized EMI tests unreliable.

The research presented has revealed that in the case of random modulation a blurring of instantaneous values of switching frequency contributes to the decreasing of maximum EMI values as well as to the prevention of the frequency beat phenomenon.

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Abbreviations

The following abbreviations are used in this manuscript:

AV	Average
CISPR	International Special Committee on Radio Interference
DetM	Deterministic Modulation
EM	ElectroMagnetic
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EUT	Equipment Under Test
FPGA	Filed-Programmable Gate Array
IEC	International Electrotechnical Commission
IFBW	Intermediate Frequency Band Width
PDF	Probability Density Function
QP	Quasi Peak
RanM	Random Modulation
STFT	Short-Time Fourier Transform

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FPGA-Based System for Electromagnetic Interference Evaluation in Random Modulated DC/DC Converters

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Abstract: Field-Programmable Gate Array (FPGA) provides the possibility to design new "electromagnetic compatibility (EMC) friendly" control techniques for power electronic converters. Such control techniques use pseudo-random modulators (RanM) to control the converter switches. However, some issues connected with the FPGA-based design of RanM, such as matching the range of fixed-point numbers, might be challenging. The modern programming tools, such as LabVIEW, may facilitate the design process, but there are still fixed-point operations and limitations in arithmetic operations. This paper presents the design insights on the FPGA-based EMC friendly control system for DC/DC converter. Probability density functions (PDF) are used to analyse and improve pseudo-random algorithms. The theoretical algorithms, hardware details and experimental results are presented and discussed in terms of conducted electromagnetic interference emission.

Keywords: systems control; electromagnetic compatibility; conducted interference; DC-DC power converters; FPGA; random modulation

1. Introduction

Nowadays, with the advent of smart energy environments, the demand for cyber-physical systems [1] and the growth in switch-mode converter applications [2–6], electromagnetic compatibility (EMC) issues are becoming more and more significant [7]. Among many methods of improving EMC of converters, we may use improved control techniques. In addition to the primary function of controlling energy conversion, such a control technique can reduce the level of conducted electromagnetic interference (EMI) by spreading the harmonics on a broader frequency range [6,8]. A Field-Programmable Gate Array (FPGA) may be used for the cyber-physical implementation of such controls. It should be added that FPGA may be much more flexible and may cover more applications than other commonly used control devices such as microcontrollers (μC) or digital signal processors (DSP). In particular, FPGAs allow for the building of hardware circuits of the modified Pulse Width Modulators (PWM), unlike μC or DSP's, where the built-in PWM circuit cannot be changed.

In a typical PWM circuit, the user may set the fundamental switching frequency (fsw) and the duty cycle (D). The parameter D controls the output voltage of the converters and thus affects the energy conversion process. The f_{sw} of the PWM signal is practically irrelevant to the voltage transfer function of the converter, and of the primary energy conversion. However, it affects the losses in the switch-mode converter and the parameters of the reactance elements. Conducted EMI generated by the converter are grouped around the f_{sw} and its harmonics [8,9]. Any modification of f_{sw} leads to changes in EMI emission.

Traditionally, pseudo-random modulators (RanM) can be used as a switch control strategy, which can reduce the level of EMI [8,10]. In such type of modulation, the frequency of the PWM signal is randomly changed in the selected range. As a consequence, disturbance energy is distributed more evenly across a wider spectrum. The development of a random modulation requires a combination of changes in the frequency fsw (or the period) of the PWM signal with a pseudo-random number generator. Therefore, the range of pseudo-random numbers must be adapted to the specific hardware platform. In addition, the probability density function (PDF) of such a pseudo-random stream should be analysed in terms of the emission of conducted disturbances.

The design of RanM in FPGA may be challenging. The modern graphical programming tools such as LabVIEW may facilitate the design process. Nevertheless, in LabVIEW, there is still some inconvenience associated with fixed-point operations, and with the lack of some arithmetic operations, e.g., divide. Therefore, this manuscript demonstrates how to provide an FPGA-based control system for a DC/DC converter that limits the level of conducted EMI. The presented algorithms, based on LabVIEW engineering software, do not change the essential functions or parameters of the converter. During the design of algorithms, we take into account the PDF of frequency changes, and we propose a method of shaping the PDF in FPGA without arithmetic division and using only fixed-point operations. For the presented algorithms, we perform the EMI evaluation in an experimental system. The CISPR-A frequency band was considered as the primary frequency range for tests.

2. FPGA-Based Systems Design

2.1. FPGA Hardware

In the manuscript, we consider National Instruments PXIe-8135 controller as the primary development environment. The PXIe-8135 is an Intel Core i7 embedded controller with the design tool—LabVIEW. The development environment also includes the FPGA R-Series Multifunction RIO - PXI-7854R card (illustration in Figure 1) with VIRTEX-5 LX110 [11].

Figure 1. Field-Programmable Gate Array (FPGA) PXI-7854R illustration [11].

The PXI-7854R FPGA-based card has a few dozen Input/Output (I/O) resources, which include analog/digital converters (ADCs), digital/analog converters (DACs) and digital I/O lines. The design tool LabVIEW accesses the FPGA PXI-7854R device through the bus interfaces (PXI Triggers and PXI BUS). This connection makes possible timing, triggering, processing and custom I/O measurements, based on FPGA target programming, and most of it is available for demanded functions. Those required functions may use varied amounts of logic, besides using I/O resources. We assume that all control techniques require the same I/O resources, such as signals controlling transistors, or input faults. Therefore, the number of FPGA resources, used for logical and arithmetic operations, indicates the algorithmic complexity and it will be considered as one essential parameter to evaluate the control techniques implemented in FPGA.

2.2. PWM Modulator Algorithm

To control the converter switches the PWM modulator is used. Figure 2 shows the main flowchart of the PWM modulator. For better visualization, we divide all operations into three (III) parts. In part I, the user may set the main control parameters: the average switching frequency f_{sw} and duty cycle of the PWM signal D. Then, the program calculates the required number of clock ticks for the period (N) and the duration of high state (N_d) according to the Equations (1) and (2).

$$N = f_{FPGA}/(f_{sw} \cdot SC_{TL}) \tag{1}$$

$$N_d = D \cdot N \tag{2}$$

where:
f_{FPGA}—onboard available clock frequency, f_{sw}—switching frequency and SC_{TL}—single cycle timed loop (in clock ticks).

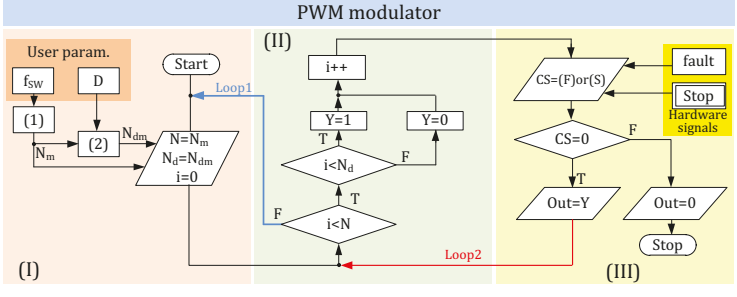

Figure 2. The main flowchart of the PWM modulator, providing parameters (I), counter ramp (II), and generation of output signal (III).

The index m (in Figure 2) means that the N_{dm} and N_m value is taken and recalculated for the m'th PWM period. The presented modulator can, therefore, cooperate with an external voltage controller and dynamically change the factor D. The duration of the period, represented by N_m, may be constant for deterministic modulation (DetM) or may be changed randomly for RanM case. Part II illustrated the carrier function counter ramp represented by the variable i. Parameters N and N_d are compared with the variable i to determine the value of output signal Y and control the loop I execution. Part III presents the generation of control (output) signal and the interaction with a CS function. In the presence of hardware signals of fault (F) or the stop button (S), the function CS returns 1, and the PWM operation is interrupted. The fault signal is typically generated by converter hardware in any emergency, while the stop signal is from the user. Figure 3 shows the operation of the modulator.

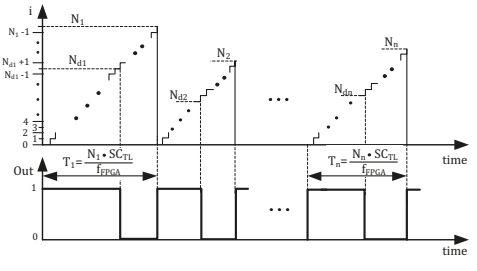

Figure 3. The principle of the PWM operation.

2.3. Random Number Generator

The main advantage of RanM instead DetM is highlighted in the literature [8,10,12–15] as the EMI noise reduction related to the f_{sw} and its harmonics. The random number generator is crucial to the operation of RanM control algorithms. Since we consider FPGA features connected with the fixed-point operation, we propose to generate the random stream by a linear congruential generator (LCG). The LCG is a modular arithmetic algorithm, which provides a stream of pseudo-randomized numbers calculated with a Equation (3).

$$RN_m = (\alpha \cdot RN_{m-1} + c) \; mod \; n \tag{3}$$

where:
RN_m—the m'th random number provided by LCG, α, c, n—LCG coefficients.

The values of coefficients configured for the FPGA implementation were $\alpha = 17$ and $RN_0 = 17$, $c = 0$ and $n = 2^{32}$. The modulo operation is made automatically due to the use of long integer variables with 32 bits of storage. For RanM, the generation of a random stream is done in a loop to get a new pseudo-random number for each PWM signal period. The presented LCG generates pseudo-random numbers with a period of 2^{31} and a normal distribution. To show the property of a random stream, Figure 4 shows the 10,000 numbers RN_m generated by LCG and their histogram/distribution.

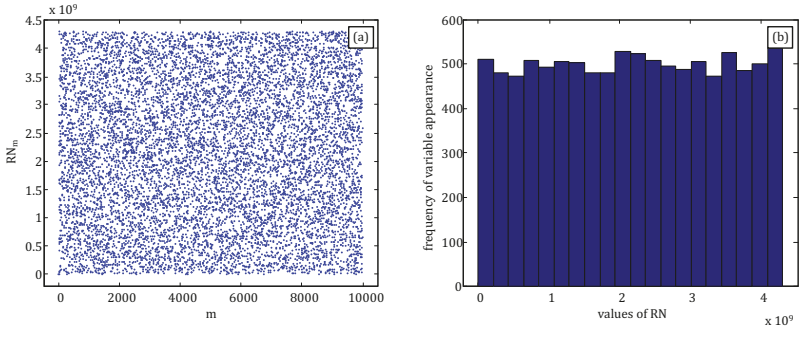

Figure 4. RN_m distribution (**a**), and histogram (**b**).

2.4. FPGA Implementation

This section presents the practical implementation of DetM and RandM in FPGA systems utilizing LabVIEW software. Additionaly, for RanM probability density function PDF analysis in MATLAB software will be shown.

Traditionally, during LabVIEW programming, we use modules with palettes of structures and functions. The number of such functions in LabVIEW FPGA Module is much smaller than for typical control devices with a microprocessor. Further, available functions can only operate on integer variables. Despite these drawbacks, the LabVIEW program Implementation in FPGA systems allows full control of program execution and high speed calculation. For instance, the LabVIEW FPGA Module has access to Single-Cycle Timed Loops (SCTL). The SCTL is a unique loop structure that executes all functions inside within one fixed time period (SC_{TL}) [11]. The SC_{TL} may be defined by the user as a time period or in ticks of the FPGA clock. In the control board used, the maximum clock frequency is 40 MHz.

To realize the algorithm from Figure 2 in LabVIEW for FPGA, the While Loop structure with a sub-system For Loop was chosen. The For Loop corresponds to the loop II in Figure 2 and is executed N times. The While Loop corresponds to the loop I in Figure 2. The While Loop is performed until the CS function is activated. For DetM we consider the $SC_{TL} = 1$ tick, and the number $N = N_m$ is constant.

2.4.1. Single Randomization

For RandM the number N_m is randomly changed for each PWM period using a random stream from the LCG (described in previous section). However, due to the use of fixed-point operations in FPGA, the resulting random number must be scaled (reduction of bit precision) to make it suitable for N_m calculation. Figure 5 illustrates in the part I how to scale the RN_m using the Reshaped Array Function (R_{AF}) which is available in the LabVIEW environment.

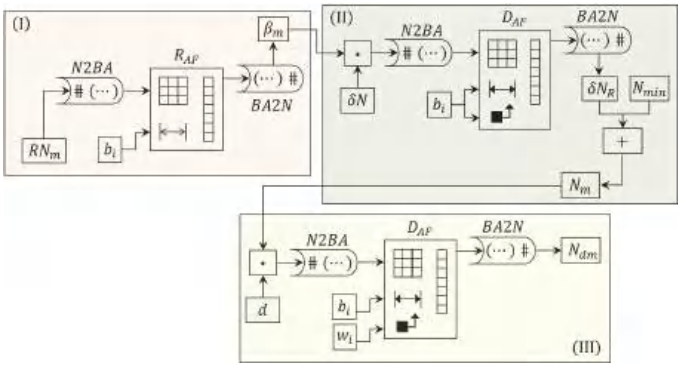

Figure 5. The scheme of the RN_m scaling process, led to lower bit precision (**I**), and for calculating the random stream of N_m (**II**) and N_{dm} (**III**).

Figure 5 shows in part I the parameter b_i, which is responsible for providing the length of the output array and must be numeric. Before resizing, the number RN_m is converted to a Boolean Array by the $N2BA$ function. After resizing, the Boolean Array is converted to a number again by the $BA2N$ function. As a result, a random number, β_m, from 0 to $2^{b_i} - 1$ is obtained. The next task is to calculate N_m and N_{dm} (from Figure 2), to change randomly according to the random β_m number for each PWM period. The changes of the N_m and N_{dm} should also take place within the assumed range from the N maximum and minimum values. These operations should be performed with the appropriate precision in fixed-point arithmetic. However, LabVIEW software for FPGA does not allow direct actions of the mathematical division. The solution to the stated problem for N_m calculation is shown in part II of the Figure 5. The δN describes the maximum assumed changes in the PWM period and may be calculated as:

$$\delta N = N_{max} - N_{min} + 1. \tag{4}$$

The δN can be also represented relative to the average value of N, e.g., $\delta N = 50\% \cdot N_{AV} + 1$. Thus, for the first interaction illustrated in Figure 5, part II, consider the multiplication of the β_m by δN. Since a divide operation is not available, the Delete from Array Function (D_{AF}) is applied to provide δN_R, a random stream that corresponds to the range between the 0 and the value of $\delta N - 1$. In this step, the N_m value is calculated using Equation (5). The final formula for calculating N_m according to the concept from Figure 5, part II, is presented in Equation (6).

$$\delta N_R = (((RN_m \gg (32 - b_i)) \cdot \delta N) \gg b_i) \tag{5}$$

$$N_m = \delta N_R + N_{min} \tag{6}$$

Although Equation (6) accurately describes random changes in the N value (which corresponds to the PWM period—T_{PWM}), it does not provide information on the average value. Therefore, later in the article, discussing RanM properties, we will give the average value of $N - N_{AV}$, and δN, so

the variation range of N is equal to $N_{AV} \pm \delta N/2$. Choosing the right δN is not apparent and should be the subject of a broader analysis. Despite, this topic will not be fully discussed in this article. However, we will show the basic challenges that face when choosing parameters for RanM.

We can take δN value based on expected frequency randomization. For instance, if we assume that $f_{sw} = 80$ kHz and this frequency may change $\pm 50\%$, we will obtain $max(f_{sw}) = 80$ kHz + 50% = 120 kHz, $min(f_{sw}) = 80$ kHz $-$ 50% = 40 kHz. The N_{min} value will be related to 120 kHz and N_{max} to 40 kHz (based on Equation (1)), so δN = 1000 $-$ 333 + 1=668. However, the value of $N_{AV} = 667$ which does not correspond to a frequency of 80 kHz. Figure 6 shows the histogram of randomized N_m values and the histogram of randomized frequencies f_{sw} related to N_m, for $N_{AV} = 667$ with $\delta N = 668$. Figure 6b shows that switching frequency f_{sw} varies within the assumed range from 40 to 120 kHz. Despite this, the frequency distribution is not uniform and the average frequency is not equal to 80 kHz. Adopting the δN in such a way is therefore not particularly useful. Another possible approach to selecting δN value may be made based on a relative change in time. Figure 7 shows the histogram of N_m values and histogram of f_{sw}, for N_{AV} = 500 (value related to f_{sw} = 80 kHz) with δN = 334 so $N \in < N_{AV} \pm 30\% >$. In such a case, the average value of the frequency is closer to that intended, but the frequency distribution is still strongly non-linear.

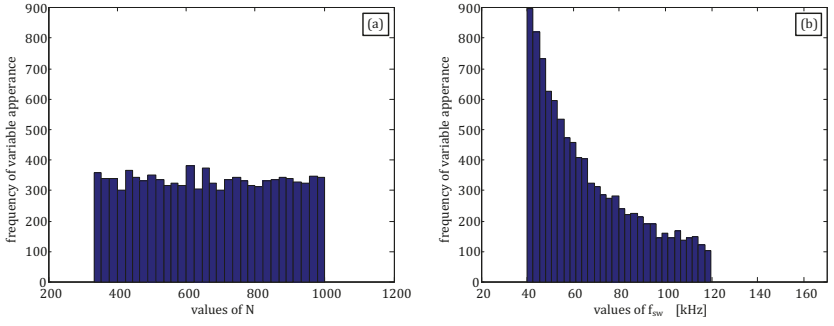

Figure 6. Histogram of N_m ticks distribution (**a**), and histogram of frequency distribution (**b**), for $N_{AV} = 667$ and $\delta N = 668$.

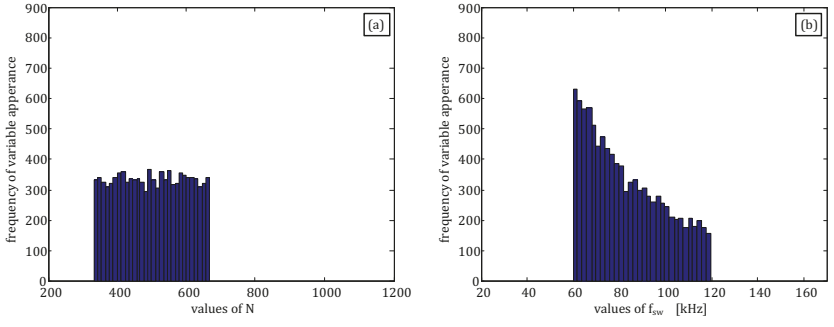

Figure 7. Histogram of N_m ticks distribution (**a**) and histogram of frequency distribution (**b**), for $N_{AV} = 500$ and $\delta N = 333$.

Figure 5 shows in part III the D_{AF} function with consideration of the set up of length and index of array, to provide calculation of N_{dm}. We assumed that the coefficient d, represented as an 8 bit integer will be proportional to duty cycle factor D. The FPGA implementation considers the index value (w_i) equal to 8, and the b_i equal to 23. Thus, the final value of N_{dm} is configurable, maintaining the proportionality with N_m, within a range defined by d, as follows in Equation (7).

$$N_{dm} = D \cdot N_m = ((d \cdot N_m) >> w_i) = \frac{d \cdot N_m}{2^{w_i}} \tag{7}$$

To calculate the period of PWM signal and its Duty cycle for RanM we use Equations (6) and (7), respectively. These equations are computed in the fixed time of a one loop execution—SC_{TL}. We may consider the situation, in which the time SC_{TL} is also changed randomly (RSC_{TL}).

2.4.2. RanM with RSC_{TL}—Additional Randomization

When we randomly change both the number of periods of the For Loop (N_m) and the duration of this loop, we can talk about an additional randomization (RanM with RSC_{TL}). Basically, for RSC_{TL} generation, we assume the same principle, as illustrated in Figure 5, part I and part II, however instead of $SC_{TL} = 1$ tick we generate random value from 7 to 13. The m'th PWM period T_{PWMm} is equal to $(N_m \cdot SC_{TLm})/f_{FPGA}$. Figure 8 shows the histogram of the T_{PWMm} and histogram of related f_{sw}, for $N = 50$, $\delta N = 34$ and $RSC_{TL} \in < 7 : 13 >$. Figure 8 shows that when we consider N_m and RSC_{TL}, the density distribution in both cases, (a) and (b), is changed. This approach of N_m and RSC_{TL} randomization gives us the possibility of shaping the density distribution. The frequency distribution is closer to the Gaussian distribution, which should be more favourable in terms of the average frequency and converter losses.

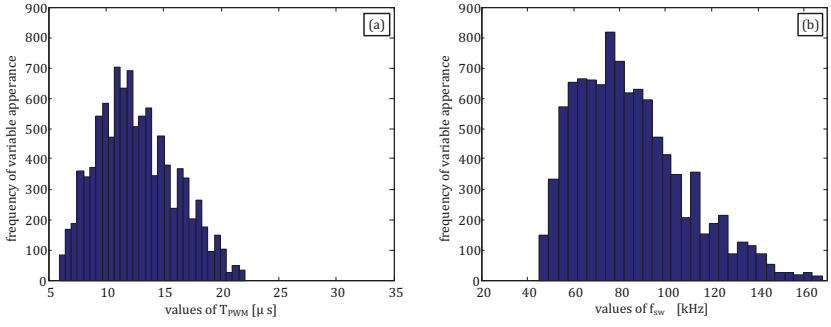

Figure 8. Histogram of T_{PWMm} distribution (**a**) and histogram of related f_{sw} distribution (**b**), for $N_{AV} = 50$ with $\delta N = 34$, and $RSC_{TL} \in < 7 : 13 >$.

2.4.3. RanM2—Split Distribution of Variable

The other method to shape the T_{PWMm} and f_{sw} distributions is to split the N_m distribution to a few sub-ranges in the entire Nm range. For the presented FPGA implementation, we propose to use two predefined random sequence ranges. Then we consider the use of one random bit, digital 1 and 0 levels to choose the range of N_m. The FPGA implementation is executed with a particular function (SF), which is available in the LabVIEW environment. The parameter S determines whether the SF returns the value wired to T or F. Thus, for each parameter, F or T, we assign one of the two predefined random sequence ranges, both provided by Nm. Figure 9 illustrating the proposed FPGA implementation. We will denote random modulation with such a distribution as RanM2.

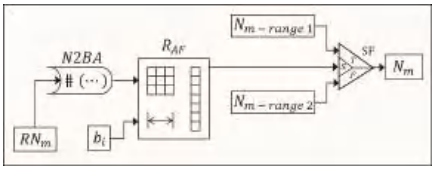

Figure 9. Illustration of N_m generation in proposed RanM2.

Figure 10 shows the histograms of Nm values and their corresponding f_{sw} values, for $N_{AV1} = 750$ with $\delta N_1 = 500$ and $N_{AV2} = 416$ with $\delta N_2 = 167$.

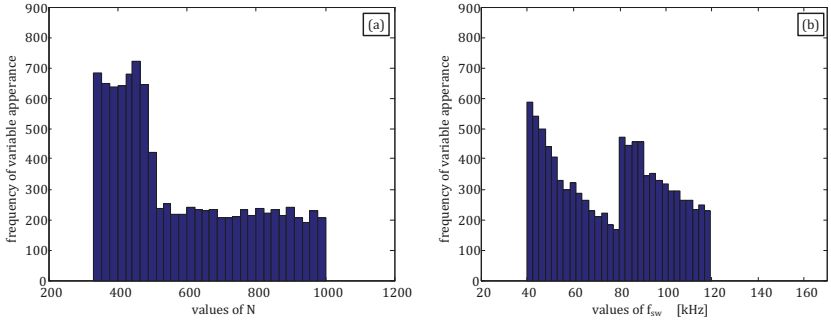

Figure 10. Histogram of N_m ticks distribution (**a**) and histogram of frequency distribution (**b**), for RanM2 with parameters: $N_{AV1} = 750$ with $\delta N_1 = 500$ and $N_{AV2} = 416$ with $\delta N_2 = 167$.

As one can see, the use of two probability distributions for a PWM period (which is proportional to N_m) produces a more equal alignment of the frequency distribution. Therefore, in such a manner there is a possibility to create, with obvious limitations, the distribution of frequency.

2.4.4. RanM2 with RSC_{TL}

The presented concept of two distributions of N_m (RanM2) may be linked with the concept of additional randomization RSC_{TL}. Figure 11 considers such a case with $RSC_{TL} \in < 7 : 13 >$ and for $N_{AV1} = 75$ with $\delta N_1 = 50$ and $N_{AV2} = 42$ with $\delta N_2 = 17$. The obtained histograms are more smooth than histograms in Figure 10, which can be an advantage. However, the use of RSC_{TL} increases the frequency spread.

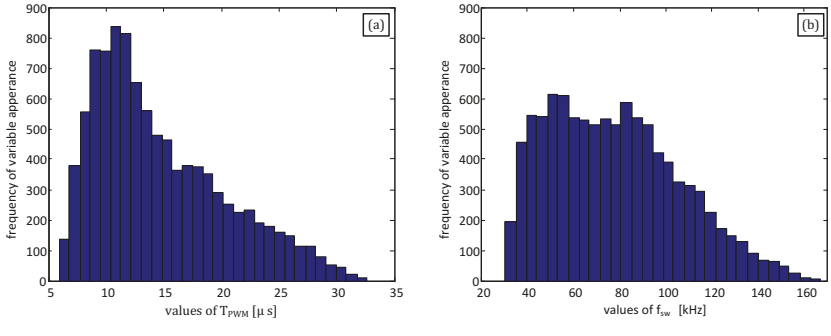

Figure 11. Histogram of N_m ticks distribution (**a**) and frequency distribution (**b**), for RanM2 with RSC_{TL} with parameters: $RSC_{TL} \in < 7 : 13 >$, $N_{AV1} = 75$, $\delta N_1 = 50$, $N_{AV2} = 42$ and $\delta N_2 = 17$.

Figure 12 shows the LabVIEW general program implemented in FPGA. In Figure 12, the parts corresponding to (I) and (II) refer to the basic modulator configuration (Figure 2). Therefore, it is applicable to both DetM and RanM. Part (III) presents the random number generator with a number scaling block, corresponding to part I of (Figure 5) and is used only for RanM, for both approaches of randomization discussed in Section 2.4 Parts (IV) and (V) correspond to part II and part III of (Figure 5), respectively. Since the FPGA needs to execute predefined random sequence ranges (the concept of additional randomization), the D_{AF} function proportionally increases.

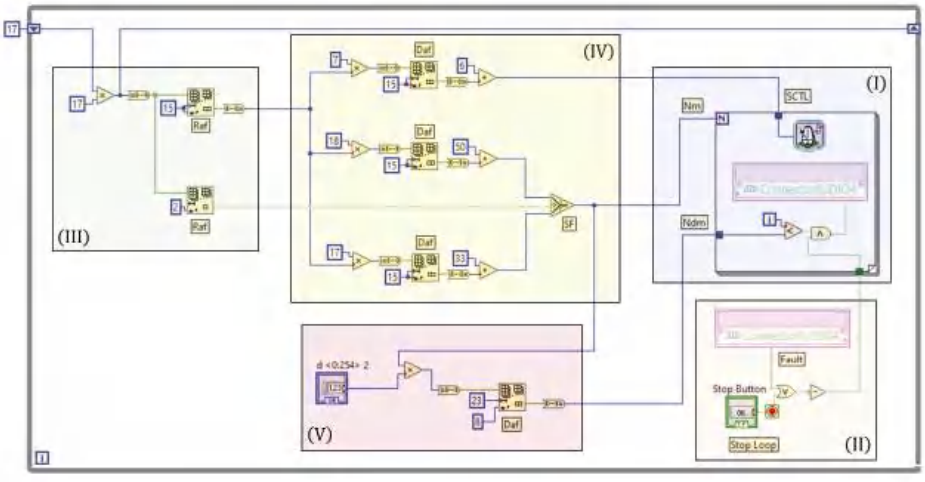

Figure 12. LabVIEW general program implemented in FPGA, for loop (counter ramp) and output signal generation (I), conditions for stopping the program II), random number generator (III), N_m and SC_{TL} calculation (IV), and N_{dm} calculation (V).

3. Experimental Results

This section provides the results of an experimental system. All presented analyses and measurements concern a buck-converter topology, with a C2-class high speed insulated-gate bipolar transistor (IGBT), and a hardware interface for signal and ground to the R-Series Multifunction RIO (FPGA PXI-7854R). The control signal output (RanM or DetM) is provided, at the hardware level, by the NI SCB-68A shielded connector block. Combined with the shielded cables, the SCB-68A provides rugged, very low-noise signal termination to the transistor gate drive. Figure 13 illustrates the scheme of the measuring testbed.

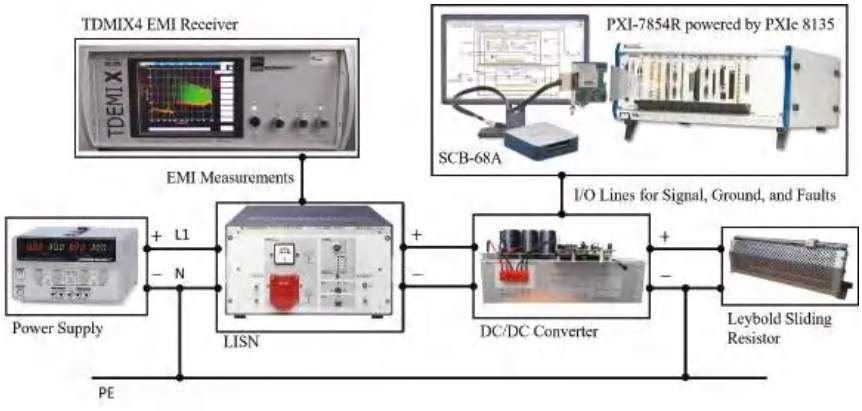

Figure 13. Schematic diagram of measuring testbed.

According to the schematic diagram illustrated in Figure 13, the buck-converter topology is powered by a regulated laboratory power supply. Additionally, the FPGA control board power is controlled by the PXIe 8135 to prevent additional couplings through the power source. A Leybold sliding resistor 320 Ω, 1.5 A was connected as load for the buck converter output. The EMI

measurement was performed with the 50 Ω/50 µH Line Impedance Stabilization Network (LISN). The important parameters of the buck-converter and the testbed are summarized in Table 1.

Table 1. The main parameters of buck-converter topology.

Component/Function	Specification
Transistors type	IXGH40N60C2D1
I_C (max)	40 A
t_{on}	40 ns
t_{off}	180 ns
Transistor Gate Drivers	HCPL-316J
Converter Power	1800 W (max)
DC capacitors	1500 µF
Max DC voltage	450 V
Load	sliding resistor 320 Ω (max), 1.5 A (max)

Figure 14 shows the measurements for all cases (DetM and RanM) presented in Section 2. The results have been obtained using the TDMI X6 EMI receiver, which provides a 3D spectrogram for Quasi Peak (QP) detector, which is required by EMC standards in CISPR A frequency band.

The Figure 14a refers to the measurement for DetM with $N_m = N_{AV} = 500$ and $\delta N = 0$. The first harmonic magnitude (occurring at 80 kHz) is the most significant in the whole frequency spectrum. The magnitude of this harmonic is equal to 93.76 dBµV. The Figure 14b refers to measurement for RanM with $N_{AV} = 667$, δN = 668 and SC_{TL} = 1. As expected, the maximal harmonic magnitude is not connected with the $f_{sw} = 80$ kHz. Despite this, the frequency varied within the assumed range (Figure 5), and the spectrum level is lowered to value 74.24 dBµV. The Figure 14c presents the measurement results for RanM with $N_{AV} = 500$, $\delta N = 330$ and SC_{TL} = 1. As expected, the maximal harmonic magnitude is lowered and its frequency is more connected with the f_{sw} = 80 kHz. The maximum amplitude of the disturbances is equal in this case to 73.43 dBµV, and despite the smaller range of f_{sw}, variation is lower than in the case of RanM from Figure 14b. Therefore, we can conclude that increasing the δN range does not always lead to a lowering of the spectrum level. The Figure 14d refers to the measurement for RanM with $N_{AV} = 50$, $\delta N = 34$ and $RSC_{TL} \in < 7 : 13 >$. The maximal harmonic magnitude is connected with the f_{sw} = 80 kHz, and a little EMI noise reduction is provided, whether compared with Figure 14b,c. The Figure 14e refers to the measurement for RanM2 for parameters: N_{AV1} = 750 with δN_1 = 500, N_{AV2} = 416 with δN_2 = 167, and SC_{TL}. As expected, two extremes are visible in the spectrum. The Figure 14f shows the result of measurement for RanM2 with RSC_{TL} (concept of additional randomization). The parameters of modulator are: $RSC_{TL} \in < 7 : 13 >$, $N_{AV1} = 75$, $\delta N_1 = 50$, $N_{AV2} = 42$ and $\delta N_2 = 17$. The EMI noise is spread with a better shape between all RanM proposed. Unfortunately, the spread of f_{sw} value is the largest of the analysed cases (Figure 11). Based on the measurement, it is difficult in this case to determine the main/dominant frequency of disturbances.

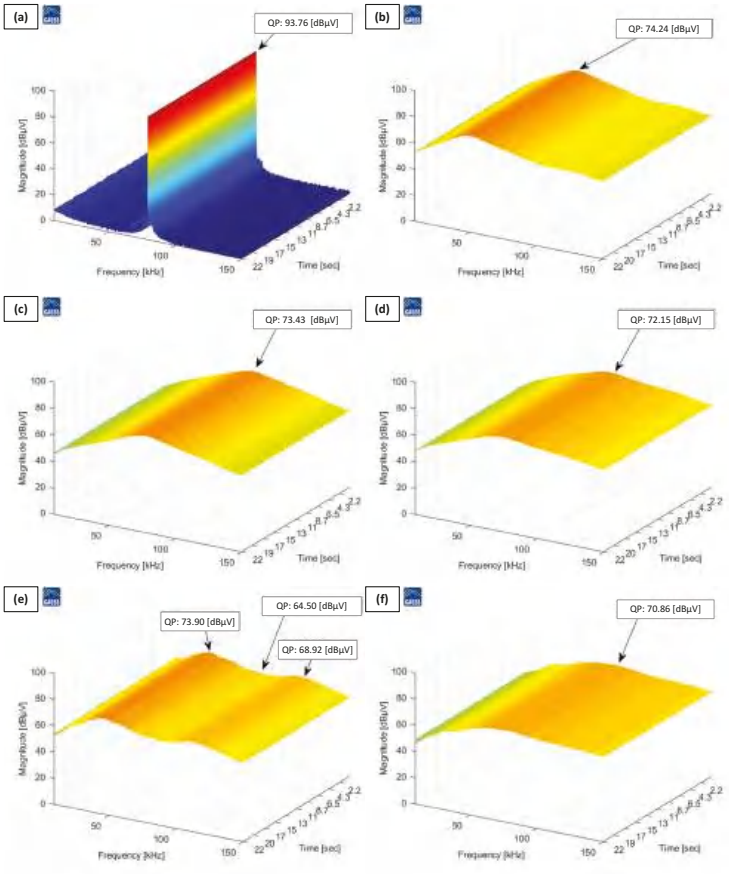

Figure 14. The electromagnetic interference (EMI) spectrum for DetM with $N = 500$ (**a**), RanM with $N_{AV} = 667$, $\delta N = 668$ (**b**), RanM with $N_{AV} = 500$, $\delta N = 330$ (**c**), RanM with RSC_{TL} for $N_{AV} = 50$, $\delta N = 34$ and $RSC_{TL} \in < 7 : 13 >$ (**d**), RanM2 with $N_{AV1} = 750$, $\delta N_1 = 500$, $N_{AV2} = 416$, $\delta N_2 = 167$ (**e**), RanM2 $RSC_{TL} \in < 7 : 13 >$, $N_{AV1} = 75$, $\delta N_1 = 50$, $N_{AV2} = 42$ and $\delta N_2 = 17$ (**f**).

4. Discussion and Analysis of Results

According to Figure 14a, the maximum harmonic magnitude in the spectrum (observed at 80 kHz) for DetM is about 93.76 dBµV. Furthermore, Figure 14d shows the maximum harmonic magnitude in the spectrum (observed at 80 kHz) for RanM with RSC_{TL}, which is about 72.15 dBµV. Therefore, RanM with RSC_{TL} provides 21.61 dBµV for QP detector, with lower EMI levels than DetM. Applying the concept of additional randomization with RSC_{TL} and sectional distribution of Nm, RanM2 obtained the best results—Figure 14f. The results are about 22.90 dBµV for the QP detector, being lower than DetM. According to the literature, the evaluated harmonic reduction could also be provided by the Harmonic Spread Factor (HSF) [16,17]. The HSF is an accurate evaluation index of any waveform for testing its harmonic spreading effects, and is defined as follows in Equations (8) and (9).

$$HSF = \sqrt{\frac{1}{N}\sum_{j=1}^{N}(H_j - H_o)^2} \tag{8}$$

$$H_o = \frac{1}{N}\sum_{j=1}^{N}(H_j) \tag{9}$$

where: H_j is the amplitude of the jth harmonics and H_o is the average value of all N harmonics.

The ideally spread spectrum must be near zero, i.e., white noise, presenting an HSF equal to zero. In this manuscript, the HSF analysis provides in absolute value, the harmonic reduction into CISPR A frequency band, for QP detector measurement and additionally for AV detector. Figure 15 shows the results of HSF calculation.

It is possible to observe that there are almost no differences between all HSF provided by RanM and RanM2 (for both QP and AV detectors). Of course, there is a significant difference between RanM2 and DetM. RanM2 based on the concept of additional randomization with SC_{TL} presents the best HSF. However, whether compared with RanM2 based on the concept of additional randomization with RSC_{TL} the difference is only 0.3% for QP and 0.1% for AV. In terms of EMI noise reduction, the difference between RanM2 with SC_{TL} and with RSC_{TL} is not too big for both detectors (less than 4 dB). Despite this, the frequency distribution was different in each case.

Additionally, hardware resources were also analysed. The hardware resources on an FPGA are indicated by the number of slices. The DetM code after the compilation process presents total slices of 3.0% from all available slices in the VIRTEX-5 LX110 FPGA. On the other hand, among all RM codes, the concept of additional randomization, RanM2 with RSC_{TL} presents greater use of the number of slices, with 5.5%.

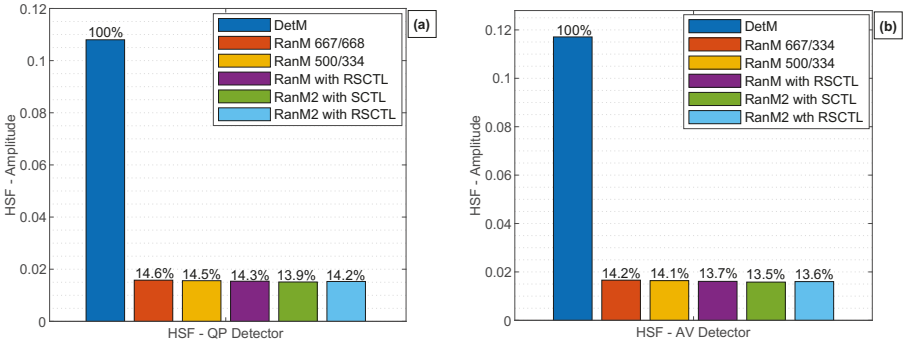

Figure 15. Harmonic Spread Factor (HSF) calculations: (**a**) detector Quasi Peak (QP) and (**b**) detector Average (AV).

5. Conclusions

This manuscript demonstrates how to design RanM, and DetM oriented for FPGA implementation with the LabVIEW engineering software. Since there are some FPGA software limitations (fixed-point operation, and a lack of basic arithmetic functions), it may be challenging to complete the RanM and the DetM implementation. Therefore in the article, we have highlighted how to do some calculations required for PWM modulator implementation in FPGA. We have also shown that the realization of RanM in FPGA should consider the distribution of randomized time and frequency parameters of the PWM signal. One should pay the primary attention to the range of switching frequency f_{sw} changes and the average value of this frequency.

The presented algorithms have been implemented in FPGA - R-Series Multifunction RIO (PXI-7854R), with VIRTEX-5 LX110. The most extensive version of the algorithm (RanM2 with RSC_{TL}) used only 5.5% of FPGA resources. Presented algorithms are weary simple, and they can be easily expanded. Likewise, implementing the modulator to a control system inside the same FPGA is also possible. Therefore, the proposed solutions can be used in all DC/DC converters applications. However, one may obtain the most significant benefits in automotive and lighting applications where

there are direct limits on interference emission in the CISPR A band, and proposed control methods help fulfill these requirements.

Proposed modulators were tested experimentally. All measurements were carried out according to EMC standards in the frequency domain for CISPR A frequency band. The EMI emission (for design RanM) was significantly reduced compared to the DetM. We have achieved a reduction of the maximum EMI level value by over 20 dB. One should also remember, according to [8], that although pseudo-random modulations reduce the maximum level of interference, they do not change its aggregate power. Considering experimental research and implementation in FPGA, we assess that offered solutions have reached level 7 of Technology readiness levels (TRLs).

The differences between the EMI emission for different RanM were not significant. However, presented modulators differed in f_{sw} distribution. The minimum value of f_{sw} affects the operating conditions of the filters and and maximum amplitude of output current ripple. The maximum value of f_{sw} frequency will be significant with the restrictions of the transistors. Keeping the average value of this frequency unchanged, we will not change the overall losses, and converter efficiency will be consistent. Therefore, by using the proposed methods (with appropriate parameters), one can achieve energy neutrality for the converter. In the future research, we are planning to investigate which shape of the frequency distribution is preferred in respect of EMI level emissions and other operation of the converter.

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Abbreviations

The following abbreviations are used in this manuscript:

AV	Average
DetM	Deterministic Modulation
DSP	Digital Signal Processors
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
FPGA	Filed-Programmable Gate Array
HSF	Harmonic Spread Factor
LGG	Linear Congruential Generator
LISN	Line Impedance Stabilization Network
PDF	Probability Density Function
QP	Quasi Peak
PWM	Pulse-Width Modulation
RanM	Pseudo-Random Modulator

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Article

Dielectric Barrier Discharge Systems with HV Generators and Discharge Chambers for Surface Treatment and Decontamination of Organic Products

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Abstract: The article presents applications of systems with power electronic converters, high voltage transformers, and discharge chambers used for nonthermal, dielectric barrier discharge plasma treatment of a plastic surface and decontamination of organic loose products. In these installations, the inductance of the high voltage transformers and the capacitances of the electrode sets form resonant circuits that are excited by inverters. The article presents characteristic features of the installations and basic mathematical relationships as well as the impact of individual parameters of system components. These converters with their output installations were designed, built, and tested by the authors. Some of the converters developed by the authors are manufactured and used in the industry.

Keywords: resonant inverter; dielectric barrier discharge; nonthermal plasma; treatment of plastic surface; decontamination of organic loose products

1. Introduction

Plasma systems and plasma treated materials are now commonly used. The cold, nonthermal plasma (NTP) is produced usually by high voltage (HV) electrical discharges. In nonthermal plasma, most of the electric energy is used to produce high-energy electrons, not to heat the gas. The electrons themselves do not treat the surface. The high-energy electrons (1–2 eV) excite electronic states of molecules, vibrational states, and provide molecular dissociation (oxygen at the most). Namely atomic oxygen and electronically excited molecules contribute to the surface treatment and pollution control. Cold plasma applications are very diverse. The main applications of NTP include surface modification of plastics [1–3], ozone generation [4,5], surface decontamination [6–11], sterilization of wounds and soil [12,13], toxic and harmful gas and sewage decomposition [14–20]. One of the methods of producing cold plasma is the dielectric barrier discharge (DBD). A number of studies present theoretical foundations of barrier discharges, including models of discharge chambers and their substitute schemes, analytical description of current and voltage waveforms, voltage-charge characteristics (the Lissajous figures) [21–24]. The article [21] additionally includes a review of the applications of DBD to high power CO_2 lasers, excimer based ultraviolet and fluorescent lamps and flat large-area plasma displays. Another important application of barrier discharges and corona discharges (CD) is the investigation of the ionic wind generation and examination of its results for the development of propulsion [25]. The use of both barrier and corona discharges when supplying a set of several

electrodes with alternating and direct voltage enables the creation of curtains from nonthermal plasma with a relatively large width of the air gap [26].

Many articles are focused on the development of high voltage generators that are components of DBD plasma systems. Depending on the application, the power of supplies ranges from single watts to hundreds of kilowatts. The choice of power and feed method is important for the operation of the DBD reactor and for the intensity of the reaction. The most common voltage waveform used to power DBD plasma reactors is the high voltage alternating current (AC) wave. In DBD reactors and in pulsed corona discharge reactors (PCD, without a dielectric layer) unipolar and bipolar voltage waves are used, sometimes a discontinuous wave with a prepolarization.

Already in 1857, Werner von Siemens reported on first experimental investigations with DBD. He applied a mechanical pulser ("Wagnerscher Hammer") interrupting the primary winding circuit of the HV transformer as the high-voltage generator [27,28]. Another simple high-voltage generator for barrier discharges can consist of an autotransformer and a high-voltage transformer fed directly from the power grid of voltage frequency 50 or 60 Hz [3]. However, the high voltage delivered to the electrodes with a frequency of 50 or 60 Hz has a much higher value than the voltage with the increased frequency generated by an inverter. Very popular solutions are voltage source inverters (VSI), with unregulated or regulated input voltage and with high voltage transformers connected to the output [22,26,29–35]. These inverters can often have a full or half-bridge structure. When supplying a DBD system from an inverter the selection of the supply frequency is associated with the resonant frequency of the transformer inductances (and additional inductances if present) and electrode set capacities. Other generator designs are also used. Low power generators can be made as fly-back converters [22,25]. Bridge converters can be equipped with snubber circuits that reduce du/dt or di/dt when transistors are switching (on/off). An interesting solution is the full-bridge in which only one branch uses the LDR (coil, diode, resistor) circuit for di/dt reduction [36]. This solution may be useful if a pulse width modulation with phase shift (PS-PWM) control is used. An example of the multiresonant generator is presented in [37]. The transformer inductances and capacitances of the electrode set (together with an additional capacitor) form one resonant circuit. Another resonant circuit provides conditions for zero current switching (ZCS) off transistors. The paper [38] describes variations of a diagonal half-bridge resonant converter topology (with four diodes and two transistors), which can be used to produce a single-period AC sinusoidal waveform. The method allows power regulation within very wide limits and makes possible the precharge pulse generation for transformer magnetization and gap voltage symmetrization. The construction of a HV generator [39,40] that allows the production of voltage waves with many different shapes is also very interesting. It consists of a 24-level cascaded H-bridge inverter and works without an HV transformer. A transformerless HV generator for DBD plasma producing is described in [41]. In the abovementioned example, the HV generator uses the phenomenon of voltage increase in a circuit under serial resonance conditions. The topology of the inverters with additional AC intermediate resonant circuits has been presented in [42]. Depending on the AC intermediate circuits these generators are characterized by properties of the current or voltage sources. In case of operation as the current source, the DBD discharges were very stable and the system was insured against arc discharges in a natural way.

The basic control methods of high voltage alternating current (HVAC) generators that are used to generate DBD plasma are described in [29,30,43]. These are pulse amplitude modulation (PAM), pulse width modulation (PWM), phase shift-pulse width modulation (PS-PWM, PSC), pulse density modulation (PDM), and pulse frequency modulation (PFM). In [31,32], the hybrid control of PDM and PFM is described.

While the above articles provide a good overview of the fundamentals of DBD discharge, their applications and HV generators design, they do not discuss the impact of individual components parameters and control variables on the power of DBD discharges. The aim of the paper at hand is to fill the gap. The discussion focusses on the following parameters: inverter input voltage, inverter output voltage frequency, DBD discharge ignition voltage, resonant circuit parameters together with

the discharge chamber model parameters and transformer ratio. This article presents DBD generators and plasma reactors used for surface treatment of plastics and decontamination of loose organic materials, developed under the supervision of the authors. Generators are presented as well as entire technological devices.

The HV generators, which the authors designed, manufactured, and tested consist of power electronics converters: rectifier, DC/DC converter (if any), voltage-source inverter, and HV transformer. Transformer leakage inductances (and additional inductances if used) form a series resonant circuit with the capacities of the electrode sets. The resonant circuits create the conditions for soft switching, which is almost lossless. Thanks to the soft switching, the converters have high efficiency and generate little radio interference. Soft switching may appear as zero current switching (ZCS) or zero voltage switching (ZVS). The ZVS will be preferred in the analyzed systems, which is characterized by lower losses in the frequency and power range that the authors are interested in (up to about 100 kHz by 0.5 kW and about 25 kHz by 10 kW of rated power).

1.1. Power Electronics Converter Topology and Their Control Methods

The topology of the used power electronics converter is presented in Figure 1. Depending on the inverter control method and the assumed power and frequency range the step-down converter and/or HF resonant choke may be omitted. Then, only the transformer leakage inductances will perform the function of a resonant choke.

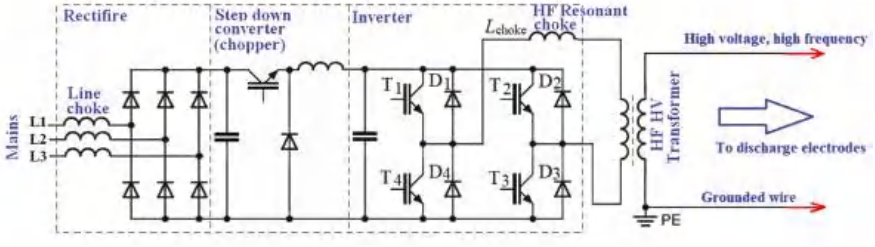

Figure 1. Schematic diagram of the power converter circuit used in the developed technological devices.

To control the output power of the converter, the following adjustment methods were considered [35]:

- pulse width modulation (PWM, with the constant inverter input voltage, the chopper can be omitted),
- changing the frequency of the inverter output (PFM, at constant inverter input voltage, the chopper can be omitted),
- changing the inverter input voltage (PAM, the chopper is necessary),
- PDM modulation (at constant inverter input voltage, the chopper can be omitted),
- combinations of the above methods.

Figure 2 shows the examples of the output current and voltage waveforms of the inverter with a series resonant circuit at the output for various analyzed control methods.

1.1.1. Output Power Control by Pulse Width Modulation, with Constant Inverter Input Voltage

Earlier studies and implementations carried out by one of the authors concerned the regulation of generator power using PWM. The chopper can be omitted to simplify the generator main circuit. This method is not recommended in the frequency range above several dozen (or even several) kHz and powers above a few kW. Turning off each of the transistors can be done "softly" (with appropriate transistors control) in the ZVS technique. However, switching on must be done "hard". Hard commutation, at high switching frequency, causes significant losses and current stress caused by the sum of the load current and the reverse current of the inverter's diodes (Figure 2a). In each half-period

of the output current, a reverse diode conducts then a transistor and then again reverse diode. There are six switching operations during the inverter operation period. This causes the inverter output voltage to oscillate at the frequency three times greater than the current wave. In the previously tested inverters, the transistors had to be oversized and the inverter was a strong source of radio frequency interference, also for its own control circuits.

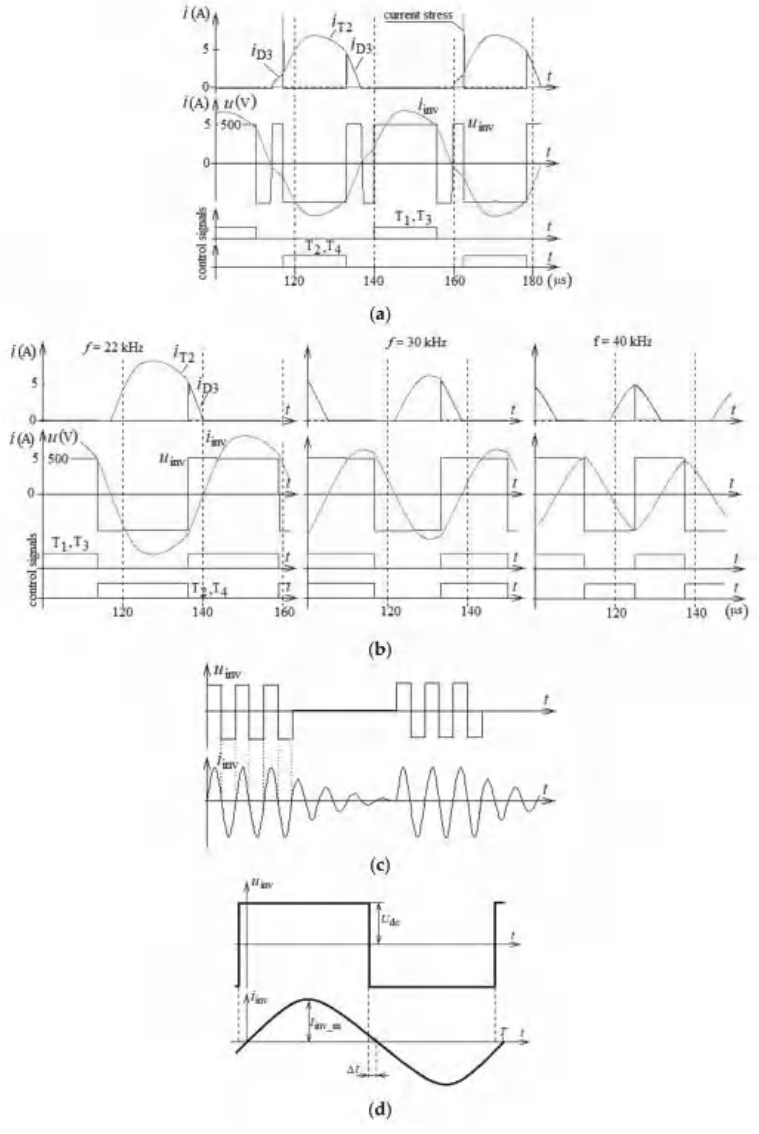

Figure 2. Waveforms of the inverter output voltage and current with different control methods, reproduced from Przegląd Elektrotechniczny [35]: (**a**) PWM, (**b**) PFM, (**c**) PDM, (**d**) PAM: i_T, i_D—transistor and diode current; i_{inv}—inverter output current; u_{inv}—inverter output voltage; for PWM, PDM, and PAM modulation it was assumed that the switching frequency is approximately equal to the resonant frequency and the voltage waveform is synchronized with the current in conditions for operation with ZVS switches.

Another kind of PWM modulation is the phase-shift pulse width modulation (PS-PWM, phase-shift control, PSC). In PS-PWM, transistors are conductive for half of the period and during diode conduction, the inverter output voltage is zero. This modulation has some advantages compared to PWM but also does not eliminate the hard switching in a wide range of power control [33,36].

1.1.2. Power Control by Pulse Frequency Modulation, with Constant Inverter Input Voltage

In this arrangement, the output power of the system is adjusted by changing the transistors switching frequency (Figure 2b). When operating below the resonant frequency, current stress in transistors occurs due to reverse currents of diodes. Thus, the authors do not recommend operating below the resonant frequency due to increased commutation losses. This method was previously used in series resonant inverters made in the thyristor technique. At the resonant frequency, the system works with maximum power. System operation (and power control) should take place at frequencies above resonance. Then ZVS conditions are created for the transistor's operation. The converter power circuit is relatively simple due to the unregulated DC voltage (no chopper). The inverter operation frequency should be limited both above and below so as not to go beyond the frequency range accepted in a given production process.

1.1.3. Power Control by Changing the Voltage at the Inverter Input

Earlier implementation carried out by one of the authors also considered regulation of generator power by changing the DC voltage supplying the inverter. This DC voltage source can be a controlled or semicontrolled thyristor rectifier, a noncontrolled rectifier with PFC converter or a transistor chopper (Figure 1). The system, although more complex, has a number of advantages. To enable the inverter transistors to work as ZVS switches, the transistors are turned off before the output current reaches zero. At the same time, if the switching frequency is close to the resonance frequency then the transistors turn off the low current. This is quasi-ZCS switching (Figure 2d). When ZVS and at the same time quasi-ZCS switching occurs, the inverter works in the most favorable conditions. Commutation losses are eliminated, and voltage and current steepness are limited. To ensure these optimal conditions it is necessary to automatically adjust the inverter switching frequency employing PLL. All power control processes take place in the chopper. Independent control of the inverter (PLL) and chopper is provided. Under these conditions, the time intervals at which energy returns to the DC source are very small. Then the amplitude, RMS, and average of the inverter output current (and transistor current) will be the lowest at the given output power. Assuming a sinusoidal current waveform and that $\Delta t << T_s$ (Figure 2d) one gets an approximate equation for the output power of the bridge inverters (Equation (1)):

$$P \approx \frac{1}{T_s/2}\int_0^{T_s/2} U_{dc} I_{inv\_m} \sin(\omega_s t) \quad dt = \frac{2U_{dc} I_{inv\_m}}{\pi} \approx 0.9 U_{dc} I_{inv\_RMS} \tag{1}$$

where: U_{dc}—DC inverter input voltage, I_{inv_m}, I_{inv_RMS}—maximum and RMS value of the inverter output current, T_s, f_s, ω_s—period, switching, and angular frequency.

1.1.4. Power Control by PDM Modulation (at Constant Inverter Input Voltage)

PDM modulation ensures even distribution of discharges over the entire length of the electrodes with a wide range of changes in average process power. The power regulation by means of PDM consists of sending in "packets" the maximum power with the frequency of a modulating generator with regulated filling [29,30,43]. The transistors in the inverter can work with ZVS soft commutation at a switching frequency greater than the resonant frequency. For maximum use of components (minimum transistors current in relation to the transferred power), the system should work with a frequency close to resonance. The general working principle is shown in Figure 2c. Turning off the "packet" is accomplished by switching on of two transistors T_1 and T_2 or T_3 and T_4. Then the

oscillations in the resonant circuit go out automatically. The generator power circuit is relatively simple due to the unregulated DC voltage. The control system should also ensure that the transformer does not saturate, regardless of the length of the "packet" of power pulses and the pause time [43]. In particular, an even number of half-waves of the inverter output voltage should be maintained. During a break in power transfer, one must remember the switching frequency to which the system tuned during power flow. Assuming a sinusoidal current waveform and that $\Delta t << T_s$ (as in Figure 2c,d), one obtains the equation for the output power of the bridge inverter:

$$P \approx \frac{2U_{dc}I_{inv\_m}}{\pi}D_{PDM} \approx 0.9U_{dc}I_{inv\_RMS}D_{PDM} \quad (2)$$

where: D_{PDM}—duty cycle of PDM.

1.1.5. Author's Method Based on Simultaneous PDM and PFM Modulation

The author's method [24,44] based on simultaneous PDM and PFM modulation differs from the methods described in [31,32]. This control method was used in DBD discharge generators manufactured and used at the Institute of Polymer Materials and Dyes Engineering (IMPIB, Toruń, Poland) [45]. The essence of this control method is the combination of PDM and PFM modulation while the inverter operation is not stopped (switching off all transistors or short-circuit state of the load) but there is a periodic increase in the switching frequency (Figure 3). The range of frequency changes is limited from above and below according to the assumed maximum and minimum power. The PDM modulating signal can have a rectangular shape with variable (Figure 3a) or with fixed (Figure 3b) filling. Limiting the maximum power protects against damage to the processed material or arcing caused by a dielectric breakdown. This control method ensures uniform discharge in a wide range of power control (about 10–100% of nominal power) and has additional advantages over the classic PDM method [31,32]. The control system does not require the use of an additional system that remembers the frequency from the moment before the inverter stops and does not require a system counting the number of half-waves of the output voltage. Another advantage is the ease of modification of existing PFM control systems to work according to the proprietary method [24].

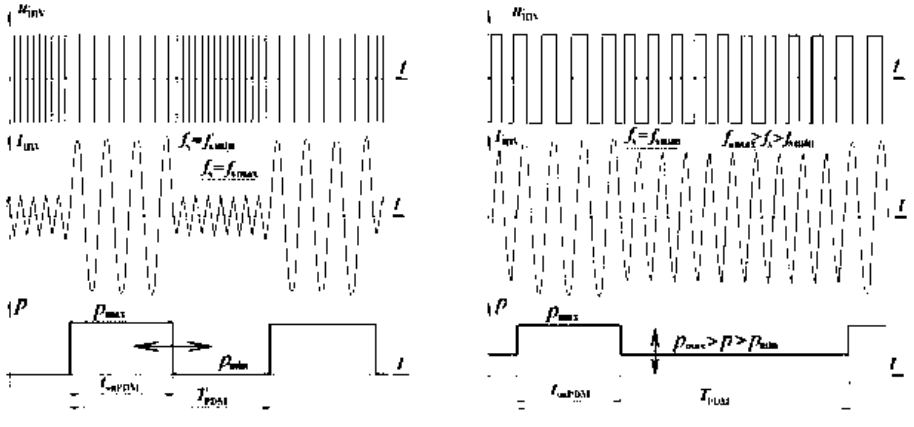

Figure 3. Examples of inverter output voltage and current waveforms using the PDM-PFM method developed by the authors: (**a**) with variable duty cycle of PDM signal, (**b**) at a constant duty cycle of PDM signal.

1.1.6. Choice of Control Method

In further projects and implementations, the PWM method was abandoned, because the inverter transistors could not work with ZVS soft commutation. The following methods were used to control HV generators for barrier discharges:

1. Power regulation by input voltage changes of the inverter (PAM, system with chopper) and switching of the inverter transistors with a frequency slightly higher than the resonant frequency. The switching frequency was tuned using the PLL loop. The inverter output voltage was ahead of the output current wave by approx. 2–3 μs. The inverter transistors switched under ZVS and almost ZCS conditions with very low commutation losses. This method of regulation ensured uniform discharges over the entire length of the electrodes in the range of 20–100% of the nominal power (P_N) of the device.
2. Power regulation by means of frequency modulation, above the resonant frequency (PFM, system without chopper), ensured the correct generation of DBD in the range of 20–100% of P_N. For a power lower than 20% of P_N, the system switched to PDM + PFM modulation according to the method developed by one of the authors. In this way, the power could be adjusted in the range of about 5–100% of P_N. This type of control ensured the operation of the inverter transistors in ZVS conditions.

2. Matching of HV Generators and DBD Reactors

Dielectric Barrier Discharges—Theoretical Basics

Figure 4 shows a simplified model of the discharge chamber. Figure 4a shows the construction ideas and Figure 4b presents simplified equivalent diagrams of the generator and the chamber. Figure 4b also contains the simplified characteristic of the barrier discharge in the air [21–24].

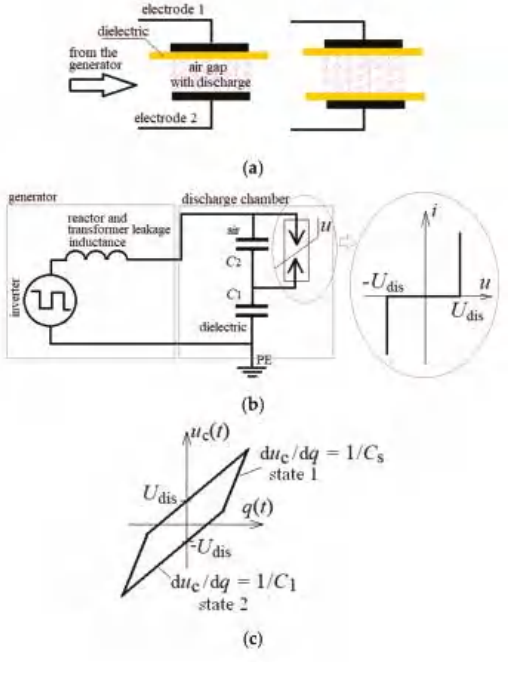

Figure 4. The idea of the construction of discharge chambers (**a**), simplified diagrams of the generator and the discharge chamber (**b**), and the trajectory of the voltage on the electrodes as a function of the charge supplied to these electrodes (**c**).

Capacities C_1, C_2 and discharge (and ignition) voltage U_{dis} depend on the shape and size of the electrodes, dielectric thickness, and its type and width of the air gap [46]. Figure 4c shows the trajectory of the voltage on the electrodes as a function of the charge supplied to these electrodes. This trajectory allows determining the capacities of the equivalent diagram and ignition voltage. To design a device for generating DBD discharges, one needs to know the parameters of the discharge chamber, transformer ratio, voltage and frequency range of the inverter output voltage, inductance in the resonant circuit.

According to the simplified scheme and the $u_C(q)$ trajectory (Figure 4b,c) one can distinguish two states in chamber operation (Figure 4c): state 1, wherein there are no discharges and state 2 in which DBD discharges occur. In state 1 the increase rate du_C/dq on the chamber terminals depends on the substitute capacity C_S made up of series-connected capacitors C_1 and C_2 (3). In state 2 the capacitor C_2 voltage does not change and the du_C/dq depends on the C_1 capacity (4). Parameters of the discharge chamber can be experimentally determined based on $u_C(q)$ trajectory (Figure 4c).

$$\frac{du_C}{dq} = \frac{1}{C_S} = \frac{C_1 + C_2}{C_1 \quad C_2} \tag{3}$$

$$\frac{du_C}{dq} = \frac{1}{C_1} \tag{4}$$

The chamber parameters related to the primary side of transformer are $C'_1 \cdot = \cdot \vartheta^2 C_1$, $C'_2 \cdot = \cdot \vartheta^2 C_2$, $C'_S \cdot = \cdot \vartheta^2 C_S$, $U_{dis} \cdot = \cdot U_{dis}/\vartheta$, where U_{dis}—discharge (and ignition) voltage, ϑ—transformation ratio. The frequency f_{syn} at which the inverter output voltage and current are synchronized is in the range $f_{r\_max} > f_{syn} > f_{r\_min}$ (Equations (5) and (6)) [34]. The synchronization frequency is the boundary of the transistors' abilities to work as ZVS or ZCS switches. The synchronization frequency f_{syn} at the rectangular inverter output voltage is only approximately equal to the resonant frequency [47].

$$f_{r\_max} = \frac{1}{2\pi\sqrt{L_r C_S \vartheta^2}} \tag{5}$$

$$f_{r\_min} = \frac{1}{2\pi\sqrt{L_r C_1 \vartheta^2}} \tag{6}$$

where $L_r = L_{choke} + L_\sigma$, L_{choke}—the additional choke (Figure 1) between the inverter output and the HV transformer, L_σ—the leakage inductance of the transformer seen from the low voltage side.

For the inverter voltage and frequency at which the capacitor C_2 voltage does not reach the U_{dis}, there are no discharges. In such conditions, the discharge chamber is a linear load. This creates a capacitor with a capacity of C_S. Capacitor C_S together with L_r creates a resonant circuit with low-pass filter properties. The shapes of electrode current and voltage are sinusoidal and the classical ac analysis can be used.

The amplitude of the capacitor C_2 voltage, which is referred to the first harmonic amplitude of the inverter output voltage is described by Equation (7), wherein U_{C2_1m}—the amplitude of the capacitor C_2 voltage, U_{inv_1m}—the first harmonic amplitude of the inverter output voltage (in the full bridge topology and a maximum duty cycle), $\omega_s = 2\pi f_s$—circular frequency of the inverter output voltage, f_s—transistors switching frequency [24,34].

$$\frac{U_{C2\_1m}/\vartheta}{U_{inv\_1m}} = \left| \frac{1}{\omega_s{}^2 L_r \quad \vartheta^2 C_S - 1} \cdot \frac{C_S}{C_2} \right| \tag{7}$$

where $U_{inv\_1m} = \frac{4}{\pi} U_{dc}$, $U_{C2m} = U_{dis} \approx U_{C2\_1m}$.

Equation (7) determines when the amplitude of the capacitor C_2 voltage reaches U_{dis}. The limit values of the switching frequencies at which the discharges appear, are determined based on Equations (8) and (9):

$$f_{s\_lim\_1} = \frac{1}{2\pi}\sqrt{\frac{1}{L_r \vartheta^2 C_2}\left(\frac{C_2}{C_S} - \frac{4}{\pi}\frac{U_{dc}}{U_{dis}/\vartheta}\right)} \quad (8)$$

$$f_{s\_lim\_2} = \frac{1}{2\pi}\sqrt{\frac{1}{L_r \vartheta^2 C_2}\left(\frac{C_2}{C_S} + \frac{4}{\pi}\frac{U_{dc}}{U_{dis}/\vartheta}\right)} \quad (9)$$

For PWM modulation, this equation is modified as shown in [29]. The discharges occur when $f_{s\_lim\_1} < f_s < f_{s\_lim\_2}$. The frequency limits depend on the capacity of the electrodes, the inductance of L_r, the discharge voltage, the inverter output voltage, and transformer winding ratio. The ratio of transformer winding has an impact on the operating frequency range and power of the device. By reducing the inverter output voltage these frequency limits approach to f_{r_max} (Equations (5) and (9)).

Figure 5a shows characteristics of discharges power as functions of frequency and inverter input voltage. Figure 5b illustrates power, current, and voltage characteristics as functions of frequency at a constant inverter input voltage (300 Vdc). Figure 5b illustrates the frequency limits according to the Equations (5), (6), (8), and (9). The characteristics from Figure 5a,b have been determined by assuming a constant value of the inductance L_r and transformer winding ratio. The following parameters of the real system (for treatment of plastic foil surface) were assumed in the simulation model: power P_N = 3 kW: $U_{dc} \approx 300$ V, two rotating electrodes: length 1700 mm, diameter 100 mm, 2 mm silicone insulation; two immovable electrodes: length 1600, width 36 mm toothed profile; air gap of approx. 2–4 mm (teeth); capacitance $C'_1 \approx 1.59$ nF, $C'_2 \approx 0.794$ nF; $L_r \approx 1.3$ mH; $\vartheta = 9.17$.

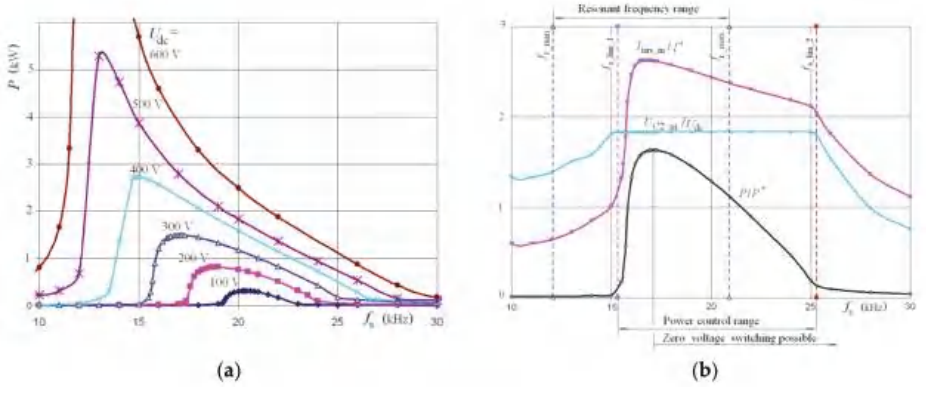

Figure 5. Characteristics of DBD discharges: (**a**) as a function of inverter output voltage and frequency, (**b**) as a function of inverter output frequency and constant inverter input voltage U_{dc} = 300 V, reproduced from Przegląd Elektrotechniczny [34]; the simulation results; base values: $I^* = U_{dc}/(L_r C_1')^{1/2}$, $P^* = U_{dc}^2/(L_r C_1')^{1/2}$.

Figure 6 shows the impact of the inductance and the transformation ratio on the frequency limits that define the range of switching frequency at the PFM modulation. The characteristics are derived by mathematical analysis (Equations (8) and (9)) for the above data. The same frequency limits were obtained by simulation. This is illustrated by the points on the curves in Figure 6. It is worth noting that experimentally measured frequencies did not diverge more than a few hundred Hz from those obtained by calculation and simulation.

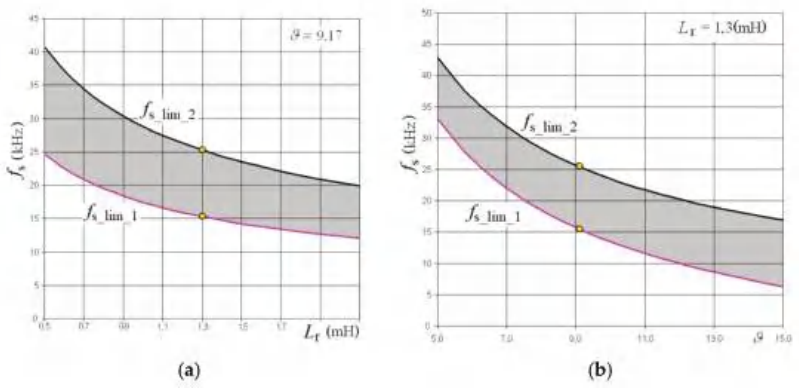

Figure 6. The range of the inverter output frequency at which the discharges appear (derived by mathematical analysis) as a function of: (**a**) inductance L_r; (**b**) transformer windings ratio, reproduced from Przegląd Elektrotechniczny [34].

Increasing demand for processing different kinds of materials with different sizes generates the need to examine the impact of the transformer windings ratio and the inductance in the treatment process. Figure 7 presents the power control characteristics for the device with the same parameters as described above. The electrodes capacitance and voltage U_{dis} are fixed. Figure 7 shows that with a change of the transformation ratio the electrode capacities and voltage U_{dis} (referred to the inverter side) also change.

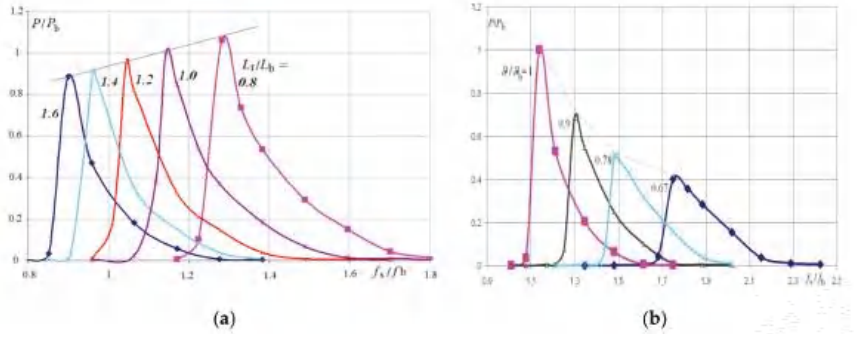

Figure 7. Relative discharge power as a function of frequency for: (**a**) various values of L_r; (**b**) various values of ϑ, reproduced from Przegląd Elektrotechniczny [34]; base values: L_b = 1 mH, ϑ_b = 9.17, $f_b = 1/(2\pi(C_1L_b)^{1/2})$.

3. Developed Prototype and Industrial Systems

3.1. Systems with Resonant Inverters for Surface Treatment (Activation) of Plastics

In order to modify the surface of plastics during printing, laminating, and gluing the DBD discharges (so-called corona treatment) are used. To achieve the desired level of adhesion the discharge energy in the range of 0.65–1.3 kJ/m^2 should be delivered. Parameters of HV generators for plastics surface treatment are generally in the range of power—0.5–10 kVA; frequency—5–50 kHz; voltage—4–20 kV. The schematic diagram of the power converter circuit used in the developed technological devices is shown in Figure 1. The idea of construction and the equivalent circuit of discharge chambers are presented in Figure 4a,b.

Figure 8 shows the construction principle of discharge chamber for foil processing, the trajectory $u(q)$ and waveforms of current, voltage, charge, and instantaneous power of the electrode set obtained experimentally. Discharges occur between the cylindrical (rotating) and rod electrode (Figure 8a). Capacitors assembly consists of the electrodes and two dielectric layers (silicon, quartz glass or ceramics, and air). The treated plastic makes the third layer of dielectric. Capacities of silicone and treated plastic foil are analyzed as one capacitor. Capacities of the electrodes and the leakage of transformer and additional choke inductances create a resonant circuit. The selection of transformer winding ratio and choke inductance allows for operating of the system in a given frequency range and assumed output power (Figures 5–7). The density of energy E/s (J/m^2) supplied to the plastic surface for the device as in Figure 8a can be determined from the equation:

$$E/s = P/(vd), \tag{10}$$

where P—DBD discharge power, v—speed of the foil, d—width of discharges (electrodes).

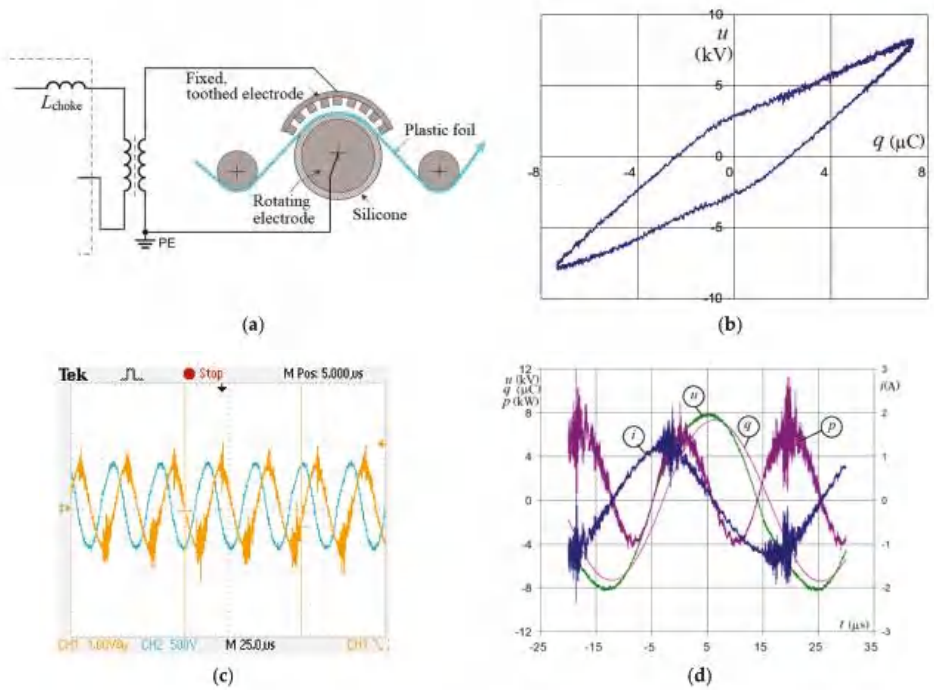

Figure 8. The discharge chamber for foil processing: (**a**) construction principle; (**b**) the trajectory $u(q)$ obtained experimentally at the frequency 26.8 kHz of the inverter output voltage and power 1.5 kW; (**c**) oscillogram of electrode current and voltage at the frequency of 26.8 kHz, CH1 1 A/div., CH2 6.25 kV/div.; (**d**) waveforms of current, voltage, charge, and instantaneous power of the electrode set obtained from the data from the oscillogram.

The waveforms of currents and voltages presented in Figure 8c were recorded using measuring devices: oscilloscope Tektronix TDS2024, current probe PA-622, high voltage differential probe P5200 with an additional voltage divider (1/12.5) at the input. The recorded data (from Figure 8c) were used to determine the trajectoryfrom Figure 8b and the waveforms from Figure 8d. Excel was used for this purpose. The capacities of C_1 and C_2 were determined on the basis of the trajectory from Figure 8b and Equations (3) and (4). In order to determine the inductance $L_r = (L_{choke} + L_\sigma)$, the secondary winding

of the HV transformer was shorted and the additional choke and the transformer were powered from the inverter at reduced voltage. The rectangular voltage wave and the triangular current waveform at the inverter output were recorded. The inductance was determined on the basis of the relationship $L_r = U_{dc}(\Delta t/\Delta i)$ where Δt is half of the period of the inverter output voltage and Δi is the current increase during this time. The determined parameters values were used during the simulation, the results of which are shown in Figures 5–7. The dimensions of the discharge chamber and the determined parameters values can be found in the description of Figure 5.

The trajectorypresented in Figure 8b prove that the model adopted for the analysis and simulation is correct for the averaged values of voltage and current of the electrodes. During the analysis and simulation with the use of this model, the electrodes current and power do not experience high-frequency oscillations visible in Figure 8c, d. This model can be used in the design and simplified analysis of the phenomena occurring in the discharge chamber. On the other hand, the oscillograms in Figure 8c, d show that many ignition and extinguishing processes occur simultaneously.

The generators for surface treatment of plastics by DBD discharge, which are described in this article, are produced now based on documentation and under the supervision of one of the authors at the Institute of Polymer Materials and Dyes Engineering (IMPiB, formerly Metalchem) in Torun, Poland [45]. Figure 9 presents the exemplary generator and discharge electrodes. The nominal powers of these generators in the range from 0.5 to 10 kW are produced.

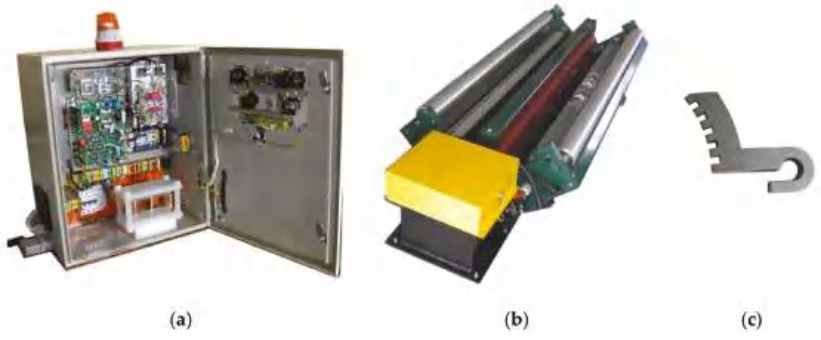

Figure 9. Construction of the devices for processing plastic film using DBD discharges: (**a**) power electronics generator with additional choke; (**b**) HV transformer and electrodes assembly, reproduced from web page IMPiB [45]; (**c**) part of the electrode.

3.2. Systems with Resonant Inverters for Decontamination of Loose Organic Material

Dielectric barrier discharges and ozone produced in this process can be used to decontaminate products such as seeds or ground dried plants. The use of plasma technologies in the food industry and agriculture has been described many times in literature [6,48–51]. However, these articles usually did not describe the construction details of plasma generators and reactors. Descriptions of some reactor designs can be found in patents [10,11]. The description of the DBD generation is analogous to the generation for surface treatment of plastics. However, the constructions of the discharge chambers are different. Figure 10 presents an equivalent diagram of part of the generator with HV transformer and construction of two types of discharge chambers for decontamination of loose organic material. The prototypes according to Figure 10b,c were built and tested under the supervision of one of the authors [7]. The first chamber (Figure 10b) has one fixed electrode, and the other in the form of a movable trolley that performs reciprocating movements transporting the treated organic material. The second version (Figure 10c) has two rotary electrodes in the form of cylinders between which the processed material is decontaminated.

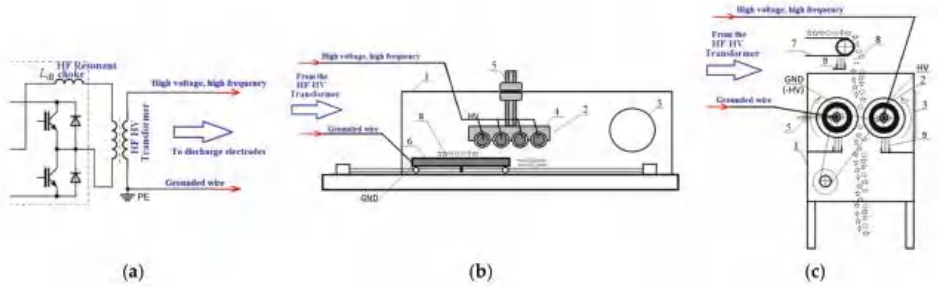

Figure 10. Construction of the devices for decontamination of loose organic material using DBD discharges: (**a**) equivalent diagram of part of a generator with transformer; (**b**) discharge chamber with a sliding electrode; (**c**) discharge chamber with rotating electrodes; 1—discharge chamber, 2—electrodes assembly, 3—suction hole, 4—insulating support, 5—electrodes gap adjustment knob, 6—transport trolley, 7—belt conveyor, 8—processed material, 9—sweeper.

New reactor designs were developed to increase the discharge power and thus to reduce the plasma exposure time and speed up the technological process. Plasma processing time is short compared with other known solutions [10]. Figure 11 shows two types of prototypes of devices for decontamination of crushed dried plants.

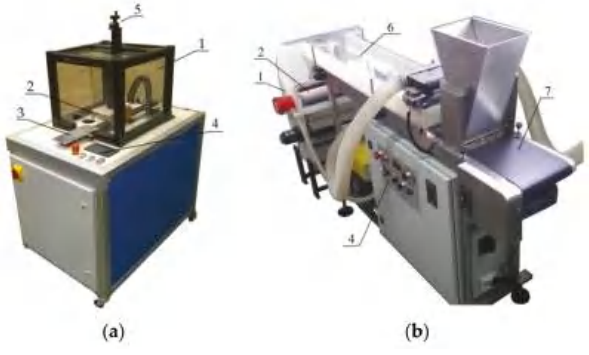

Figure 11. View of devices for decontamination of loose organic materials using DBD discharges developed and tested by the authors: (**a**) device with a sliding electrode; (**b**) device with rotating electrodes; 1—discharge chamber, 2—electrodes assembly, 3—transport trolley, 4—operator panel, 5—electrodes gap adjustment knob, 6—ozone chamber, 7—belt conveyor.

Figure 11b shows a solution that can be part of a technological line. This design is equipped with a support decontamination system which uses ozone generated in the discharge chamber. The conveyor speed determines the remaining time of the processed material in the ozone chamber. Electrodes in the form of rotating cylinders provide better cooling conditions than fixed electrodes. To increase the plasma operating time, the chamber may consist of several electrode assemblies. The implementation of such devices for the food industry is envisaged.

The power of discharges was regulated in the range of 200–1000 W by PFM or PDM + PFM modulation. The PDM + PFM modulation was used in the power range of 200–300 W to ensure even discharges over the entire length of the electrodes at low power. The decontamination efficiency of these prototypes was tested at the Faculty of Agriculture and Biotechnology of the UTP University in Bydgoszcz. The tests [52] confirm the effectiveness of DBD plasma and ozone in reducing microbial contamination of dried fragmented plants.

4. Conclusions

The article considers the most common problems concerning a proper matching of HV generators and DBD reactors It focused on parameters of electrodes sets (equivalent capacitance, discharge voltage), generator parameters (frequency and output voltage, modulation methods), transformer parameters (transformation ratio, leakage inductances), and the resonant circuit choke inductance. Thus, the article contributes knowledge to designing equipment for surface treatment of plastics and for decontamination by DBD method.

A common feature of the presented systems is that the transistors of the inverters work with the ZVS soft commutation in the whole range of power regulation. In the case of PAM + PFM modulation, the transistors work with ZVS and "almost" ZCS commutation, which radically reduces switching losses. Resonant converters created in this way had better parameters than similar systems in which transistors operated with hard commutation. This concerned parameters such as efficiency and generation of radioelectric disturbances.

The innovative solutions presented in the article are the inverters for DBD plasma generators, which use the proprietary PDM + PFM modulation method. This method ensures the extension of the power regulation range and maintaining the uniformity of discharges in DBD devices for plastic surface treatment and decontamination. The generators were built using the theoretical considerations presented in this article. New designs of discharge chambers for decontamination have been developed. They have been reserved in the European patent office. The innovative solution of the first structure, with a movable GND electrode, is the ability to precisely select the dose of energy and decontamination conditions by adjusting the discharge power, the distance between the electrodes, the speed of the trolley with the GND electrode, the number of runs of the trolley during processing. An innovative solution of the second design is, among others, the use of rotating cylindrical electrodes, which improves cooling conditions and the use of ozone produced in the process for initial decontamination.

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