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A Family of Single-Stage, Buck-Boost Inverters for Photovoltaic Applications

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Abstract: This paper introduces a family of single-stage buck-boost DC/AC inverters for photovoltaic (PV) applications. The high-gain feature was attained by applying a multi-winding tapped inductor, and thus, the proposed topologies can generate a grid-level AC output voltage without using additional high step-up stages. The proposed topologies had a low component count and consisted of a single magnetic device and three or four power switches. Moreover, the switches were assembled in a push-pull or half/full-bridge arrangement, which allowed using commercial low-cost driver-integrated circuits. In this paper, the operation principle and comparison of the proposed topologies are presented. The feasibility of the proposed topologies was verified by simulations and experimental tests.

Keywords: PV microinverters; converter topologies; single-stage; buck-boost; tapped inductor

1. Introduction

The continuous development of distributed photovoltaic (PV) power generation systems arouses much interest in MIEs/MICs, also known as microinverters. Unlike the string inverters using series-connected PV panels to achieve a high voltage, microinverters are designed to directly connect a single PV panel with a low voltage to the grid while providing an individual MPPT and, in turn, avoiding mismatch losses within the PV array. The "plug-and-play" feature of the microinverter allows the incorporation of PV modules of different types into a single array, also facilitating its future expansion and maintenance. To some extent, the labor cost can also be reduced.

In practice, the low DC voltage produced by the PV module (e.g., 20–30 V) and the relatively high AC voltage of the utility (e.g., 230 V RMS) imply that a high step-up DC-DC stage followed by a regular inverter is required. Such a straightforward scheme is referred to as the two-stage approach and is quite popular due to its ease of implementation and control. Yet, the two-stage solution is costly and the efficiency is reduced. The single-stage microinverter that combines both the voltage step-up and inversion functions in one power stage can possibly lead to a lower component count and a reduced cost. Thus, the single-stage inverters have been the focus of recent research activities. Numerous single-stage boost-derived topologies have been proposed in the literature due to the inherent voltage step-up capability [1]. The limited voltage gain of the boost-type converter can be improved by means of integrating tapped inductors, as discussed in [2,3].

Additionally, due to the voltage step-up/down capability, the buck-boost derived topologies can also be a viable solution for single-stage inverter applications. Thus, a number of buck-boost type single-stage inverters with low component counts were reported. For instance, single-stage buck-boost inverters with only three switches were proposed in [4,5], as shown in Figure 1a, where a tapped inductor was used as a regular inductor in one half-line cycle and as a fly-back transformer in the subsequent half-line

cycle. Unfortunately, this type of inverter cannot attain the required voltage step-up. As shown in Figure 1b, a four-switch, single-stage, buck-boost inverter was then presented in [6], which employed a tapped inductor and the SEPIC converter to increase the voltage gain. However, according to the operational principles, the turns ratio of the tapped inductor has to be equal to unity, and consequently, the voltage gain is still limited. Topologies in [7,8] also have only four switches to realize the single-stage conversion and have the merit of a common terminal between input and output ports. Figure 1c shows the circuit diagram of the converter in [7]. Another single-stage, buck-boost inverter has the advantage of reduced magnetic volume and low leakage currents [9]. The topologies in [10–12] were conceived to also eliminate the leakage currents, but the number of active switches is increased, as observed in Figure 1d. Furthermore, a differential buck-boost inverter with active power decoupling capability was proposed in [13,14], where no extra components are required. It has only four switches; on the contrary, a rather complicated control method is needed. An active buck-boost inverter using an "AC/AC unit" to realize the buck-boost conversion was introduced in [15,16], as presented in Figure 1e. Yet, each unit consisted of four switches, and, thus, in total, eight switches are needed for the microinverter. The authors of [17] expanded this idea to cascaded multilevel buck-boost inverters using H-bridges for each PV panel and a central AC/AC unit. To improve the efficiency and system reliability, a solution for the current shoot-through issue was discussed in [18,19] to eliminate the dead-time effect. Moreover, ref. [18] presented a converter with eight switches and four inductors, while [19] has four switches, four diodes, and six inductors, which make the topologies quite complicated. The topology in [20] has merits of a wide input voltage range, low leakage currents, small grid current ripples, and low common-mode voltages. However, as seen in Figure 1f, it has four high-frequency switches and two bidirectional switches, which are realized by connecting back-to-back MOSFETs in series. Doing so significantly increases the total number of switches (i.e., eight). Although the ideas of [4–20] are very interesting, their attained voltage gain is comparable to the traditional buck-boost converter.

Additional attempts to increase the gain of the buck-boost derived topologies were reported. For example, in [21] a series connection between a buck-boost converter and the PV array was introduced to have a higher gain, but the gain improvement was limited. The topology in [22], see Figure 2a, employed a switched inductor, which can improve the gain by the factor of $\sqrt{2}$ over that of the traditional buck-boost converter. However, in total, the topology in [22] had four switches, eight diodes, and four inductors. The tapped-inductor buck-boost inverter topologies presented in [23,24], as shown in Figure 2b,c, respectively, can achieve a much higher voltage gain than the traditional ones, but the switch counts were up to eight, whereas [25,26] had five switches, as presented in Figure 2d. The advantage of the topologies in [25,26] is that only one high-frequency switch was used, and thus, the switching losses were lower. For the topologies in Figure 2, the main characteristics are further compared in Table 1. According to Table 1, most of the topologies had a high semiconductor count, from 7 up to 12. The experimental efficiency of more than 96% was reported in [23]. However, the test was with an input of 100–200 V and a 110-V output, which cannot support the performance with a high-voltage step-up. An efficiency of 86% was achieved in [25] with a 60-V input, a 230-V output, and 100-W output power, which is reasonable for a tapped-inductor buck-boost inverter. Yet, the experimental efficiency of the other two proposals was not reported clearly in the literature.

Table 1. Comparison of the main topologies of the existing single-stage, buck-boost inverters.

Ref.	Switches Count	Diodes Count	Inductors Count	Input Voltage	Output Voltage	Output Power	Efficiency
[22]	4	8	4	20 V	314 V	100 W	/
[23]	8	0	1 Tapped	100–200 V	110 V	500 W	>96%
Figure 2b [24]	8	0	1 Tapped	40 V	230 V	/	/
[25]	5	2	1 Tapped	60 V	230 V	100 W	86%

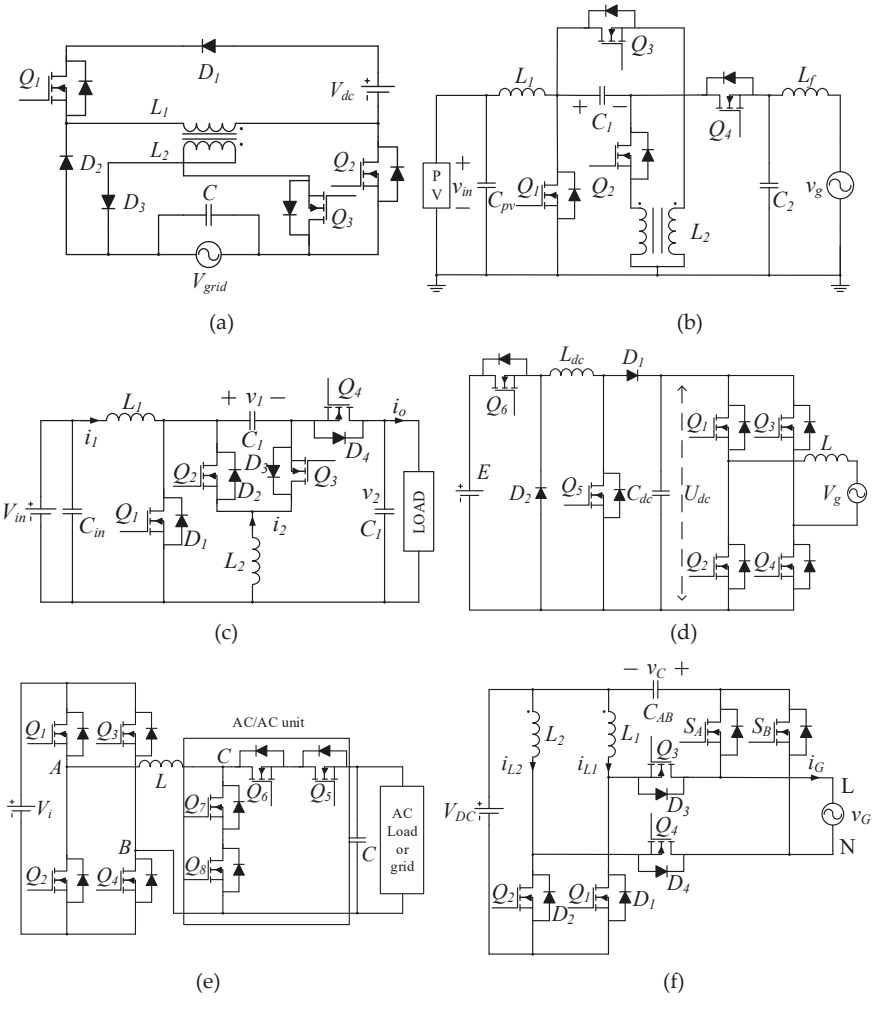


Figure 1. Prior-art, single-stage, buck-boost inverters: (**a**) [5], (**b**) [6], (**c**) [7], (**d**) [12], (**e**) [15], and (**f**) [20].

The high switch count of the reviewed converters, the resulting circuit complexity, higher cost, and lower efficiency, counter the main design goal of producing a simple and low-cost single-stage inverter. Therefore, more efforts have been made to develop more single-stage, buck-boost inverter topologies with a high gain and a low switch count. Recently, a family of single-stage, buck-boost rectifiers with high power factor were proposed in [27], analyzed, and verified in [28]. With the same principles, a family of tapped-inductor, buck-boost microinverters can be derived by reversing the power flow. This calls for the application of bidirectional switches. The proposed tapped-inductor, buck-boost type inverter family is illustrated in Figure 3. The basic operation and the preliminary simulation study of the two topologies in the family were reported in [29,30], while the converters have not been experimentally verified, and the design considerations are not fully addressed.

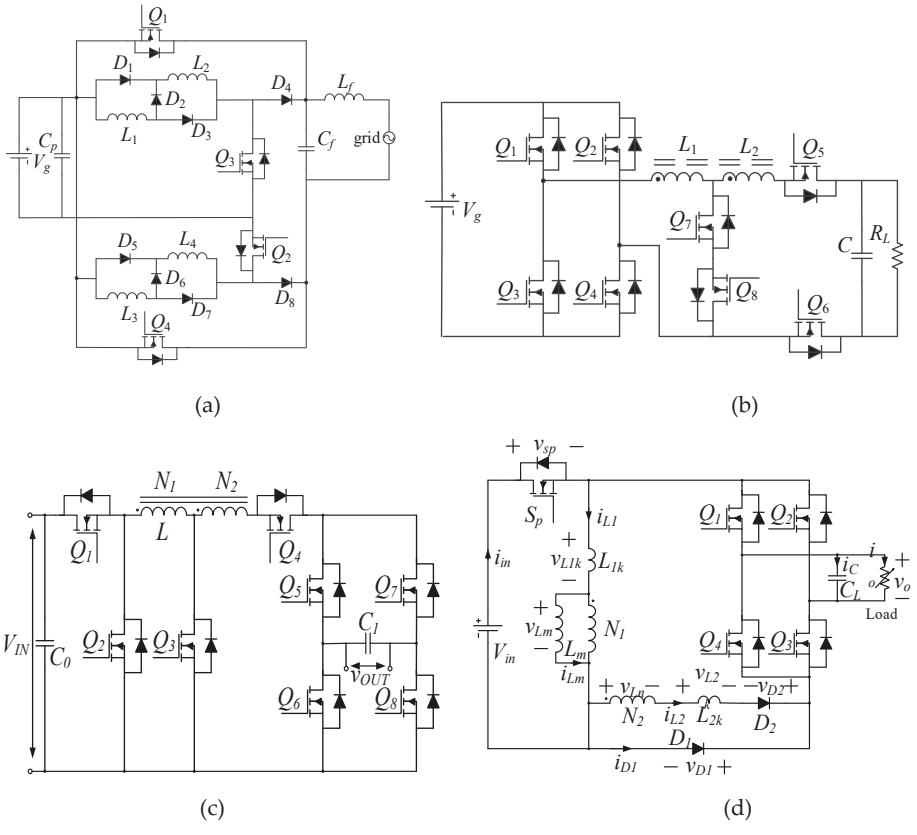
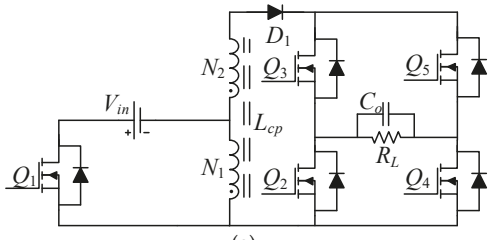
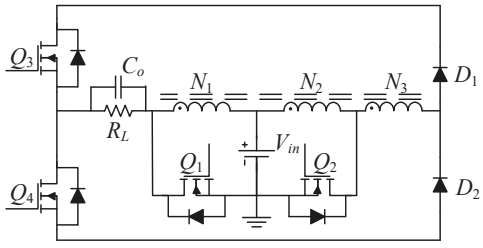


Figure 2. Prior-art, single-stage, buck-boost inverters with high gains: (**a**) [22], (**b**) [23], (**c**) [24], and (**d**) [25].

Accordingly, in addition to the topologies in [29,30], this paper further introduces two more practical topologies and all four topologies in the family are presented in detail. More importantly, a comparison of the proposed family was done thoroughly in terms of the component count, the voltage conversion ratio, the voltage stress, the peak current stress, and the RMS current stress, which can be used in the design phase. What is more, more detailed simulation studies for all the topologies in the family were presented. A prototype of the SSBBI of the proposed family was built and experimental results are illustrated in this paper. The rest of the paper is organized as follows. Section 2 introduces the proposed family, and the operation principles of the proposed family are demonstrated on a topology (i.e., the SSBBI) in Section 3. Circuit characteristics are discussed in Section 4, including the analysis of the conversion ratio, turns ratio, and duty cycle constraints together with voltage and current stresses, as design considerations. Simulation results are given in Section 5, where the comparison of the family is provided. Experimental tests are presented in Section 6 to validate the discussion. Finally, concluding remarks are provided in Section 7.



(**a**)



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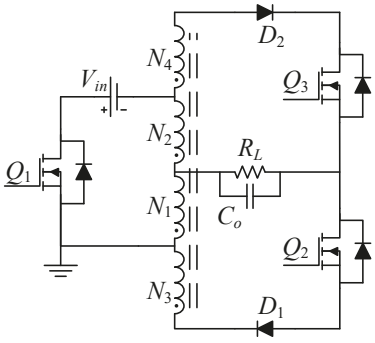

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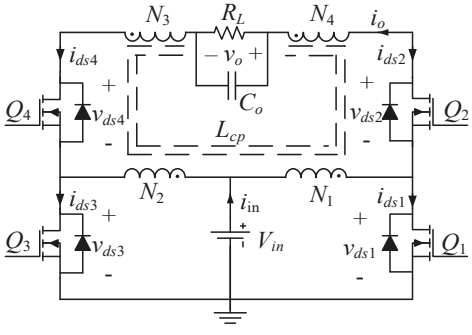


(**d**)

Figure 3. Proposed family of single-stage, buck-boost inverters: (**a**) Variant 1, (**b**) Variant 2, (**c**) Variant 3, (**d**) Variant 4 (SSBBI).

2. Single-Stage, Buck-Boost Inverter Family

As shown in Figure 3, the proposed inverter family makes use of a tapped inductor to attain a high step-up voltage conversion ratio. This helps to generate a grid-compatible voltage from a low DC voltage source. Two, three, and four winding, tapped-inductor structures are needed. The turns ratio, n, of the tapped inductor is defined as follows. For the two-windings inverter topology in Figure 3a, $n = N_2/N_1$. The three-windings topology in Figure 3b has an equal number of primary turns, $N_1 = N_2$, and the turns ratio is defined as $n = N_3/N_1 = N_3/N_2$. The topologies in Figure 3c,d rely on a symmetrical tapped-inductor structure with an equal turns ratio, defined as $n = N_3/N_1 = N_4/N_2$.

The topology in Figure 3a includes a floating source, a single ground-referenced PWM switch, Q_1, and a ground-referenced line frequency unfolding bridge, Q_2–Q_5. The topology in Figure 3b includes a grounded source, a ground-referenced push-pull pair of PWM switches, Q_1–Q_2, and a floating line frequency unfolding totem pole, Q_3–Q_4. The topology in Figure 3c includes a floating source, a single ground-referenced PWM switch, Q_1, and a floating line frequency unfolding totem pole, Q_2–Q_3. The topology in Figure 3d includes a grounded source and a ground-referenced full bridge. Here, the lower switches, Q_1–Q_3, are PWM devices, whereas the high switch pair can perform either a simple line frequency unfolding function or be operated as synchronous rectifiers. Since the body diodes of the high switches are exploited as rectifiers, the reverse recovery capability should be considered. This can be an issue for silicon-based devices, while the emerging GaN MOSFETs can deliver the required performance.

To summarize, the proposed inverters have the merits of:

(1) Generating a grid-level AC output voltage from a relatively low DC input voltage without extra high gain DC-DC converters.
(2) Having a low component count as single-stage topologies consisting of a single magnetic device and three or four switches.
(3) A push-pull or half/full-bridge arrangement of the switches, where the commercial low-cost driver-integrated circuits can be easily used.

The proposed tapped-inductor, buck-boost inverter family in Figure 3 was then studied through simulations. The exploration indicated that the topology in Figure 3d can also help to avoid much of the practical grounding, driving, and controller interface issues. Additionally, considering the lowest semiconductor count (see Table 2), the topology in Figure 3d appears as the most attractive candidate in the family. Hereafter, this topology (i.e., the SSBBI in Figure 3d) is considered in the following detailed analysis to exemplify the converter operation.

Table 2. Comparison of the component count of the tapped-inductor, buck-boost inverter family.

Topologies	Switches	Diodes	Windings	Filter Cap.
Figure 3a	5	1	2	1
Figure 3b	4	2	3	1
Figure 3c	3	2	4	1
Figure 3d	4	0	4	1

3. Operation Principles of the Proposed SSBBI

As shown in Figure 3d, the power stage of the proposed SSBBI included four switches, Q_1–Q_4, in a full-bridge arrangement. A tapped inductor, L_{cp}, with four windings was employed. The output filter capacitor here was C_o and the load was an equivalent resistance, R_L, for stand-alone applications. The voltage across them was the AC output, v_o. As mentioned previously, two symmetrical pairs of windings were used for the tapped inductor. The turns of the primary windings must be the same, i.e., $N_1 = N_2$. Similarly, equal secondary windings were used, i.e., $N_3 = N_4$. The turns ratio of the tapped inductor was then obtained as $n = N_3/N_1 = N_4/N_2$. The SSBBI can generate a bipolar output voltage

with the help of the symmetrical structure, and thus, it can achieve the DC-AC inversion. The desired output voltage can be obtained using any common control strategy of a constant frequency duty cycle. The operation principle is detailed in the following.

Supposing the converter was operating in the CCM, the SSBBI had two switching states in each half-line cycle, denoted as states A and B in the positive half-line cycle and A′ and B′ in the negative half-line cycle. The switching states of the four switches are listed in Table 3, and further illustrated in Figure 4.

Table 3. Switching states of semiconductor devices.

Switches	Positive Output Voltage		Negative Output Voltage	
	State A	State B	State A′	State B′
Q_1	On	Off	Off	Off
Q_2	Off	On	On	On
Q_3	Off	Off	On	Off
Q_4	On	On	Off	On

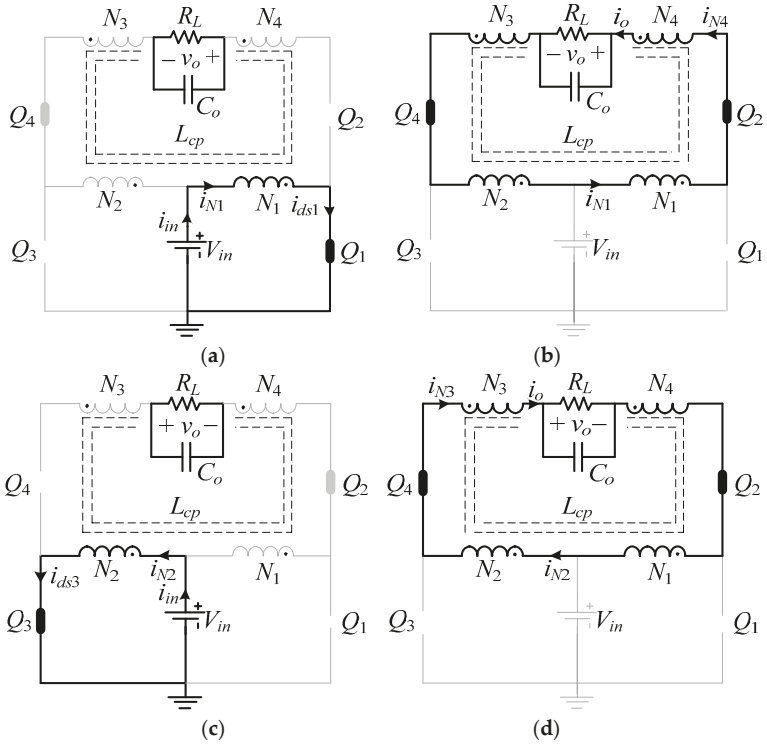


Figure 4. Equivalent circuits (switching states) of the proposed SSBBI: (**a**) State A, (**b**) State B, (**c**) State A′, (**d**) State B′.

According to the equivalent circuit of state A shown in Figure 4a, the state started at the beginning of each switching cycle in the positive half-line cycle. Here, the switch Q_1 was turned on and the state lasted for the duration of DT_s. In this state, the tapped inductor was charged by the input source, V_{in}, through the primary winding N_1. The output capacitor, C_o, can sustain the output voltage on the load. As shown in Figure 4b, state B began when the switch Q_1 was turned off and lasted for the duration of

$(1 - D)T_s$. In this state, the energy stored in the tapped inductor was discharged and released to the output side through all the four windings of the tapped inductor. During states A and B, when the output voltage was positive, Q_1 and Q_2 were switched, while the switch Q_3 was maintained off and Q_4 remained on. In comparison, the states A and B were replaced by the states A' and B' during the negative output half-line cycle due to the symmetrical operation principle. The equivalent circuits of state A' and B' are shown in Figure 4c,d, respectively.

The key waveforms of the SSBBI are described in Figure 5, where S_{Q1}–S_{Q4} are the gating signals for Q_1–Q_4 switches, respectively. Due to the symmetry of the SSBBI, it was sufficient to consider its operation during the positive half cycle. When Q_1 was turned on and Q_2 was turned off, the primary winding of the tapped inductor was energized. This caused the magnetizing current of the tapped inductor to ramp up. When Q_1 was turned off and Q_2 was turned on, the tapped inductor was discharged to support the output through all the windings. Thus, the magnetizing current of the tapped inductor ramped down. Notably, in terms of control of the converter, in grid-tied applications, the task of the control circuit is to shape the average output current, I_o, into a sinusoidal waveform (see i_{N4} in Figure 5), while the controller should regulate the output voltage in stand-alone applications.

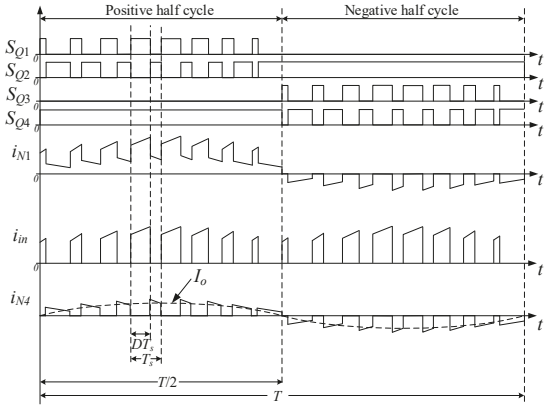


Figure 5. Illustration of key waveforms of the proposed SSBBI.

4. Analysis and Design Considerations of the Proposed SSBBI

4.1. CCM Voltage Gain

In the CCM, the tapped inductor, L_{cp}, was charged by the input voltage source, V_{in}, only through the primary winding N_1 or N_2 during the time of DT_s (state A or A'). However, the output voltage, v_o was stressed on all the four windings of the tapped inductor during the time of $(1 - D)T_s$ (state B or B'). Thus, according to the volt-sec balance, it gives

$$\int_0^{DT_s} V_{in}dt + \int_{DT_s}^{T_s} \frac{-v_o}{2n+2}dt = 0 \tag{1}$$

which led to that the quasi-steady-state voltage gain of the SSBBI to be calculated as

$$M = \frac{v_o}{V_{in}} = 2(n+1)\frac{D}{1-D}. \tag{2}$$

It can be recognized from Equation (2) that the SSBBI was a buck-boost type topology and had the function of voltage step-up/down. A higher gain can be achieved by choosing a proper turns ratio, n.

4.2. Turns Ratio and Duty Cycle Constraints

It should be noticed that when the tapped inductor is discharged to the output side (see states B and B'), the voltage across the primary winding must be always less than the DC input voltage, V_{in}. Accordingly,

$$\frac{v_o}{2(n+1)} < V_{in}. \tag{3}$$

In this way, it prevented the discharging current of the tapped inductor to go back to the DC input source through the body diode of the switch at the lower side. Such a condition should be avoided since the output voltage would be clamped and the circulating current will lower the efficiency as well. With this concern, the turns ratio should be designed sufficiently large to make the SSBBI work properly. Thus,

$$n > \frac{V_{o\max}}{2V_{in}} - 1. \tag{4}$$

Moreover, it can be obtained by combining (2) and (3) that

$$\frac{D}{1-D} < 1. \tag{5}$$

Subsequently, the maximum duty ratio, $D_{\max}$, should be limited to

$$D_{\max} < 0.5. \tag{6}$$

4.3. Voltage and Current Stress

4.3.1. Voltage Stress of Switches

During state A, the input voltage, V_{in}, was imposed on the primary winding N_1 of the tapped inductor when the switch Q_1 was on. Therefore, the voltage stress on the switch Q_3 was the sum of the input voltage and the induced voltage across the primary winding N_2, which was twice the input voltage, V_{in} *as*

$$V_{Q3\max} = 2V_{in}. \tag{7}$$

Meanwhile, since the switch Q_4 was in on-state, the voltage across the four windings of the tapped inductor as well as the output voltage, v_o, was stressed on the off-state switch Q_2. Thus, the maximum stress of the Q_2 will lead to:

$$V_{Q2\max} = 2(n+1)V_{in} + V_{o\max}. \tag{8}$$

The same results can be obtained for the switches Q_1 and Q_4 in state A' because of the symmetrical operation of the SSBBI. The voltage stresses for all the switches are summarized in Table 4.

Table 4. SSBBI switch voltage and current stresses.

Switches	Voltage Stress	Current Stress	
		Peak	RMS
Q_1, Q_3	$2V_{in}$	$2(n+1)I_m + \frac{I_m V_m}{V_{in}}$	$I_{acrms}\sqrt{\frac{3}{8}\frac{V_m^2}{V_{in}^2} + \frac{8}{3\pi}\frac{(n+1)V_m}{V_{in}}}$
Q_2, Q_4	$2(n+1)V_{in}+V_{o\max}$	$I_m + \frac{I_m V_m}{2(n+1)V_{in}}$	$I_{acrms}\sqrt{1 + \frac{4}{3\pi}\frac{V_m}{(n+1)V_{in}}}$

4.3.2. Analysis of Current Stress

It was assumed that the output voltage and current of the SSBBI were ideally in phase without harmonics as

$$\begin{cases} v_o(t) = V_m \sin \omega t \\ i_o(t) = I_m \sin \omega t \end{cases} \tag{9}$$

Furthermore, by applying Equations (2) and (9), and replacing the steady-state duty ratio D with the time-varying duty ratio $d(t)$, it can be obtained that

$$\frac{v_o(t)}{V_{in}} = 2(n+1)\frac{d(t)}{1-d(t)} = \frac{V_m \sin \omega t}{V_{in}} \tag{10}$$

from which the duty ratio, $d(t)$, can be derived as

$$d(t) = \frac{V_m \sin \omega t}{2(n+1)V_{in} + V_m \sin \omega t}. \tag{11}$$

For the proposed SSBBI, the average output current equaled to the average current of the upper switch, $\langle i_o(t) \rangle = i_{Q2}(t)[1 - d(t)]$, as shown in Figure 6. Therefore, assuming that the current ripples are negligible, the current amplitude of the switch Q_2 can be obtained by combining Equations (9) and (11) as

$$i_{Q2}(t) = \frac{\langle i_o(t) \rangle}{1-d(t)} = I_m \sin \omega t + \frac{I_m V_m \sin^2 \omega t}{2(n+1)V_{in}}. \tag{12}$$

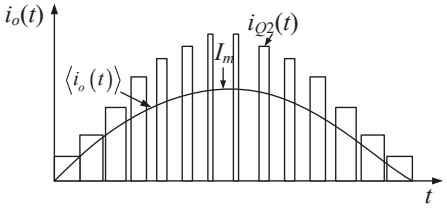


Figure 6. Illustration of the switch current, $i_Q(t)$, and the average output current, $<i_o(t)>$, throughout the half-line cycle.

Thus, the maximum current of the switch Q_2 at the peak output voltage can be obtained as

$$I_{Q2\max} = I_m + \frac{I_m V_m}{2(n+1)V_{in}}. \tag{13}$$

The squared RMS current of the switch Q_2 within a switching period is:

$$i^2_{Q2rmsTs} = \frac{1}{T_s}\int_t^{t+T_s} i^2_{Q2}(t)dt = [1-d(t)]i^2_{Q2}(t). \tag{14}$$

Subsequently, the squared value of the switch RMS current is:

$$I^2_{Q2rms} = \frac{1}{T/2}\int_0^{T/2} i^2_{Q2rmsTs}dt \tag{15}$$

with T being the generated output voltage period. Substituting Equations (11), (12), and (14) into (15) yields

$$I^2_{Q2rms} = \frac{1}{T/2}\int_0^{T/2} I^2_m \sin^2 \omega t + \frac{I^2_m V_m \sin^3 \omega t}{2(n+1)V_{in}}dt = I^2_{acrms}\left(1 + \frac{4}{3\pi}\frac{V_m}{(n+1)V_{in}}\right). \tag{16}$$

Thus, the RMS current of the switch Q_2 is obtained as

$$I_{Q2rms} = I_{acrms}\sqrt{1 + \frac{4}{3\pi}\frac{V_m}{(n+1)V_{in}}}. \tag{17}$$

The current amplitude of the lower switch Q_1 is $2(n + 1)$ times higher than the upper switch current due to the function of the tapped-inductor turns ratio, n. Thus,

$$i_{Q1}(t) = 2(n+1)i_{Q2}(t) = 2(n+1)I_m \sin \omega t + \frac{I_m V_m \sin^2 \omega t}{V_{in}}. \quad (18)$$

Therefore, the peak current through the lower switch, Q_1, is:

$$i_{Q1\max} = 2(n+1)I_m + \frac{I_m V_m}{V_{in}}. \quad (19)$$

The squared value of the lower switch RMS current through the switching period, T_s, is:

$$i^2_{Q1rmsTs} = \frac{1}{T_s}\int_t^{t+T_s} i^2_{Q1}(t)dt = d(t)i^2_{Q1}(t). \quad (20)$$

Since the low switch conducts for half the line period, the squared value of its RMS current on the line period scale can be calculated as:

$$I^2_{Q1rms} = \frac{1}{T}\int_0^T i^2_{Q1rmsTs}dt. \quad (21)$$

Substituting Equations (11), (18), and (20) into (21), gives

$$I_{Q1rms} = I_{acrms}\sqrt{\frac{3}{8}\frac{V_m^2}{V_g^2} + \frac{8}{3\pi}\frac{(n+1)V_m}{V_{in}}}. \quad (22)$$

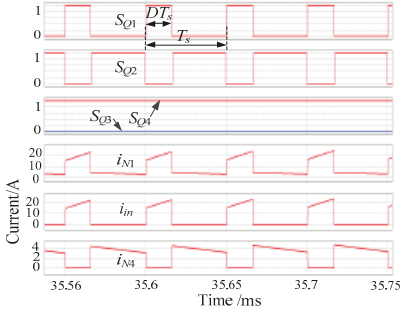
With the above analysis, the voltage and current stresses of the SSBBI are summarized in Table 4.

5. Simulation Results and Comparison

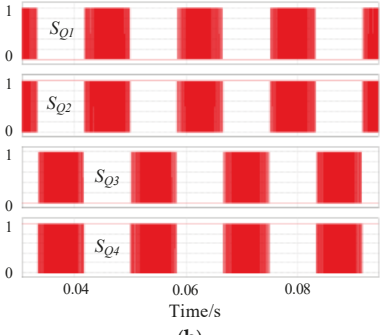
5.1. Basic System Operation

Referring to Figure 3d, simulations were carried out to verify the feasibility of the proposed SSBBI in PSIM software. The key simulation parameters were: Output power P_o = 200 W, input voltage V_{in} = 48 V, output voltage v_o = 110 V/60 Hz, switching frequency f_s = 20 kHz, tapped-inductor magnetizing inductance L_m = 150 µH, turns ratio n = 1.5, and output capacitance C_o = 2 µF. Several control strategies can be applied to control the proposed SSBBI. Initially, to validate the basic operational principle, the simple open-loop SPWM was used. Simulation results are shown in Figure 7, which demonstrates that the SSBBI can generate the desired output voltage. This provides proof of concept of the proposed circuit family for single-stage microinverter applications.

Furthermore, as can be observed in Figure 7a, the circuit simulation results (key waveforms) were in a close agreement with the analytical results in Figure 5. The gate-driving signals are further shown in Figure 7b to demonstrate the controllability of the converter. Moreover, the output voltage of the proposed inverter is given in Figure 7c, as well as the voltage across the switches. It can be observed in Figure 7c that the SSBI can produce high-quality sinusoidal outputs, and the voltage stresses on the switches were also in consistency with the analysis. Additionally, the currents flowing through the power devices under the 200-W output power are presented in Figure 7d, which again agrees with the theoretical analysis presented in Section 4.



(**a**)



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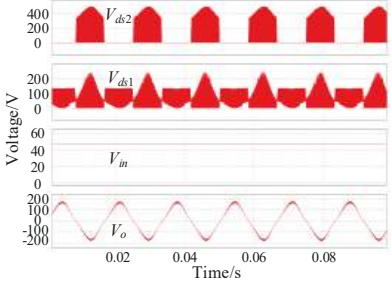

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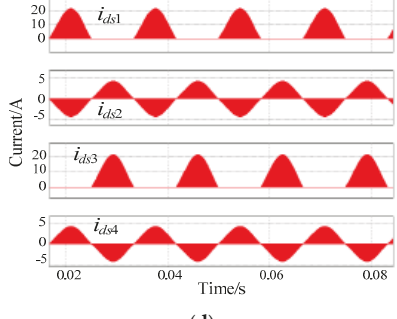
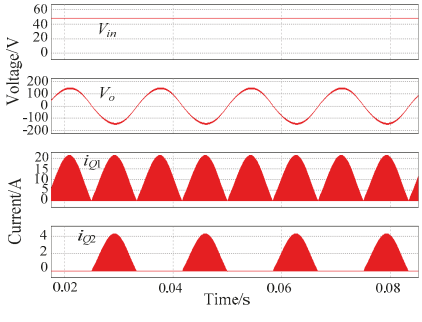


(**d**)

Figure 7. Key simulation waveforms of the proposed SSBBI: (**a**) Driving signal and currents on the switching period scale; (**b**) driving signals for switches; (**c**) V_{ds} of the switches in one leg, input, and output voltage; (**d**) switch currents on the output period scale.

The analytical results were further verified by simulations. Key simulated waveforms of the proposed topologies in Figure 3a–c are shown in Figure 8. It is observed in Figure 8 that all the topologies of the proposed family can generate a good-quality sinusoidal output voltage. Simulations also support the theoretically predicted results of the current stress analysis. When comparing the performance of the topologies in Figure 3a–c with the SSBBI, it can be seen that the four topologies had similar high-quality output voltage waveforms and the comparable current stress at the same output power. However, the SSBBI had the lowest semiconductor count and the easier driver implementation, which proved again the competitiveness of the SSBBI in the family.



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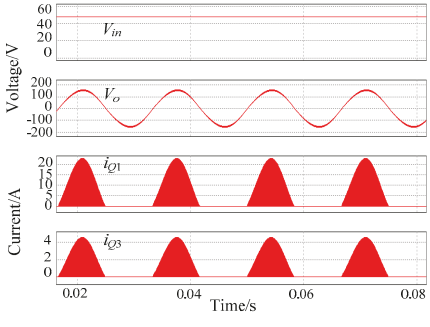

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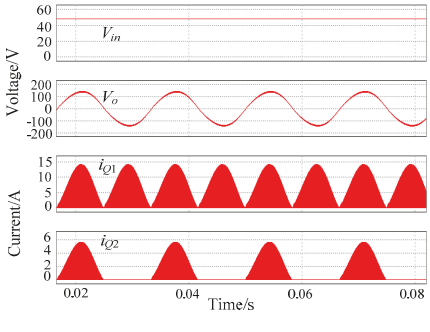


(**c**)

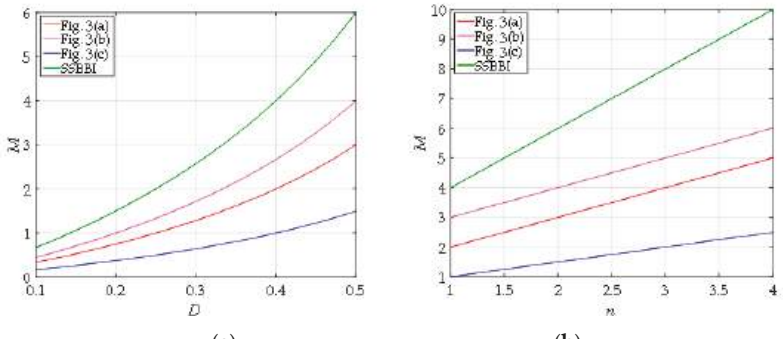
Figure 8. Simulation waveforms of the input voltage, output voltage, and switches' current of the variant topologies: (**a**) Figure 3a, (**b**) Figure 3b, (**c**) Figure 3c.

5.2. Comparison of the Proposed Single-Stage, Buck-Boost Inverter Family

To better appreciate the merits of the proposed single-stage inverter family, a detailed comparison of the proposed topologies is conducted in this section. The voltage conversion ratio of the proposed family and its derivation under the assumption of the CCM operation is summarized in Table 5. The benchmarking of the proposed topologies' voltage conversion ratio with the same turns ratio $n = 2$ is further shown in Figure 9a and with the same duty ratio $D = 0.5$ in Figure 9b. According to Table 5 and Figure 9, the SSBBI had the largest voltage gain in the family. The peak voltage stress analysis was performed and is summarized in Table 6. Lastly, Tables 7 and 8 present the results of the peak current and the RMS current stress analysis of semiconductor devices. As can be seen from Tables 6–8, the voltage and current stresses of the SSBBI were comparable to other topologies in the family. Moreover, as mentioned previously, the SSBBI component count was lower by one or two diodes. Thus, the SSBBI had the optimum circuit composition and characteristics in the family.

Table 5. Comparison of the voltage conversion ratio of the proposed topologies.

Topology	Voltage Gain $M = v_o/V_{in}$
Figure 3a	$M_a = (n+1)\frac{D}{1-D}$
Figure 3b	$M_b = (n+2)\frac{D}{1-D}$
Figure 3c	$M_c = \frac{(n+1)}{2}\frac{D}{1-D}$
SSBBI	$M = 2(n+1)\frac{D}{1-D}$



(**a**) (**b**)

Figure 9. Comparison of the voltage conversion ratio, M, of the proposed single-stage inverter family: (**a**) As function of the duty ratio D (for $n = 2$), (**b**) as function of the turn ratio n (for $D = 0.5$).

Table 6. Comparison of the voltage stress.

Topology	Voltage Stress		
	Low Side Switches	High Side Switches	Diodes
Figure 3a	$V_{in} + \frac{V_{o\max}}{n+1}$	$V_{o\max}$	$(n+1)V_{in}+V_{o\max}$
Figure 3b	$2V_{in}$	$(n+2)V_{in}+V_{o\max}$	$(n+2)V_{in}+V_{o\max}$
Figure 3c	$V_{in} + \frac{2V_{o\max}}{n+1}$	$2V_{o\max}$	$\frac{(n+1)V_{in}}{2} + V_{o\max}$
SSBBI	$2V_{in}$	$2(n+1)V_{in}+V_{o\max}$	/

Table 7. Comparison of the peak current stress.

Topology	Peak Current Stress		
	Low Side Switches	**High Side Switches**	**Diodes**
Figure 3a	$(n+1)I_m + \frac{I_m V_m}{V_{in}}$	$I_m + \frac{I_m V_m}{(n+1)V_{in}}$	$I_m + \frac{I_m V_m}{(n+1)V_{in}}$
Figure 3b	$(n+2)I_m + \frac{I_m V_m}{V_{in}}$	$I_m + \frac{I_m V_m}{(n+2)V_{in}}$	$I_m + \frac{I_m V_m}{(n+2)V_{in}}$
Figure 3c	$\frac{(n+1)}{2} I_m + \frac{I_m V_m}{V_{in}}$	$I_m + \frac{2I_m V_m}{(n+1)V_{in}}$	$I_m + \frac{2I_m V_m}{(n+1)V_{in}}$
SSBBI	$2(n+1)I_m + \frac{I_m V_m}{V_{in}}$	$I_m + \frac{I_m V_m}{2(n+1)V_{in}}$	/

Table 8. Comparison of the RMS current stress.

Topology	RMS Current Stress		
	Low Side Switches	**High Side Switches**	**Diodes**
Figure 3a	$I_{acrms}\sqrt{\frac{3}{4}\frac{V_m^2}{V_{in}^2} + \frac{8}{3\pi}\frac{(n+1)V_m}{V_{in}}}$	$I_{acrms}\sqrt{\frac{1}{2} + \frac{4}{3\pi}\frac{V_m}{(n+1)V_{in}}}$	$I_{acrms}\sqrt{1 + \frac{8}{3\pi}\frac{V_m}{(n+1)V_{in}}}$
Figure 3b	$I_{acrms}\sqrt{\frac{3}{8}\frac{V_m^2}{V_{in}^2} + \frac{4}{3\pi}\frac{(n+2)V_m}{V_{in}}}$	$I_{acrms}\sqrt{\frac{1}{2} + \frac{4}{3\pi}\frac{V_m}{(n+2)V_{in}}}$	$I_{acrms}\sqrt{\frac{1}{2} + \frac{4}{3\pi}\frac{V_m}{(n+2)V_{in}}}$
Figure 3c	$I_{acrms}\sqrt{\frac{3}{4}\frac{V_m^2}{V_{in}^2} + \frac{4}{3\pi}\frac{(n+1)V_m}{V_{in}}}$	$I_{acrms}\sqrt{\frac{1}{2} + \frac{8}{3\pi}\frac{V_m}{(n+1)V_{in}}}$	$I_{acrms}\sqrt{\frac{1}{2} + \frac{8}{3\pi}\frac{V_m}{(n+1)V_{in}}}$
SSBBI	$I_{acrms}\sqrt{\frac{3}{8}\frac{V_m^2}{V_{in}^2} + \frac{8}{3\pi}\frac{(n+1)V_m}{V_{in}}}$	$I_{acrms}\sqrt{1 + \frac{4}{3\pi}\frac{V_m}{(n+1)V_{in}}}$	/

6. Experimental Results and Discussion

6.1. Experimental Results of SSBBI

A 100-W laboratory prototype of the proposed SSBBI was built and tested. The key operation parameters were: Input voltage, V_{in} = 48 V; output voltage, v_o = 110 V/60 Hz; and switching frequency, f_s = 20 kHz. The prototype's view and the components arrangement are shown in Figure 10. The board was designed larger to reserve additional space needed for experimenting with various snubbers and control schemes. The main components of the prototype are summarized in Table 9. The tapped inductor was designed according to the design guide provided by Magnetics-Inc [31], including the magnetic core, the turns, and the wire. A dSPACE system was used to implement the control for the quick experimental study of the SSBBI.

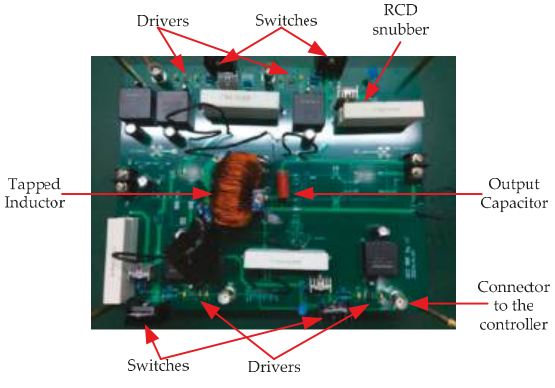


Figure 10. Photo of the experimental prototype of the proposed SSBBI.

Table 9. Main components of the prototype of the proposed SSBBI.

Components	Value/Model
High side switches	IPW90R340C3
Low side switches	IPW65R125C
Driver ICs	1EDI20N12AF
Primary magnetizing inductance	100 μH
Inductor core	55439A2
Inductor Turns	30/45
Output capacitor	2.2 μF

Experimental results are shown in Figures 11 and 12. Figure 11 presents the gate-driving signals for switches at the line period scale and at the switching period scale, respectively. The output voltage and the switch voltage are shown in Figure 12. Observations in Figure 12 clearly indicate that the output voltage was sinusoidal. The THD of the experimental output voltage was around 5% with the open-loop control. This verified that the experimental SSBBI prototype operated according to the theoretical expectations. That is, the proposed SSBBI can achieve the inversion and produce a high-quality sinusoidal output.

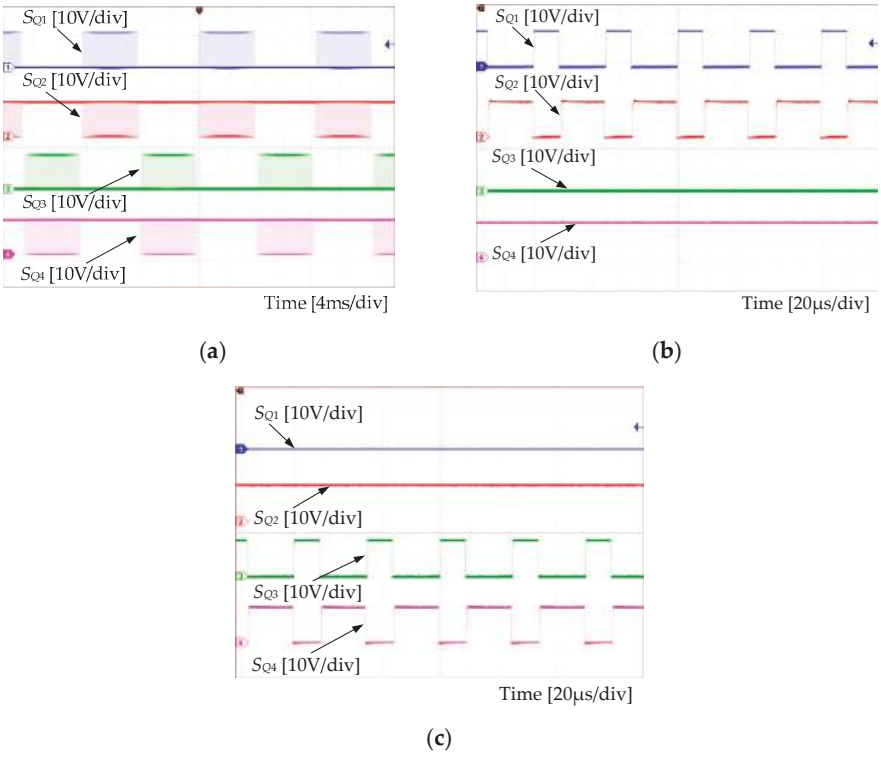


Figure 11. SSBBI's driving signals: (**a**) At the line period scale, (**b**) during positive half-line cycle (at switching period scale), (**c**) negative half-line cycle (at switching period scale).

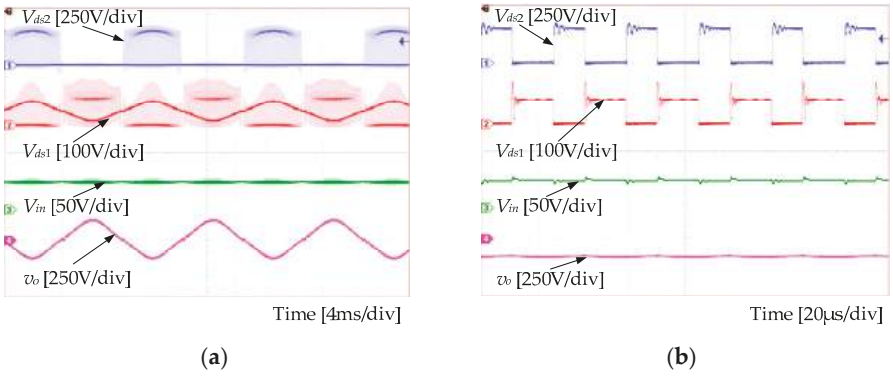


Figure 12. Experimental waveforms of V_{ds2}, V_{ds1}, V_{in}, and v_o: (**a**) At the line period scale, (**b**) at the switching period scale.

In addition, as shown in Figure 12, when zooming into the switch voltage waveform, it was revealed that a voltage spike appeared at the instant of the switch turning off. This is typical for converters with coupled inductors [32]. For the first version of the prototype, a simple RCD snubber was used to verify the basic operation principle of the proposed topologies. The efficiency of 75% was achieved with 100-W output power, where the RCD snubber accounted for a large portion of the total power losses. Moreover, the voltage spike can be suppressed with an appropriate snubber arrangement and design to capture and recycle the leakage energy to achieve much higher efficiency according to the analysis. Snubber details and verification are the subjects of the follow-up research work. What is more, the voltage gain was slightly lower than the theoretical one due to the power losses. With the planned regenerative snubber, the power losses will be less and, thus, the practical voltage gain should be closer to the theoretical one. Overall, the simulation and experimental results were in agreement with the theoretical analysis. Thus, the effectiveness of the proposed inverter family was verified, which had the merits of single-stage conversion, low component count, and easy implementation. These advantages are significant from PV applications, while the efficiency should be further enhanced.

6.2. Comparison of the SSBBI and the State of the Art

After the preliminary experimental test of the SSBBI prototype, the non-optimized performance of the SSBBI could be compared with its counterparts. The comparison results are shown in Table 10. According to Table 10, it is known that the SSBBI had the lowest semiconductor count, almost half of its counterparts. The lower component count makes the SSBBI a simple structure, requiring simpler driving and auxiliary power supplies. These advantages will lead to lower cost, which is a practical concern for the microinverters.

Table 10. Comparison of the SSBBI with the state of the art.

Topologies	Switches Count	Diodes Count	Inductors Count	Input Voltage	Output Voltage	Output Power	Efficiency
[22]	4	8	4	20 V	314 V	100 W	/
[23]	8	0	1 Tapped	100–200 V	110 V	500 W	>96%
Figure 2b [24]	8	0	1 Tapped	40 V	230 V	/	/
[25]	5	2	1 Tapped	60 V	230 V	100 W	86%
SSBBI	4	0	1 Tapped	48 V	110 V	100 W	75%

The efficiency performance of the SSBBI was not outperforming, as mentioned previously. With the theoretical analysis and simulations, the power losses on the RCD snubber were around 15%. Thus, with a proper regenerative snubber, the efficiency will be more than 85% as predicted, where component

optimization can further be applied to improve the efficiency. Nevertheless, the efficiency of 85% will be reasonable for a 100-W, single-stage, buck-boost inverter and comparable with the experimental efficiency in [25].

7. Conclusions

This paper introduced a family of single-stage, buck-boost inverter topologies. Compared to the counterparts, the proposed topologies had a lower component count. The key feature of the proposed family was the application of a multi-winding tapped inductor that helped to attain a higher voltage gain required in PV applications, as microinverters. The operational principle was discussed in this paper, which was supported by simulation and experimental results. A stand-alone experimental SSBBI prototype was designed, built, and tested. Experimental results showed that the proposed topology is capable of delivering a well-shaped sinusoidal output. However, the practical voltage gain was slightly lower than theoretical prediction and the efficiency was not at a very satisfactory level due to the RCD snubber losses and the un-optimized components of the converter, which will be the future work. Overall, the proposed family can present a viable solution to single-stage microinverter applications.

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

n	Turns ratio of the tapped inductor
N_1, N_2, N_3, N_4	Windings of the tapped inductor
Q_1, Q_2, Q_3, Q_4, Q_5	Switches (MOSFETs)
D_1, D_2	Diodes
L_{cp}	Tapped inductor
R_L	Equivalent load resistance
C_o	Output capacitor
V_{in}	Input voltage
i_{in}	Input current
v_o	Output voltage
i_o	Output current
v_{ds1}, v_{ds2}, v_{ds3}, v_{ds4}	Drain-source voltage of the switches Q_1–Q_4
i_{ds1}, i_{ds2}, i_{ds3}, i_{ds4}	Currents through the switches Q_1–Q_4
D	Duty cycle
T_s	Switching period
i_{N1}, i_{N2}, i_{N3}, i_{N4}	Currents through the windings
S_{Q1}, S_{Q2}, S_{Q3}, S_{Q4}	Gating signals the switches Q_1–Q_4
I_o	Average output current
M	Voltage gain
$V_{o\max}$	Maximum output voltage
$D_{\max}$	Maximum duty ratio
$V_{Q1\max}$, $V_{Q2\,\max}$, $V_{Q3\,\max}$, $V_{Q4\,\max}$	Voltage stress on the switches Q_1–Q_4

$v_o(t)$	Time-varying output voltage
$i_o(t)$	Time-varying output current
V_m	Peak output voltage
I_m	Peak output current
ω	Angular frequency
$d(t)$	Time-varying duty ratio
$I_{Q1\max}$, $I_{Q2\max}$	Maximum current of the switch Q_1, Q_2
$i^2_{Q1rmsTs}$, $i^2_{Q2rmsTs}$	Squared RMS current of the switch Q_1, Q_2 within a switching period
I^2_{Q1rms}, I^2_{Q2rms}	Squared RMS current of the switch Q_1, Q_2
I_{Q1rms}, I_{Q2rms}	RMS current of the switch Q_1, Q_2
f_s	Switching frequency
L_m	Tapped-inductor magnetizing inductance

Abbreviations

DC	Direct current
AC	Alternating current
PV	Photovoltaic
MIE/MIC	Module-integrated electronic/converter
MPPT	Maximum power point tracking
SEPIC	Single ended primary inductor converter
PWM	Pulse width modulation
MOSFET	Metal oxide semiconductor field-effect transistor
GaN	Gallium nitride
SSBBI	Single-stage, buck-boost inverter
CCM	Continuous conduction mode
SPWM	Sinusoidal pulse width modulation
THD	Total harmonic distortion
RMS	Root mean square
RCD	Resistor-capacitor-diode

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energies

MDPI

Article

Modular Multilevel Converter for Photovoltaic Application with High Energy Yield under Uneven Irradiance

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Abstract: The direct integration of Photovoltaic (PV) to the three-phase Modular Multilevel Converter (MMC) without *dc–dc* converters results in high-efficiency PV power plant with increased energy yield. The arm power control method for the MMC further improves the extraction of available power under uneven irradiance across different phases of the MMC. However, the uneven irradiance between the sub-modules results in residual voltage that results in harmonics and unbalance components. In this paper, the effect of uneven irradiance across the sub-module of the MMC is investigated with arm power control method. A modified balancing algorithm for the arm power control of the MMC is proposed which enables balanced power to be injected into *ac* grid despite uneven irradiance across the sub-modules in the MMC. The modified balancing algorithm enables to keep the unbalance in the phase currents below 10% and the Total Harmonic Distortion (THD) is confined as per IEEE 519 standard.

Keywords: modular multilevel converter; photovoltaic power system; grid integration; control system; distributed renewable energy source

1. Introduction

The aim of decreasing the emission of greenhouse gas to minimize the impact on the environment has given a tremendous push to power plants based on renewable energy sources. Solar power is abundantly available and many countries have pledged to use 100% renewable energy by 2050 [1]. The large share of energy consumption from renewable sources will be contributed by solar power in the near future. As the extraction of solar power is highly weather-dependent, efficient power converters are necessary that can harvest the available power at all weather conditions.

Modular PV power plants are preferred in locations where energy yield is impacted due to varying weather conditions. Furthermore, modular PV power plants are preferred for commercial installation where partial shading of the panel is a concern. The modular power converters decrease the effects of PV panel mismatch as compared to central power converters where the PV panels are connected to form an array. The modularity of such converters can be a panel, string, or array level. However, in most of the cases the modularity is achieved at the cost of additional *dc–dc* converters [2].

The PV power plant using Cascaded H-Bridge (CHB) converter is studied in [3,4], it operates at high efficiency and increases energy yield due to increase in number of Maximum Power Point Tracking (MPPT). The Modular Multilevel Converter (MMC) proposed in [5] increases the number of MPPT for the same number of switches compared to the CHB converter. The MMC topology, its

variants, and applications are discussed in [6,7]. In [3,8,9], MMC is proposed as an inverter for PV plant. The detailed discussion on topology and control methods for the MMC are presented in [10]. The Figure 1a shows a three-phase double star MMC with Half-Bridge (HB) sub-modules. Each phase of the MMC can be divided into sub-units referred to as upper and lower arm, respectively. Each arm of the MMC has series-connected power electronic blocks referred to as "sub-modules" and an inductor referred to as "arm inductor". The sub-modules can be identical or a combination of different power converter topologies [11]. Typically used sub-modules are half-bridge or full-bridge converters.

Three distinct variants of the topology for connecting the PV panels to the sub-modules are shown in Figure 1b–d. In [12,13], the PV panels are directly connected to the sub-module of the MMC as shown in Figure 1b. The overall efficiency of the PV plant is considerably high as the MMC efficiency is in the range of 99% [14]. Such a system is comparable to the central PV power plant with the additional benefit of an increased number of independent MPPT algorithms, which in this case is equal to the number of sub-modules. This results in higher energy yield and better efficiency than the central PV power plant. In [15], the authors show that the Levelized Cost of Energy (LCOE) for the MMC-based PV plant can be brought lower than that of the central PV plant. The PV panels connected to the sub-modules using the *dc–dc* converters is shown in Figure 1c,d. The use of a *dc-dc* converter allows the decoupling of the PV control and the MMC control. The advantage is that the sub-module capacitor voltages across the MMC are equal; therefore, no modification is necessary in the MMC control. However, in this configuration the overall efficiency is lower compared to PV plant without *dc-dc* converters. In cases where the isolated converters are used, the *dc*-link voltage can be scaled to Medium Voltage (MV) facilitating direct connection of the MMC PV plant to the distribution grid. Thereby, avoiding the need for a step-up transformer typically used for connection to the MV grid.

In [16], the control method for the MMC uses individual Pulse Width Modulators (PWM) for each of the sub-modules. In [17], the method presented in [16] is further extended to control the MMC with the energy sources connected to the sub-modules. The energy in each of the sub-module is locally controlled, which effectively provides the possibility of distributing the control between the main and local controllers. It uses phase-shifted PWM and additional sub-modules are necessary as energy buffers to avoid: (1) large variation of capacitor voltage in the sub-module with an energy source and (2) to avoid very high switching frequency of the sub-module. In [18,19] the non-carrier based approach is used for controlling the MMC when the energy sources are connected to the sub-modules. The non-carrier based control method relies on calculating the fundamental positive and negative sequence circulating current references required to balance the energy between the upper and lower arms of the MMC. In [12], a cost function is presented to optimize the calculation of fundamental circulating current references for extracting the maximum power from the PV and injection of balanced power to the grid. Calculating weights for the cost function is not straight forward and is usually obtained from trial-and-error or extensive simulation cases. In [13], arm power control of MMC is presented, the control system is distributed such that each arm of the MMC is controlled independently. This method also avoids the mathematical computation of the fundamental circulating current references.

Using arm power control the MMC is controlled such that maximum power is extracted from the PV panels and a balanced power is injected to the *ac* grid. The sum of sub-module capacitor voltages in an arm of the MMC is allowed to be different across the upper and lower arms of the MMC. However, within the arm of the MMC, all capacitor voltages are maintained to be equal. This is achieved with the help of sorting and tracking algorithm. The variation of the irradiance is assumed at arm-level for the three-phase MMC leading to six independent MPPT. Such an assumption is viable in large power plants were the effects of shading is minimal. In the case of residential and commercial PV plants, the consequence of shading between the sub-modules cannot be neglected. The shading of PV panels will result in a decrease of power extracted as the MMC is only capable of MPPT at arm-level. This will reduce the yield ratio and LCOE compared to the module-level power converters.

The MMC with arm power control can enable MPPT at the sub-module level. This is achieved by providing individual sub-module capacitor voltage references obtained from the MPPT algorithm. As a result, the sub-module capacitor voltages within the arm of the MMC will not be equal to its average value. Therefore, the voltage inserted by each arm of the MMC will not be equal. As the output voltage in a phase of the MMC is the difference of the upper and the lower arm voltages, the unequal arm voltages will result in a residual voltage at the output terminal. A high deviation in the magnitude of the sub-module capacitor voltages in the arm of the MMC might result in higher residual voltage. This will result in undesired current harmonics and unbalance current components.

In this paper, the effect of unequal sub-module capacitor voltages in the arm of the MMC using arm power control is investigated. A modified sorting and balancing algorithm is proposed that allows the MMC-based PV plant with arm power control to track the MPPT at the sub-module level and inject balanced power to the *ac* grid. The effect of phase current THD is analyzed in the case of uneven irradiance on the sub-modules. The modified sorting and tracking algorithm mitigates the residual voltage between the converter and grid voltages thereby reducing the THD in the phase currents. As a consequence of lower residual voltage the unbalance in the phase current is mitigated. The modified algorithm ensures balanced power injection to the *ac* grid despite extreme unbalance in power generation. The proposed solution makes the arm power control for the MMC suitable for PV applications which are prone to uneven irradiance.

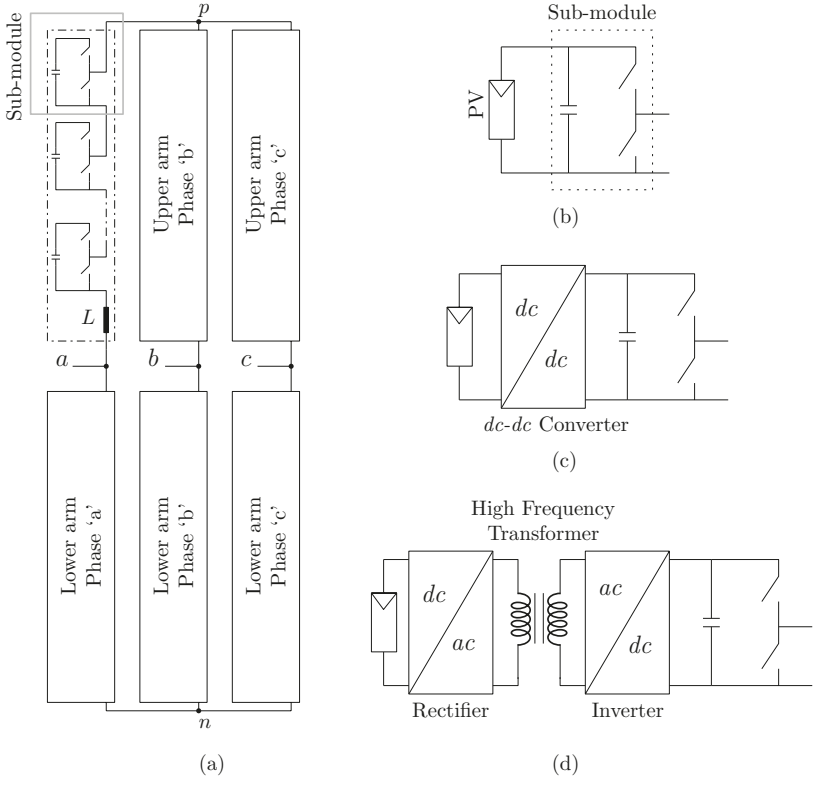


Figure 1. The Modular Multilevel Converter (MMC) and sub-modules with photovoltaic (PV) panels. (**a**) Three-phase MMC indicating the upper and lower arms and the sub-module, (**b**) the HB sub-module with direct connection of the PV panel, (**c**) the PV is connected to the sub-module using a non-isolated *dc-dc* converter, and (**d**) the PV is connected to the sub-module using a isolated converter.

2. Direct Connection of PV Panels to the MMC

To utilize the modularity, increase efficiency, and reliability of the MMC, either a group or individual PV panels is connected directly to the sub-modules of the MMC. Such a configuration inherits the advantages of the MMC such as redundancy, fault-tolerant operation, improved harmonic performance, and hot-swap.

The topology of the MMC with the direct connection of PV panels to the sub-module is shown in Figure 2. Two PV panels are connected in series to form a string which is connected to the sub-module with a series diode to avoid power flow into the PV string. The number of PV panels connected in series or parallel depends on the sizing of the PV plant. Such a configuration is versatile and can have "$6N$" independent MPPT algorithms. The MPPT granularity is defined as the number of independent MPPT. The MMC can be controlled such that MPPT is performed either at sub-module, arm, or MMC level depending on the irradiance pattern. This will ensure high energy yield under different operating conditions.

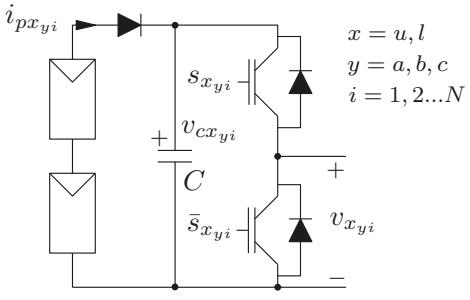


Figure 2. The PV string, two PV panels in series, is connected to the ith sub-module. A diode is included to avoid the power flow into PV string.

The sub-module is said to be inserted when the capacitor is included in the arm of the MMC, i.e., when insertion index $n_{x_{yi}} = 1$. When the capacitor is not included in the arm of the MMC, the corresponding sub-module is said to be bypassed, i.e, when insertion index is $n_{x_{yi}} = 0$. When the sub-module is inserted the output voltage of the sub-module is $v_{x_{yi}} = n_{x_{yi}} \cdot v_{cx_{yi}}$. Therefore, the voltage across the arm of the MMC is sum of the individual sub-module output voltages expressed as

$$v_x = \sum_{i=1}^{N} n_{x_{yi}} \cdot v_{cx_{yi}} \tag{1}$$

The current through the sub-module capacitor voltage is expressed as

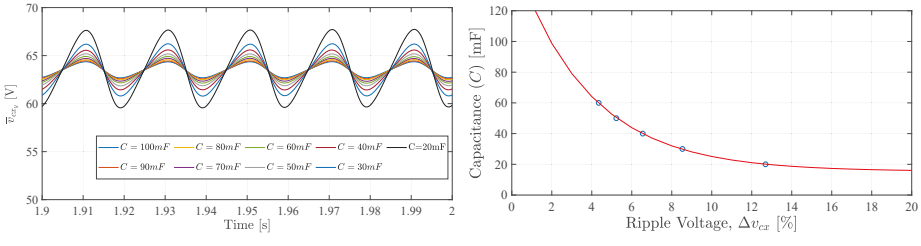
$$C\frac{d}{dt}\left(v_{cx_{yi}}\right) = i_{px_{yi}} + n_{x_{yi}} \cdot i_{x_y} \tag{2}$$

The current from the PV string, $i_{px_{yi}}$, depends on the irradiance level, temperature, and the capacitor sub-module voltage. To track the maximum power on each sub-module, the capacitor voltage is varied and retained at an operating point where the maximum power is extracted from the PV string. When the sub-module is inserted the magnitude of the capacitor voltage changes based on the net current through the capacitor. In this configuration, the PV string current always has a positive average value, however, the arm current alternates sinusoidally. Therefore, the sub-modules in the arm of the MMC have to be selectively inserted or bypassed to reduce the error between the capacitor voltage and the Maximum Power Point (MPP) voltage.

The fundamental sub-module capacitor ripple voltage also influences the power extracted from the PV string. In [20], the effective power loss per panel is studied concerning the sub-module capacitor

voltage ripple. For a fixed switching frequency, irradiance of 1000 W/m^2, and at a constant temperature, it is shown that the decrease of sub-module capacitor voltage ripple from 10% to 5% results in a decrease of effective loss of power extracted from PV panel, i.e., from 2.47% to 0.56%, respectively.

In Figure 3a, the voltage across the sub-module capacitor is shown for capacitance between 20 mF to 100 mF incremented in steps of 10 mF. The data from the Canadian Solar CS6K-285M-FG PV panel is used for the analysis. The maximum allowed sub-module capacitor voltage is 75 V. The switching frequency is selected to be 10 kHz, the irradiance is maintained at 1000 W/m^2. Figure 3 shows the capacitance of the sub-module against the capacitor voltage ripple, to keep the fundamental ripple voltage within 5% of the rated sub-module capacitor voltage the capacitance has to be greater than 50 mF. This capacitance is easily attainable as the sub-module operates at low voltage in the order of few tens of volts.



(**a**) (**b**)

Figure 3. (**a**) Sub-module capacitor voltages for different value of capacitance ranging from 20 mF to 100 mF in steps of 10 mF. (**b**) Sub-module capacitance as a function of ripple voltage at maximum rated capacity of the plant operating with 10 kHz switching frequency.

3. Arm Power Control of MMC Based PV Plant

The block diagram of arm power control proposed in [13] is shown in Figure 4. The power in each arm of the MMC is independently controlled such that (1) each phase of the MMC delivers the same balanced power to the grid, and the (2) maximum power from the PV is extracted in each arm of the MMC. Such a control method leads to MPPT granularity of six.

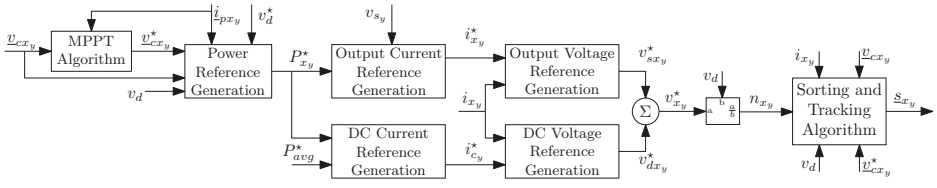


Figure 4. The block diagram of arm power control method of the MMC for PV application proposed in [13].

The MPPT Algorithm provides the individual voltage references for the sub-modules in arm of the MMC as a vector, $\underline{v}^{\star}_{cx_y}$ [1 × N]. These voltage references are added to obtain the desired sum-capacitor voltage reference for individual arm of the MMC, i.e., $v^{\Sigma\star}_{cx_y} = \sum_{i=1}^{N} v^{\star}_{cx_{yi}}$. A Proportional-Integral (PI) controller is used to generate the power reference such that the voltage error between $v^{\Sigma\star}_{cx_y}$ and v_{dc} is driven to zero as

$$P^{\star}_{x_y}(s) = \left[v^{\Sigma\star}_{cx_y}(s) - v_{dc}(s)\right] \cdot \left(k_{p_{dc}} + \frac{k_{i_{dc}}}{s}\right) \tag{3}$$

The *ac* current reference for the arm of the MMC is calculated using the power reference ($P^{\star}_{x_y}$) and the grid voltage at the point of common coupling. The *dc* current reference for the arm of the MMC is obtained with a PI controller to drive the error between the arm power reference and the average arm

power to zero. The average arm power is the mean of power extracted from the PV in each arm of the MMC, defined as in (4).

$$P_{avg} = \frac{1}{6}\left(\sum_{y=a,b,c}\left[\sum_{x=u,l}\left\{\sum_{i=1}^{N} v_{cx_{yi}} \cdot i_{px_{yi}}\right\}\right]\right) \tag{4}$$

The desired voltage reference for each arm of the MMC is obtained as sum of outputs from "output voltage reference generation" and the "*dc* voltage reference generation" blocks, respectively. In the *dc* voltage reference generation, a separate Proportional Resonant (PR) controller is used to suppress the second harmonic circulating current. The insertion index for the arm is calculated as (5) using the arm voltage reference, $v^{\star}_{x_y}$.

$$n_{x_y} = \frac{v^{\star}_{x_y}}{v_{dc}} = \frac{\sum_{i=1}^{N} n_{x_{yi}} \cdot v_{cx_{yi}}}{v_{dc}} \tag{5}$$

The number of sub-module inserted in a switching period is positive integer value of N_{x_y}, i.e., $N_{x_y} = \left\lfloor n_{x_y} \cdot N \right\rceil$. The "Sorting and Tracking Algorithm" is shown in Figure 5, the sub-modules are referred as SM in the algorithm. It enables the insertion and bypass of the sub-module in a switching period such that the sub-module voltages in an arm of the MMC are maintained to their desired values. However, in [13], all the sub-module capacitor voltages in an arm of the MMC are maintained equal. The scenario of the uneven irradiance within the arm of the MMC has not been considered. Such an uneven irradiance within the arm of the MMC will result in different sub-module capacitor voltage references from the MPPT algorithm. The algorithm provides the provision to address unequal irradiance between the sub-modules in an arm of the MMC. The list L_1 contains all the sub-modules with voltage less than their MPPT references, and L_2 contains all the sub-modules with voltage greater than their MPPT references. Based on the polarity of the arm current and the magnitude of the sub-module capacitor voltages, the sub-modules are either inserted or bypassed to maintain the voltage within a threshold ϵ. The only limitation is that all the sub-module capacitor voltage references are identical for an arm of the MMC, i.e., $\forall\ i = 1\ to\ N$, $v_{cx_{yi}} = v^{\star}_{cx}$.

For this study, the parameters of the MMC are identical to the case considered in [13], as tabulated in Table A1. The PI- and PR-controller parameters are shown in Table A2.

Scenario 1

In this scenario, all the PV panels connected to the sub-module of the MMC receive equal irradiance. At the Standard Test Condition (STC), the irradiance is 1000 W/m^2, cell temperature is 25 °C, and airmass is 1.5. The operation of the MMC under STC, where all the sub-module receive equal irradiance of 1000 W/m^2 is shown in Appendix B.

All the sub-module capacitor voltages (v_{cx_y} $[V]$ for x = u, l and y = a, b, c, respectively) are maintained at the desired MPP voltage references, as shown in Appendix B Figure A1a. Active power (P $[kW]$) is injected to the grid by maintaining zero reactive power (Q $[KVAr]$). During the entire operation of the MMC the *dc* and *ac* circulating currents are zero, as shown in Appendix B Figure A1b.

The frequency spectrum of the phase currents injected to the grid for scenario 1 is analyzed in this paper and are shown in Figure 6a–c. The THD for each phases are 1.01%, 1.1%, and 1.04% for phase "a", "b", and "c" currents, respectively. The THD of currents in each phase do not vary significantly. The control of the MMC makes sure that the distortion in all the three phases are minimized by maintaining the desired *ac* voltage reference. The THD is well below the 5% limit as required by IEEE 519 [21] for the scenario 1.

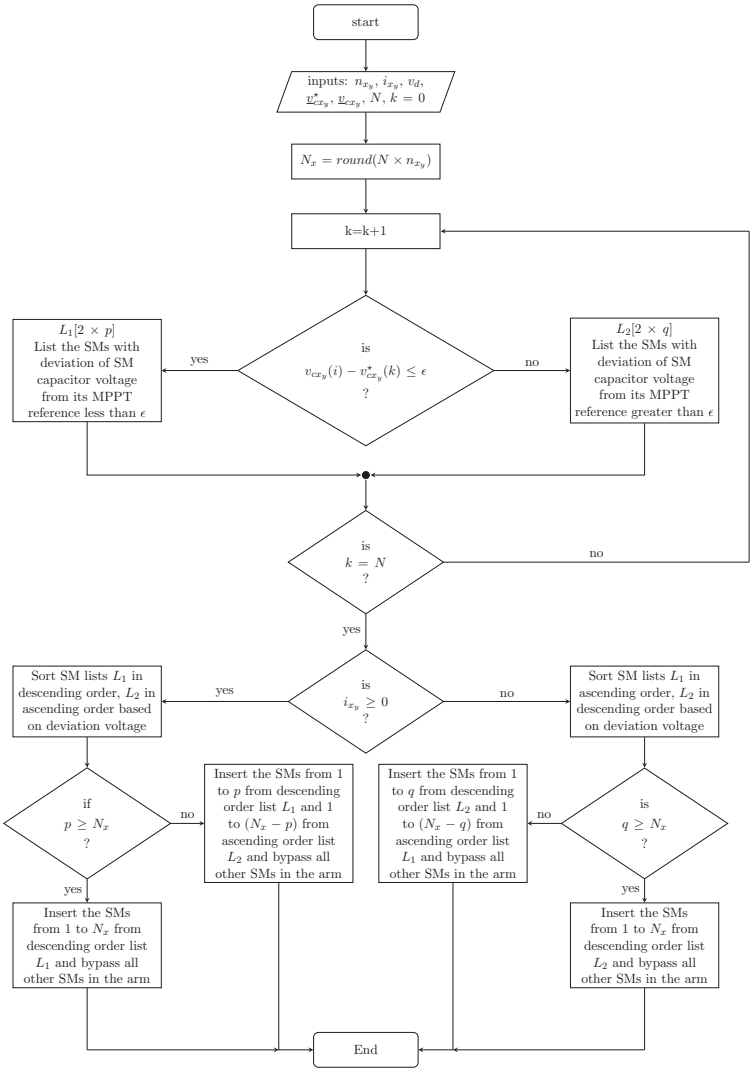
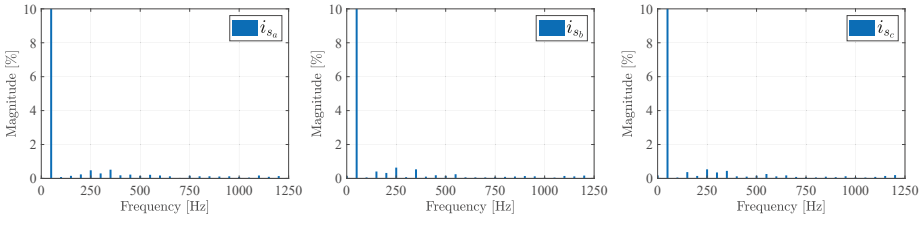


Figure 5. The sorting and tracking algorithm used in the arm power control of the MMC for PV application [13].



(**a**) THD = 1.01% (**b**) THD = 1.1% (**c**) THD = 1.04%

Figure 6. Frequency spectrum of the output phase currents in % with respect to the 50 Hz fundamental current (100%).

The positive, negative and zero sequence components of the three phase currents are shown in Figure 7. The negative sequence component under steady state is less that 1 A. The amount of unbalance in the currents is 0.3% for scenario 1.

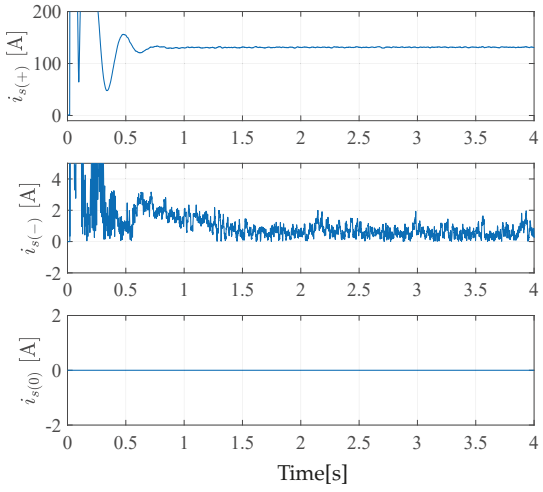


Figure 7. The positive sequence current ($i_{s(+)}$), negative sequence current ($i_{s(-)}$), and zero sequence current ($i_{s(0)}$) for the currents injected to the grid.

4. Uneven Irradiance and Its Consequence

The distribution of irradiance pattern within an arm of the MMC is highly dependent on weather conditions and shading. In [13], the irradiance across the sub-modules in an arm of the MMC are assumed to be identical, and the MPPT is allowed only at arm-level. Such a restriction decreased the harvested power when the irradiance is uneven across the sub-modules in an arm of the MMC. Therefore, the sub-module level MPPT is investigated in this section as scenario 2.

Scenario 2

In this section, a scenario is considered where the irradiance across the PV panels connected to sub-modules in an arm of the MMC is uneven. The sub-modules in an arm of the MMC are allowed to track MPPT by providing individual MPP references from the MPPT algorithm to the power reference generation block in the controller.

If the sub-module capacitor voltage is allowed to follow the MPPT reference within the arm of the MMC, then each sub-module in the arm will deviate from the average value i.e., $v_{cx_{yi}} \neq v_{cx_y}^{\Sigma}/N$.

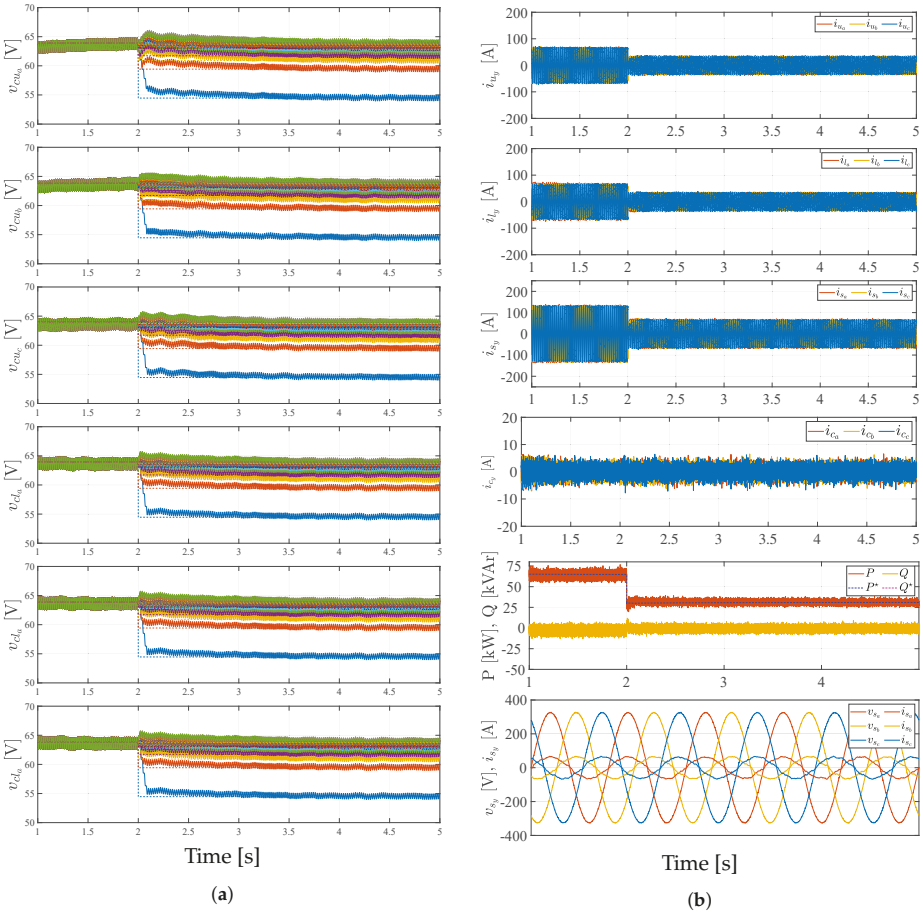
The current controllers will increase or decrease the inserted arm voltage reference to compensate for the voltage difference due to unequal sub-module voltages in the arm of the MMC. However, the sorting and tracking algorithm does not account for the voltage error between the desired arm voltage and the arm voltage to be inserted. This voltage error varies based on choice of sub-modules to be inserted. This leads to a voltage error in each switching period per arm of the MMC, resulting in a residual voltage. This residual voltage per phase (sub-script 'y' is dropped for simplicity) can be expressed as

$$v_{x,\epsilon} = N\left(\frac{v_x^{\star}}{v_{dc}}\right) - \sum_{j=1}^{N_x} v_{cx_{K(j)}} \tag{6}$$

where the 'K' is a row matrix [$1 \times N_{x_y}$] with the sub-module indexes to be inserted. Therefore, $v_{cx_{yK(j)}}$ will yield the value of the sub-module capacitor whose index is stored in the jth location of the row matrix 'K'.

If the residual error is large then it will lead to increased harmonics in the output current. Such a variation is acceptable until the THD is well below 5% as required by IEEE 519 [21] and that no *dc* current greater than 0.5% of the rated current is injected to the grid [22].

The simulation results are shown where the irradiance is linearly distributed across all of the upper and lower arms of the MMC from 10 W/m^2 to 1000 W/m^2. For the scenario considered, the sub-module capacitor voltages are shown in Figure 8a for each of the six arms of the MMC. Figure 8b shows the upper and lower arm currents (i_{u_y} $[A]$, i_{l_y} $[A]$), output currents (i_{s_y} $[A]$), circulating currents (i_{c_y} $[A]$ $\forall$ y = a, b, c), the active and reactive power injected to the grid (P $[kW]$, Q $[kVAr]$), and the last plot shown the voltages (v_{s_y} $[V]$ $\forall$ y = a, b, c) at PCC along with the phase currents (i_{s_y} $[A]$) for 100 ms duration between 4.9 s to 5 s, $\forall$ y = a, b, c.



(**a**) (**b**)

Figure 8. Simulation results for scenario 2: (**a**) Capacitor voltages for all the sub-modules in an arm of the MMC for all three phases. From the top, upper arm phase "a", upper arm phase "b", upper arm phase "c", lower arm phase "a", lower arm phase "b", and lower arm phase "c", respectively. (**b**) The upper and lower arm currents (i_{u_y} $[A]$, i_{l_y} $[A]$), output currents (i_{s_y} $[A]$), circulating currents (i_{c_y} $[A]$ $\forall$ y = a, b, c), the active and reactive power injected to the grid (P $[kW]$, Q $[kVAr]$), and the plot shown the voltages (v_{s_y} $[V]$ $\forall$ y = a, b, c) at PCC and the phase currents (i_{s_y} $[A]$) for 100 ms duration between 4.9 s to 5 s, $\forall$ y = a, b, c.

It is seen that the sorting and tracking algorithm [13] can be used for tracking the MPP voltages for the respective sub-modules by providing the individual references from the MPPT algorithm instead of a average voltage. Moreover, balanced active power is injected to the grid at unity power factor. Since each arm of the MMC produces equal power there is no need to transfer power between the phases of the MMC. Hence the circulating current is zero. The Figure 9 shows the residual voltage defined as in (6). The Figure 10a–c shows the frequency spectrum of the phase currents; the THDs are 5.11%, 5.28%, and 5.36% for phase a, b, and c currents, respectively. It is seen that the THD is higher that the permitted level as per IEEE 519 standard.

The positive, negative, and zero sequence components of the three-phase currents are shown in Figure 11 for the scenario 2. It is seen that the unbalance current injected to the grid is well within 0.5% of the rated magnitude of phase current for the scenario 2.

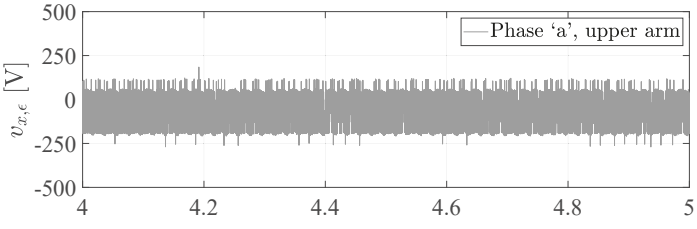
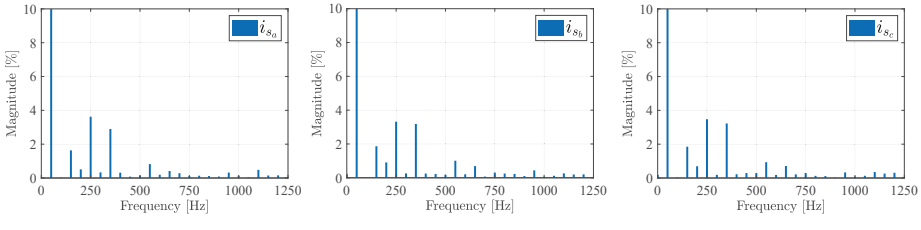


Figure 9. The residual voltage as defined in (6) for the phase a upper arm of the MMC.



(**a**) THD = 5.11%, $\|i_{s_{a_1}}\|$= 43.06A (**b**) THD = 5.11%, $\|i_{s_{b_1}}\|$= 43.11A (**c**) THD = 5.11%, $\|i_{s_{c_1}}\|$= 43.06A

Figure 10. Frequency spectrum of the output phase currents in % with respect to the 50 Hz fundamental current, $\|i_{s_{y_1}}\|$ ∀ y = a, b, c.

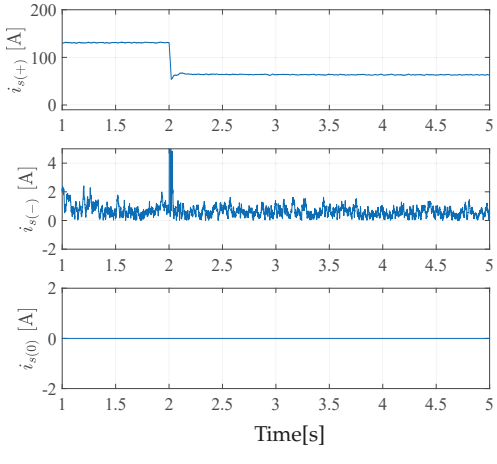


Figure 11. The positive sequence current ($i_{s(+)}$), negative sequence current ($i_{s(-)}$), and zero sequence current ($i_{s(0)}$) for the currents injected to the grid for scenario 2.

5. Modified Sorting and Tracking Algorithm

The sorting and tracking algorithm enables the MMC to have individual MPPT for each sub-module, as seen in scenario 2. This increases the MPPT granularity of the MMC-based PV plant to 6N. For the plant considered in this paper, the MPPT granularity will be 114. The drawback is that the residual error leads to harmonic distortion at the output current. Based on the operating condition, the value of the harmonic distortion might not adhere to the value permitted by the IEEE standard 519 [21]. Therefore, to ensure that for all operating steady-state conditions the harmonic distortion is within the limits, the residual voltage has to be alleviated. The voltage error as per (6) has to be mitigated to reduces the harmonic distortion and any unbalance in current injected to the grid.

In this section, a modified sorting and tracking algorithm is proposed that takes into account the voltage error and increases or decreases the insertion indexes. Further, during a switching period one of the inserted sub-modules is pulse-width modulated such that the average value of the inserted arm voltage inserted matches the desired arm voltage in a switching period. Sub-modules with minimum or maximum voltage deviation from their MPP voltage value are selected, based on the arm current polarity, for PWM in every switching period. Therefore, the duty ratio and the sub-module index for the PWM changes every switching period. By doing so, the loss of power extraction from the PV panel due to the PWM of the sub-module is minimized.

The sorting and tracking algorithm selects the N_x sub-modules to be inserted per arm of the MMC in a given phase, with this the residual voltage is computed as per (6). If the error is negative, then the insertion index is increased to minimize the error. If the error is positive, then the insertion index is decreased to mitigate the residual voltage. The insertion index is either increased or decreased until the magnitude of the ratio as per (7) is less than one, this will be the modified number of sub-modules to be inserted "$N_x^\star$".

$$w = \frac{|v_{x,\epsilon}|}{\sum_{j=1}^{N_x} v_{cx_{K(j)}}} \tag{7}$$

If the arm current is positive (or negative) then the sub-module with the lowest (or highest) voltage in the set of sub-modules to be inserted is selected for modulation. The duty ratio is the calculated as

$$d = \frac{\left| N\left(\frac{v_x^\star}{v_{dc}}\right) - \sum_{j=1}^{N_x^\star} v_{cx_{K(j)}} \right|}{\sum_{j=1}^{N_x^\star} v_{cx_{K(j)}}} < 1 \tag{8}$$

Scenario 3

This scenario is identical to scenario 2; however, the modified sorting and tracking algorithm is used to mitigate the THD which is observed in scenario 2. The index of the sub-module to be modulated and the duty ratio "*d*" is shown in Figure 12 for 10 ms duration. The index and the duty ratio is modified every switching period so that the average value of the arm voltage is equal to the desired arm voltage.

Figure 13 shows the residual voltage as a result of using modified sorting and a tracking algorithm. The average value of the residual voltage is now zero, and the instantaneous magnitude of the residual voltage over a switching period is lower than the value seen in scenario 2.

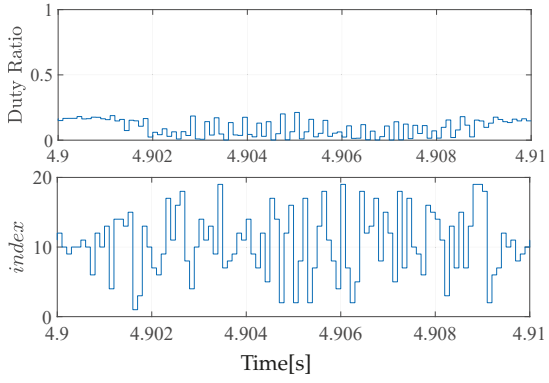


Figure 12. The duty ratio for Pulse Width Modulators (PWM) and the index of the sub-module to be modulated.

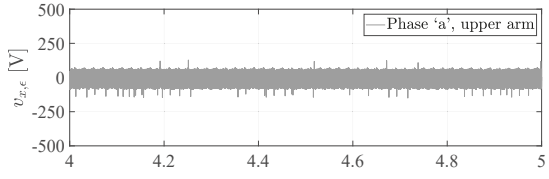
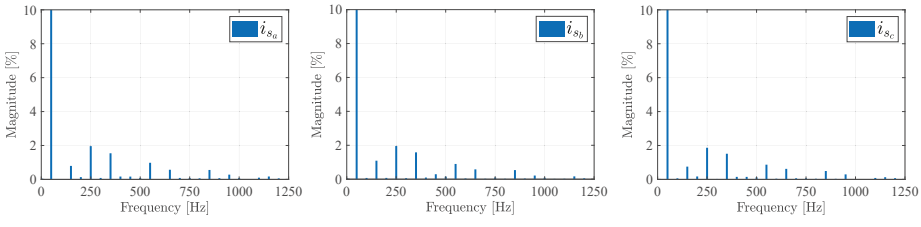


Figure 13. The residual voltage as defined in (6) for the phase "a" upper arm of the MMC with modified ST algorithm.

The frequency spectrum of the output phase currents is shown in Figure 14. the THD is calculated to be 3.68%, 3.75%, and 3.56% for phase a, b, and c currents, respectively. The THD is decreased by 30% bringing it well within the permitted level as per IEEE 519 standard.



(**a**) THD = 3.68%, $\|i_{s_{a_1}}\|$ = 44.71A (**b**) THD = 3.75%, $\|i_{s_{b_1}}\|$ = 44.88A (**c**) THD = 3.56%, $\|i_{s_{c_1}}\|$ = 44.74A

Figure 14. Frequency spectrum of the output phase currents in % with respect to the 50 Hz fundamental current, $\|i_{s_{y_1}}\|$ ∀ y = a, b, c.

6. Conclusions

The simulation results of the MMC-based PV plant with arm power control are presented specifically when the irradiance is uneven within the arms of the MMC. The consequence of uneven irradiance on each sub-modules of the arm of the MMC is discussed in terms of harmonic distortion and unbalance in the phase currents. It is seen that the MMC-based PV plant is capable of tracking the maximum power at individual sub-module level brining the MPPT granularity to "6· N". This is achieved without any additional *dc-dc* converters.

It is further noticed that, based on the operating conditions, the harmonic distortion in the output currents increases due to residual voltage between the actual inserted arm voltage and the desired arm voltage. The effect of this residual voltage is the increase in THD and the amount of unbalance

in the output current. Though there is no strict requirement on the unbalance, usually a balanced operation is desired for stable operating conditions. Furthermore, there is a strict requirement on the THD of the currents injected into the *ac* grid. It is seen that based on the operating load and irradiance pattern on the PV panels connected to the MMC the THD values can be higher than 5%, which is the allowed limit.

In this paper a modified sorting and tracking algorithm is proposed to the arm power control of the MMC. It enables the effective operation of the MMC-based PV plant even under unequal irradiance patterns across the sub-modules. For the case considered, it is shown that the THD is reduced by 30%, bringing it well within the permitted limit.

Author Contributions: Conceptualization, methodology, and validation: A.B.A., formal analysis: R.T. and D.S. Article is written by A.B.A. Article is reviewed by R.T., L.E.N., and D.S. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflicts of interest

Nomenclature

$x = u \text{ or } l$	Upper (u) or Lower (l) arm
$y = a,\ b \text{ or } c$	Phase a, b or c
$i = 1, 2, 3...$	Sub-Module index
N	Number of Sub-Modules
$n_{x_{y_i}}$	Insertion index of ith Sub-Module in upper or lower arm per phase
n_{x_y}	Insertion index of upper or lower arm per phase
i_{x_y}	Upper or lower arm current per phase
i_{s_y}	Output current per phase
i_{c_y}	Circulating current per phase
$i_{px_{yi}}$	PV string current in ith Sub-Module per phase
$v_{cx_{yi}}$	Capacitor voltage of ith Sub-Module in upper or lower arm per phase
$v_{cx_y}^{\Sigma}$	Sum capacitor voltage of upper or lower arm per phase
v_{x_y}	Inserted upper or lower arm voltage per phase
v_{s_y}	Output voltage in each phase
v_{cx_y}	Average arm capacitor voltage per phase
v_{dc}	Effective DC link voltage
P	Three phase active power
Q	Three phase reactive power

Appendix A. Parameters of Modular Multilevel Converter

Table A1. Parameters of MMC Converters.

Parameters	Symbol	Value
Rated Apparent Power	S_s	65 kVA
Rated Output Voltage	v_s	400 V
Rated Output Current	i_s	141 A
Output Frequency	f_s	50 Hz
Maximum DC Voltage	v_{dc}	1.4 kV
SM Capacitance	C	20 mF
Arm Inductance	L_a	1.2 mH
Rated SM Voltage	v_{cx}	63.4 V
Maximum SM Voltage	$v_{cx(max)}$	75 V
Switching Frequency	f_{sw}	10,000 Hz
Number of SMs	N	19